# CEM9400A

P-Channel Enhancement Mode Field Effect Transistor

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FEATURES

- $-30V$, $-3.4A$, $R_{DS(ON)}=130m\Omega$ @$V_{GS}=-10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.

SO-8

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D   D   D   D
8   7   6   5




1   2   3   4
S   S   S   G
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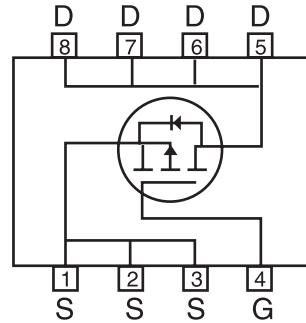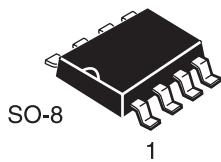
ABSOLUTE MAXIMUM RATINGS ($T_A=25°C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous[a] @$T_J=125°C$	I_D	±3.4	A
-Pulsed[b]	I_{DM}	±10	A
Drain-Source Diode Forward Current [a]	I_S	-1.9	A
Maximum Power Dissipation[a]	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient[a]	$R_{\theta JA}$	50	°C/W

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ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-2	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm20V, V_{DS}=0V$			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-1A$			130	$m\Omega$
		$V_{GS}=-4.5V, I_D=-0.5A$			250	$m\Omega$
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=-5V, V_{GS}=-10V$	-10			A
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-3.4A$		4		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	$V_{DS}=-10V, V_{GS}=0V$ $f=1.0MHz$		330	700	pF
Output Capacitance	C_{OSS}			250	520	pF
Reverse Transfer Capacitance	C_{RSS}			90	200	pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	$V_D=-10V,$ $I_D=-1A,$ $V_{GS}=-10V,$ $R_{GEN}=6\Omega$		15	40	ns
Rise Time	t_r			20	40	ns
Turn-Off Delay Time	$t_{D(OFF)}$			60	90	ns
Fall Time	t_f			20	50	ns
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-3.4A,$ $V_{GS}=-10V$		10	25	nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			3		nC

ELECTRICAL CHARACTERISTICS (T$_A$=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ^c	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^{b}						
Diode Forward Voltage	V$_{SD}$	V$_{GS}$ = 0V, Is =-1.25A			-1.3	V

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Notes

a.Surface Mounted on FR4 Board, t ≤10sec.

b.Pulse Test:Pulse Width ≤300 μ s, Duty Cycle ≤ 2%.

c.Guaranteed by design, not subject to production testing.
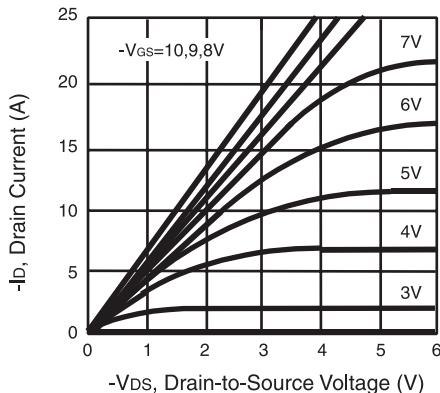
Figure 1. Output Characteristics
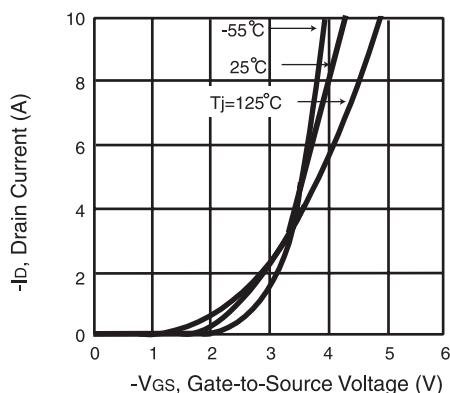
Figure 2. Transfer Characteristics
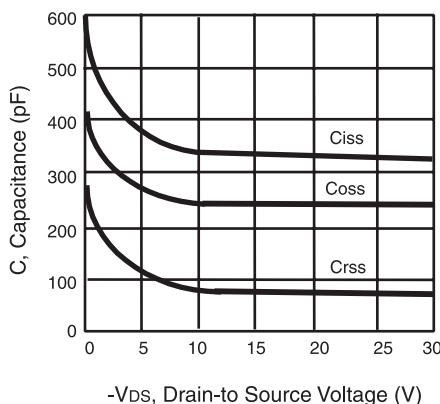
Figure 3. Capacitance
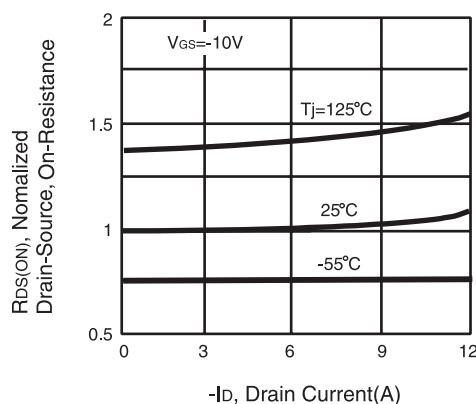
Figure 4. On-Resistance Variation with Drain Current and Temperature

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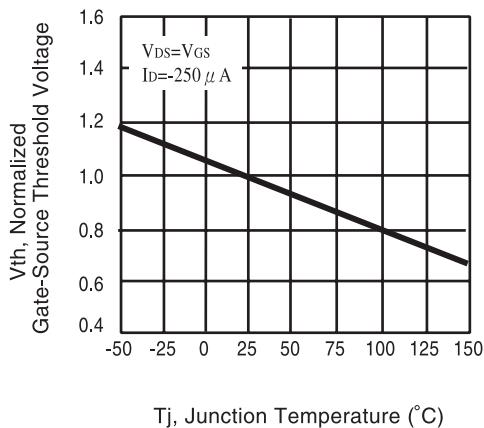
**Figure 5. Gate Threshold Variation with Temperature**

$V_{DS}=V_{GS}$
$I_D=-250\mu A$

Vth, Normalized Gate-Source Threshold Voltage
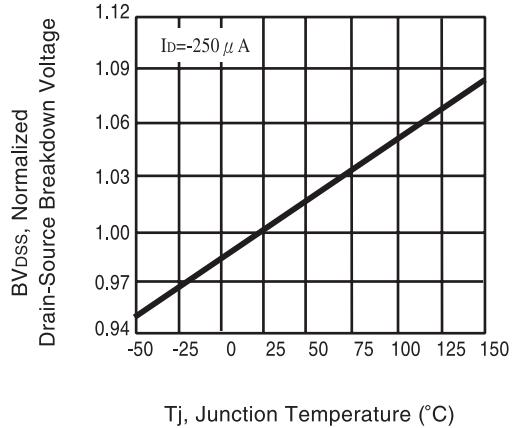
Tj, Junction Temperature (°C)

Figure 6. Breakdown Voltage Variation with Temperature

$I_D=-250\mu A$

BVDSS, Normalized Drain-Source Breakdown Voltage

Tj, Junction Temperature (°C)

Figure 7. Transconductance Variation with Drain Current

g_{FS}, Transconductance (S)

$V_{DS}=-15V$
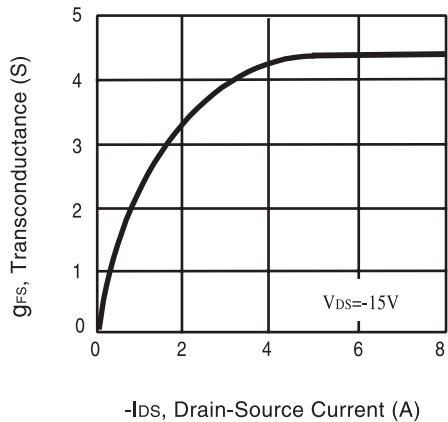
-IDS, Drain-Source Current (A)

Figure 8. Body Diode Forward Voltage Variation with Source Current

$V_{DS}=0V$

-Is, Source-drain current (A)
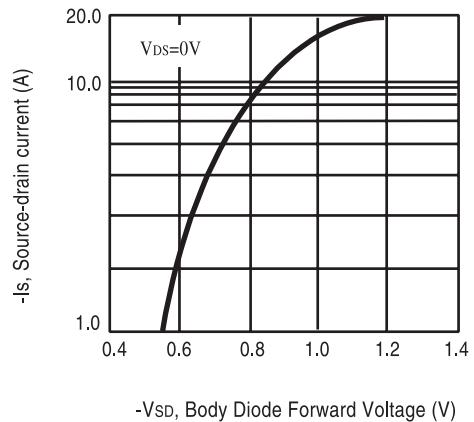
-VSD, Body Diode Forward Voltage (V)

Figure 9. Gate Charge

$V_{DS}=-10V$
$I_D=-3.4A$

VGS, Gate to Source Voltage (V)
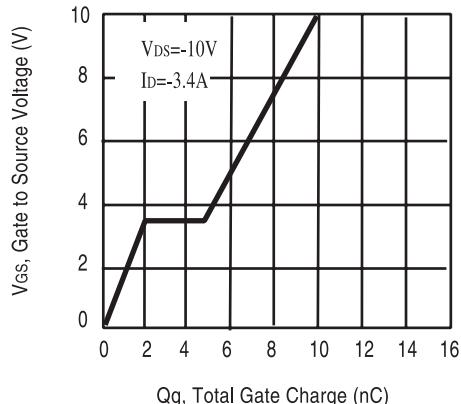
Qg, Total Gate Charge (nC)

Figure 10. Maximum Safe Operating Area

-ID, Drain Current (A)

RDS(ON) Limit
10ms
100ms
1s
DC

$V_{GS}=-10V$
Single Pulse
$T_A=25°C$
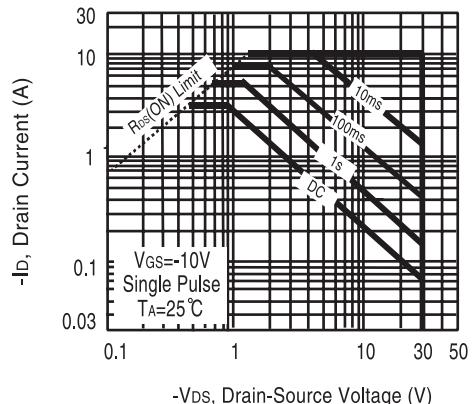
-VDS, Drain-Source Voltage (V)
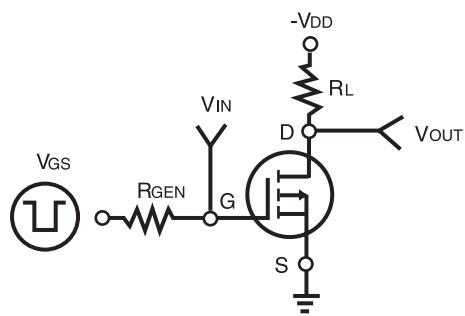
Figure 11. Switching Test Circuit
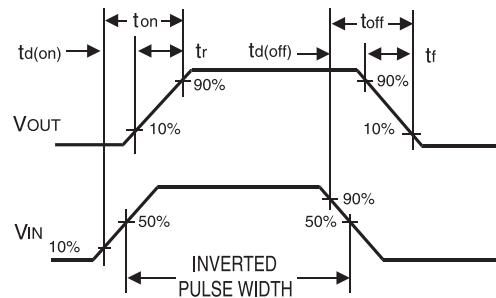

Figure 12. Switching Waveforms

Square Wave Pulse Duration (sec)
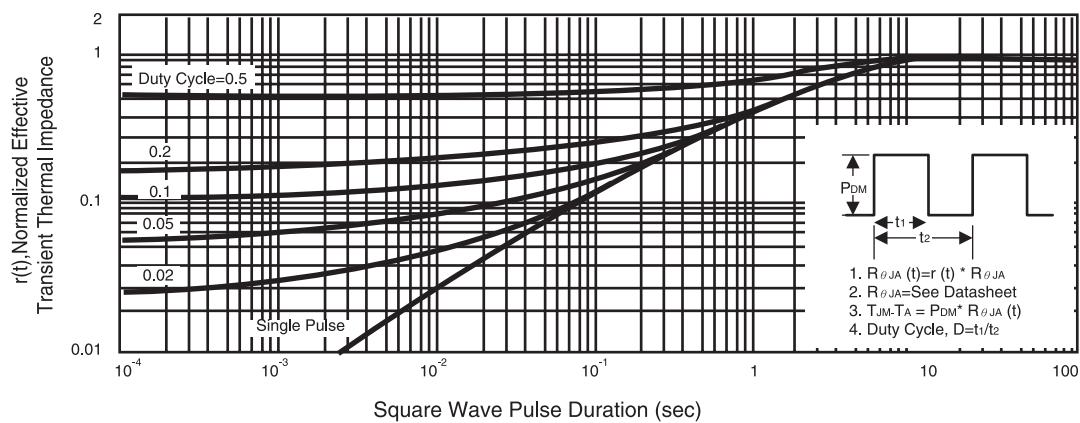
Figure 13. Normalized Thermal Transient Impedance Curve