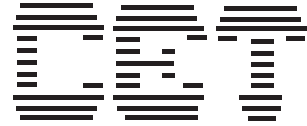


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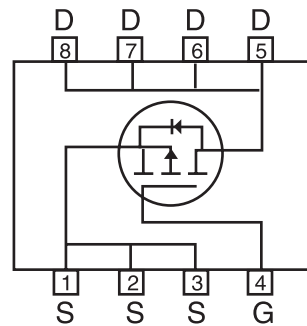
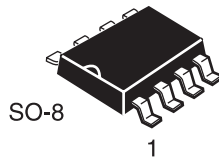
MAY 1999

## P-Channel Enhancement Mode Field Effect Transistor

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### FEATURES

- -20V , -7.7A ,  $R_{DS(ON)}=25m\Omega$  @  $V_{GS}=-4.5V$ .  
 $R_{DS(ON)}=35m\Omega$  @  $V_{GS}=-2.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	-20	V
Gate-Source Voltage	VGS	$\pm 8$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^\circ C$ -Pulsed <sup>b</sup>	ID	$\pm 7.7$	A
	IDM	$\pm 30$	A
Drain-Source Diode Forward Current <sup>a</sup>	IS	-2.3	A
Maximum Power Dissipation <sup>a</sup>	PD	2.5	W
Operating Junction and Storage Temperature Range	TJ, TSTG	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	50	$^\circ C/W$
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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V			-1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±8V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.6			V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-7.7A		19	25	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-6.6A		24	35	mΩ
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =-5V, V <sub>GS</sub> =-4.5V	-30			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-7.7A		23		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V f=1.0MHz		2690	3500	pF
Output Capacitance	C <sub>OSS</sub>			1300	1700	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			615	800	pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-6V I <sub>D</sub> =-1A, V <sub>GEN</sub> =-4.5V, R <sub>GEN</sub> =6Ω		60	80	ns
Rise Time	t <sub>r</sub>			90	130	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			310	400	ns
Fall Time	t <sub>f</sub>			190	250	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-6V, I <sub>D</sub> =-7.7A, V <sub>GS</sub> =-4.5V		46	80	nC
Gate-Source Charge	Q <sub>gs</sub>			6		nC
Gate-Drain Charge	Q <sub>gd</sub>			13		nC

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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -2.3A		-0.7	-1.2	V

- Notes
- a. Surface Mounted on FR4 Board, t ≤ 10sec.
  - b. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
  - c. Guaranteed by design, not subject to production testing.

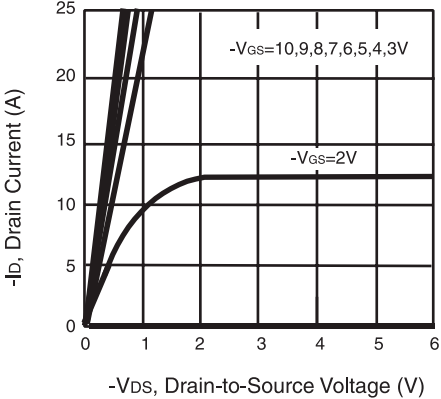


Figure 1. Output Characteristics

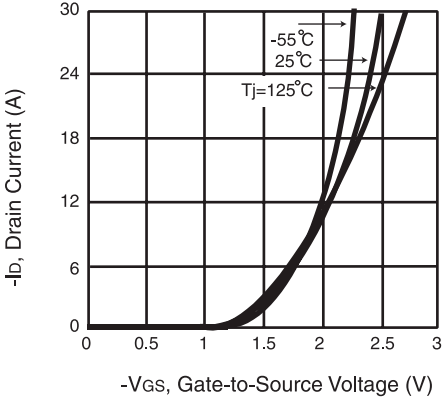


Figure 2. Transfer Characteristics

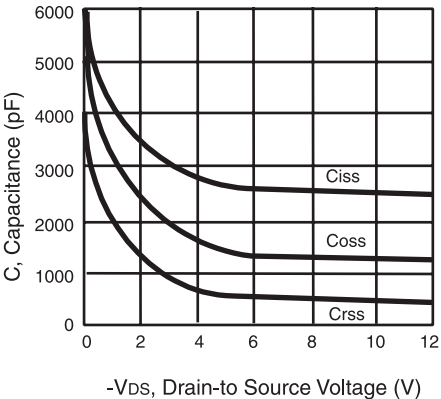


Figure 3. Capacitance

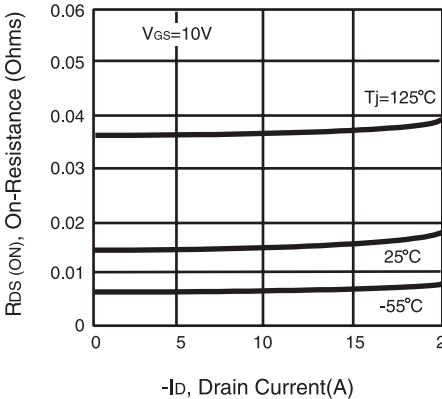
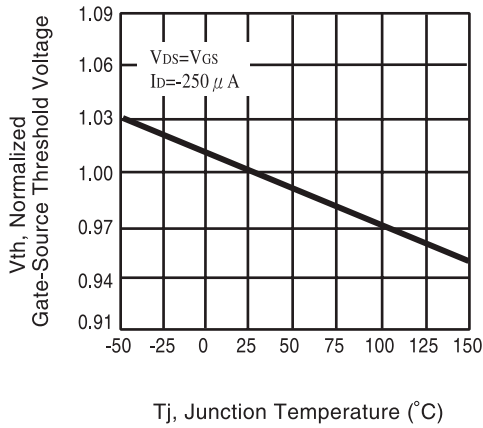


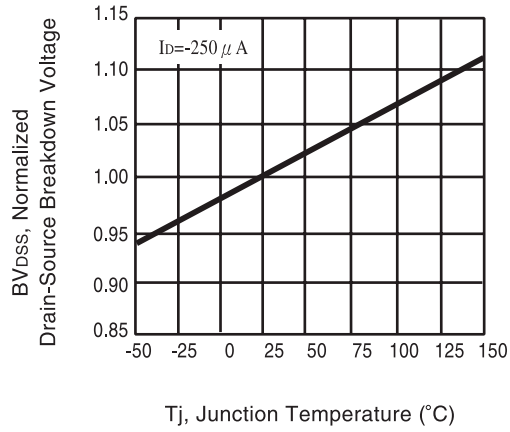
Figure 4. On-Resistance Variation with Drain Current and Temperature

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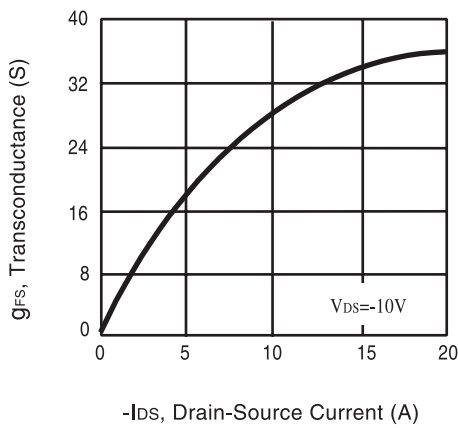
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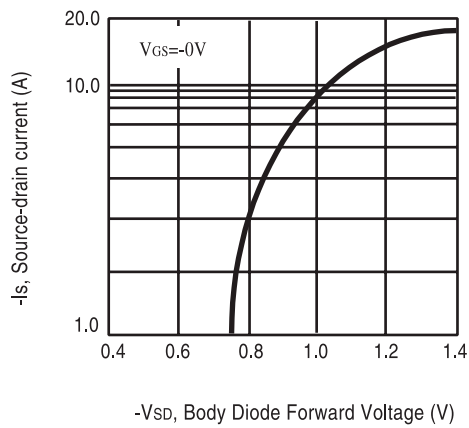
**Figure 5. Gate Threshold Variation with Temperature**



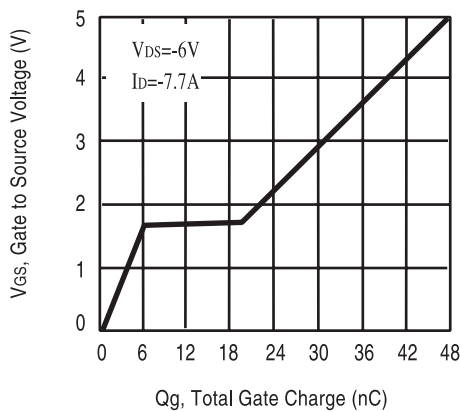
**Figure 6. Breakdown Voltage Variation with Temperature**



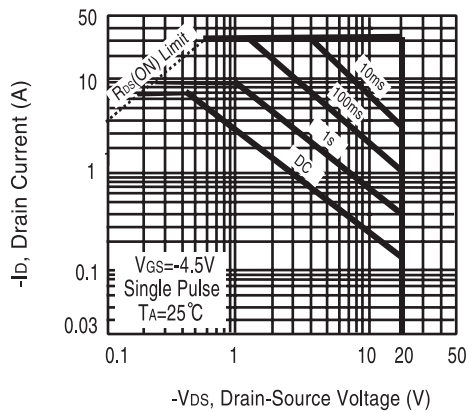
**Figure 7. Transconductance Variation with Drain Current**



**Figure 8. Body Diode Forward Voltage Variation with Source Current**



**Figure 9. Gate Charge**



**Figure 10. Maximum Safe Operating Area**

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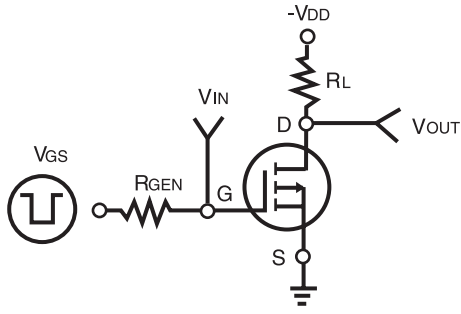


Figure 11. Switching Test Circuit

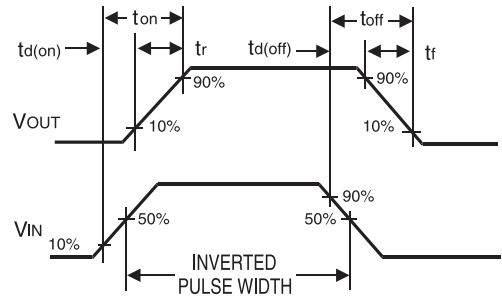


Figure 12. Switching Waveforms

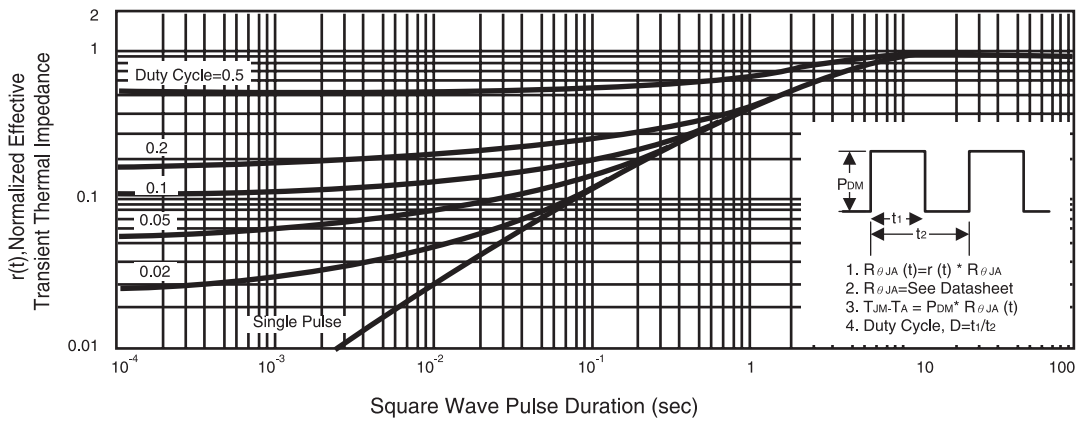


Figure 13. Normalized Thermal Transient Impedance Curve