

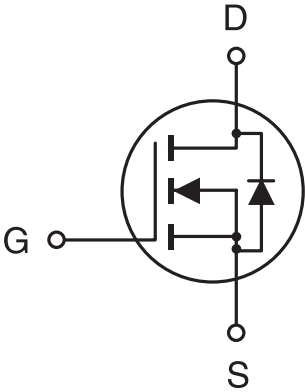
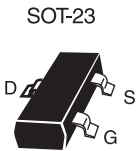
# CES7002A

March 1998

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 60V , 0.28A ,  $R_{DS(ON)}=2\Omega$  @  $V_{GS}=10V$ .  
 $R_{DS(ON)}=3\Omega$  @  $V_{GS}=5V$ .
- High dense cell design for low  $R_{DS(ON)}$ .
- Rugged and reliable.
- SOT-23 Package.



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### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous <sup>a</sup> @ $T_J=125^\circ\text{C}$ -Pulsed <sup>b</sup>	$I_D$	280	mA
	$I_{DM}$	1500	mA
Drain-Source Diode Forward Current <sup>a</sup>	$I_S$	280	mA
Maximum Power Dissipation <sup>a</sup>	$P_D$	300	mW
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-65 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	$R_{\theta JA}$	417	$^\circ\text{C/W}$
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## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =10μA	60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	2.1	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA		1.2	2	Ω
		V <sub>GS</sub> =5V, I <sub>D</sub> =50mA		1.7	3	Ω
On-State Drain Current	I <sub>D(ON)</sub>	V <sub>DS</sub> =7V, V <sub>GS</sub> =10V	500			mA
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =7V, I <sub>D</sub> =200mA	80	170		mS
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		38	50	pF
Output Capacitance	C <sub>OSS</sub>			19	25	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			3	5	pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =30V, I <sub>D</sub> =200mA, V <sub>GS</sub> =10V, R <sub>GEN</sub> =25Ω		23	30	ns
Rise Time	t <sub>r</sub>			15	20	ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			76	100	ns
Fall Time	t <sub>f</sub>			15	20	ns

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_s = 400\text{mA}$		0.8	1.2	V

### Notes

- Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.

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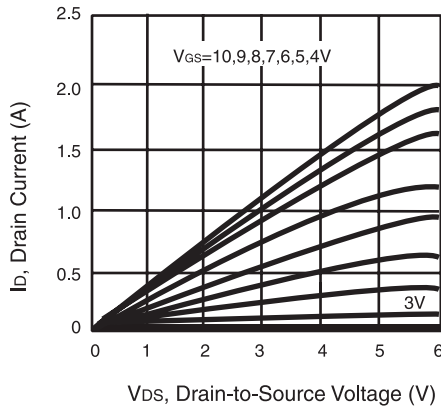


Figure 1. Output Characteristics

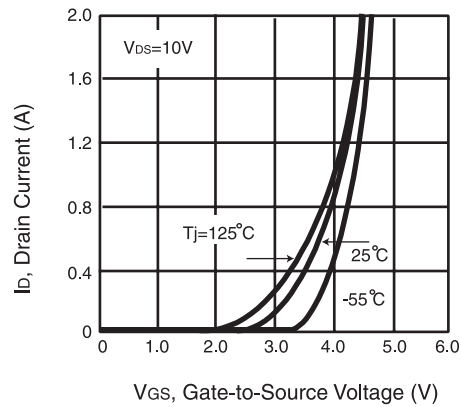


Figure 2. Transfer Characteristics

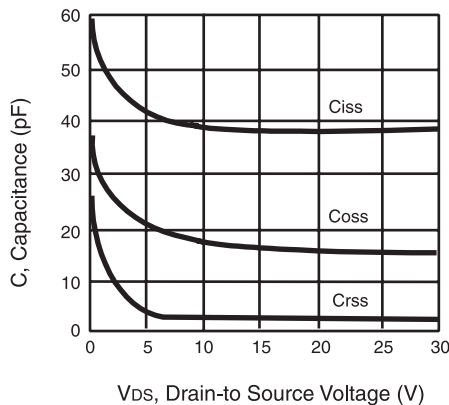


Figure 3. Capacitance

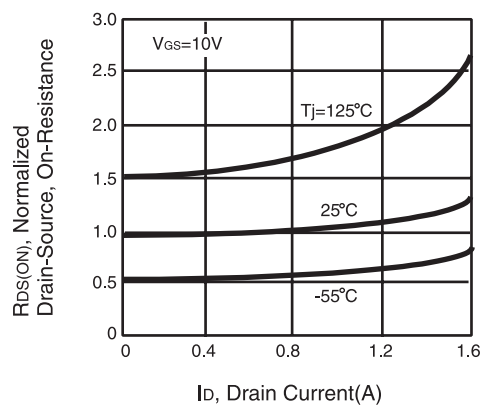


Figure 4. On-Resistance Variation with Drain Current and Temperature

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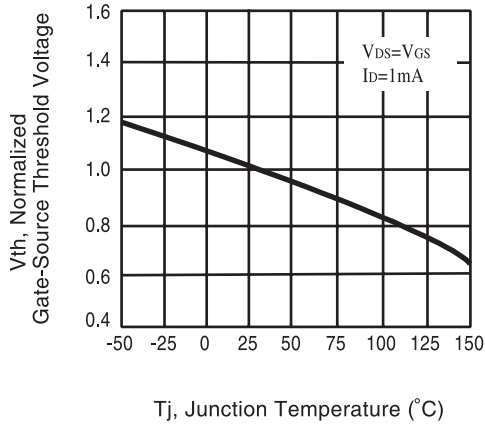


Figure 5. Gate Threshold Variation with Temperature

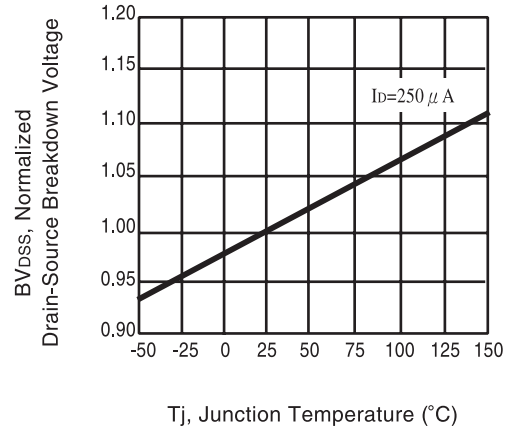
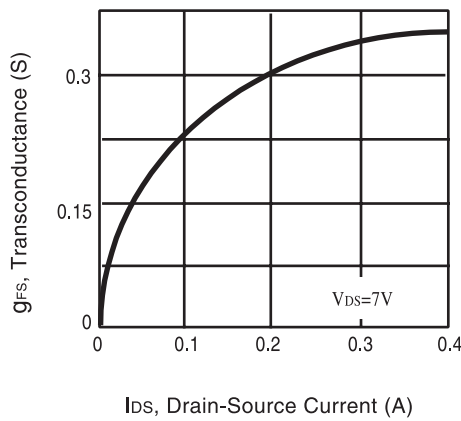


Figure 6. Breakdown Voltage Variation with Temperature



with Drain Current

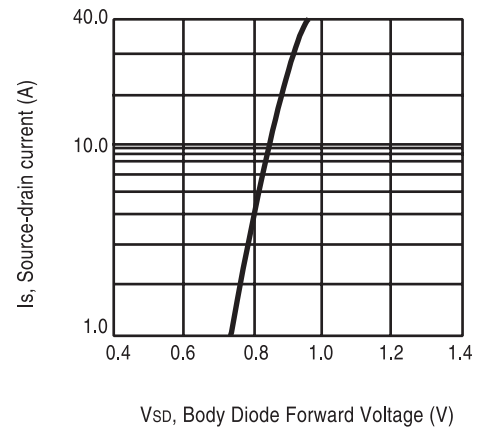


Figure 8. Body Diode Forward Voltage Variation with Source Current

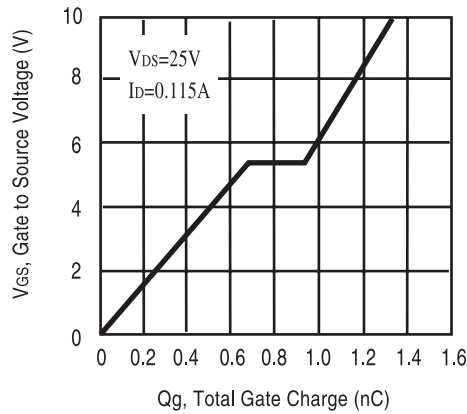


Figure 9. Gate Charge

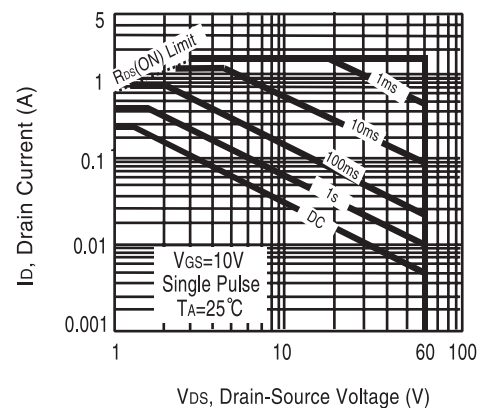


Figure 10. Maximum Safe Operating Area

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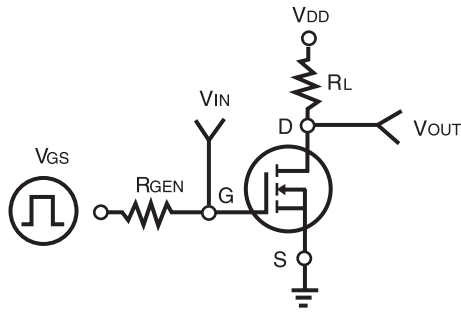


Figure 11. Switching Test Circuit

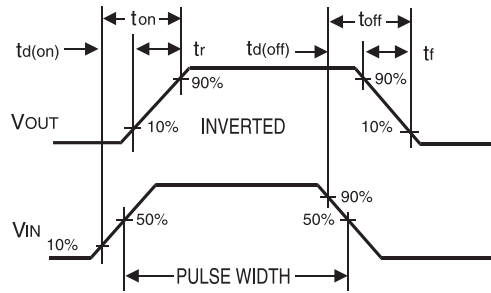


Figure 12. Switching Waveforms

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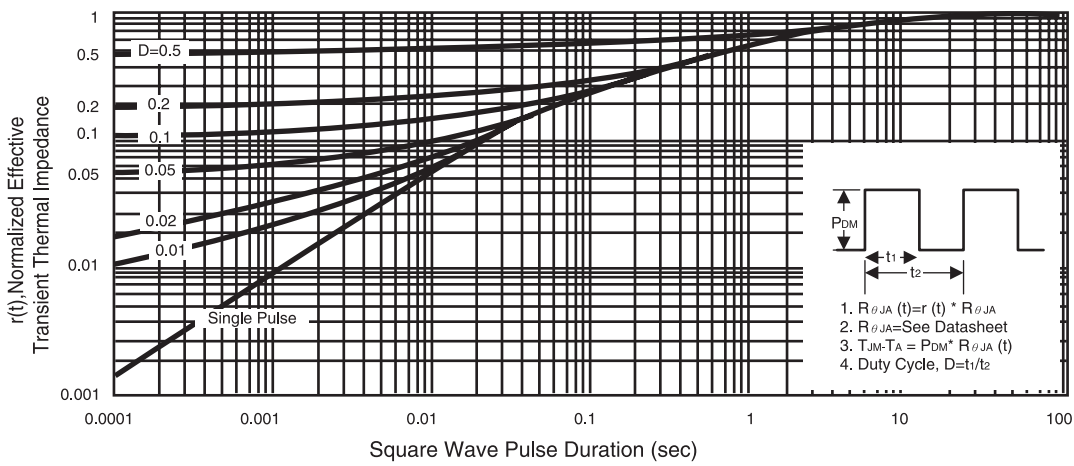


Figure 13. Normalized Thermal Transient Impedance Curve