CS51221

Enhanced Voltage Mode PWM Controller

Description

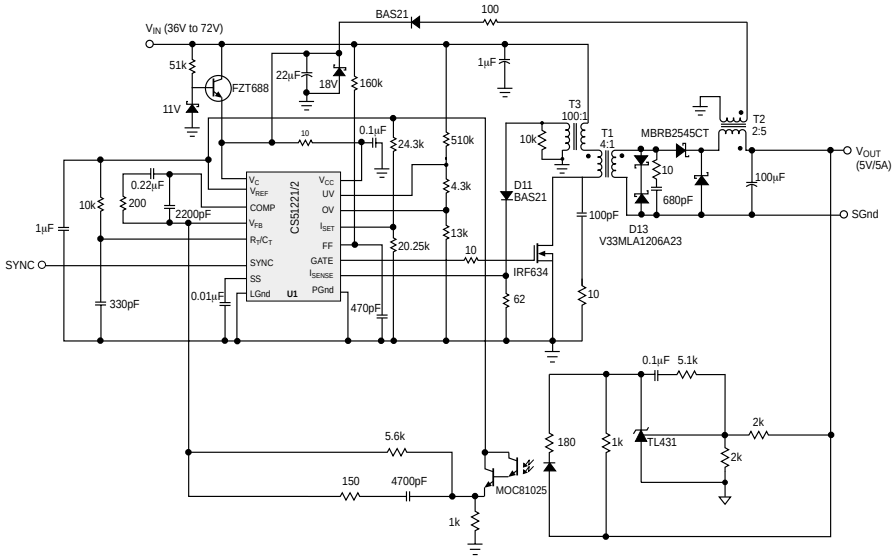
The CS51221 fixed frequency feed forward voltage mode PWM controller contains all of the features necessary for basic voltage mode operation. This PWM controller has been optimized for high frequency primary side control operation. In addition, this device includes such features as: Soft Start, accurate duty cycle limit control, less than 50μA startup current, over and under voltage protection, and bidirectional synchronization. The CS51221 is available in 16 lead PDIP and SO narrow surface mount packages.

Features

- **1MHz Frequency Capability**
- **Fixed Frequency Voltage Mode Operation, with Feed Forward**
- **Thermal Shutdown**
- **Under Voltage Lock-out**
- **Accurate Programmable Max Duty Cycle Limit**
- **1A Sink/Source Gate Drive**
- **Programmable Pulse by Pulse Over Current Protection**
- **Leading Edge Current Sense Blanking**
- **75ns Shutdown Propagation Delay**
- **Programmable Soft Start**
- **Under Voltage Protection**
- **Over Voltage Protection with Programmable Hysteresis**
- **Bidirectional Synchronization**
- **25ns GATE Rise and Fall Time (1nF load)**
- **3.3V 3% Reference Voltage Output**

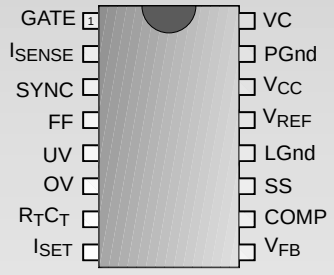
Application Diagram

36V-72V to 5V/5A converter



Package Options

16 Lead SO Narrow & PDIP



Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

Absolute Maximum Ratings

Operating Junction Temperature, T_J . . . . . Internally Limited
Lead Temperature Soldering:
Wave Solder (through hole styles only) . . . . . 10 Sec. max 260°C Peak
Reflow (SMD styles only) . . . . . 60 Sec max. above 183°C, 230°C Peak
Storage Temperature Range, T_S . . . . . -65 to 150°C
ESD (Human Body Model) 2kV

PIN SYMBOL	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
GATE	Gate Drive Output	15V	-0.3V	1.0A Peak 200mA DC	1.0A Peak 200mA DC
I_{SENSE}	Current Sense Input	6V	-0.3V	1mA	1mA
R_TC_T	Timing Resistor/Capacitor	6V	-0.3V	1mA	10mA
FF	Feed Forward	6V	-0.3V	1mA	25mA
COMP	Error Amp Output	6V	-0.3V	10mA	20mA
V_{FB}	Feedback Voltage	6V	-0.3V	1mA	1mA
SYNC	Sync Input	6V	-0.3V	10mA	10mA
UV	Under Voltage	6V	-0.3V	1mA	1mA
OV	Over Voltage	6V	-0.3V	1mA	1mA
I_{SET}	Current Set	6V	-0.3V	1mA	1mA
SS	Soft Start	6V	-0.3V	1mA	10mA
V_{CC}	Logic Section Supply	15V	-0.3V	10mA	50mA
V_C	Power Section Supply	15V	-0.3V	10mA	1.0A Peak 200mA DC
V_{REF}	Reference Voltage	6V	-0.3V	Internally Limited	10mA
PGnd	Power Ground	N/A	N/A	1.0A Peak 200mA DC	N/A
LGnd	Logic Ground	N/A	N/A	N/A	N/A

Electrical Characteristics: -40˚C < T_A < 85˚C; -40˚C < T_J < 125˚C; 3V < V_C < 15V; 4.7V < V_{CC} < 15V; Rt=12K, Ct=390pF Unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Start/Stop Voltages					
Start Threshold		4.4	4.6	4.7	V
Stop Threshold		3.2	3.8	4.1	V
Hysteresis	Start - Stop	400	850	1400	mV
I_{CC} @ Startup	V_{CC} < UVL Start Threshold		38	75	µA
■ Supply Current					
I_{CC} Operating			9.5	14	mA
I_C Operating	1nF Load on GATE		12	18	mA
I_C Operating	No switching		2	4	mA
■ Reference Voltage					
Total Accuracy	0mA < I_{REF} < 2mA	3.2	3.3	3.4	V
Line Regulation			6	20	mV
Load Regulation	0mA < I_{REF} < 2mA		6	15	mV
Noise Voltage	10Hz < F < 10kHz (Note 1)		50		µV
Op Life Shift	T = 1000Hrs. (Note 1)		4	20	mV
Fault Voltage		2.8	2.95	3.1	V
$V_{REF(OK)}$ Voltage		2.9	3.05	3.2	V
$V_{REF(OK)}$ Hysteresis		30	100	150	mV
Current Limit		2	40	100	mA
■ Error Amp					
Reference Voltage	V_{FB} = COMP	1.234	1.263	1.285	V
V_{FB} Input Current	V_{FB} = 1.2V		1.3	2	µA
Open Loop Gain	(Note 1)	60			dB
Unity Gain Bandwidth	(Note 1)	1.5			MHz
COMP Sink Current	COMP = 1.4V, V_{FB} = 1.45V	3	12	32	mA
COMP Source Current	COMP = 1.4V, V_{FB} = 1.15V	1	1.6	2.0	mA
COMP High Voltage	V_{FB} = 1.15V	2.8	3.1	3.4	V
COMP Low Voltage	V_{FB} = 1.45V	75	125	300	mV
PSRR	Freq = 120Hz (Note 1)	60	85		dB
SS Clamp, V_{COMP}	SS = 1.4V, V_{FB} = 0V, I_{SET} = 2V	1.3	1.4	1.5	V
COMP Max Clamp	Note 1	1.7	1.8	1.9	V

Electrical Characteristics: -40˚C < T_A < 85˚C; -40˚C < T_J < 125˚C; 3V < V_C < 15V; 4.7V < V_{CC} < 15V; Rt=12K, Ct=390pF Unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Oscillator					
Frequency Accuracy		260	273	320	kHz
Voltage Stability			1	2	%
Temperature Stability	(Note 1) -40˚C < T_J < 125˚C		8		%
Max Frequency	(Note 1)	1			MHz
Duty Cycle		80	85	90	%
Peak Voltage	(Note 1)	1.94	2.00	2.06	V
Valley Clamp Voltage		0.90	0.95	1.00	V
Valley Voltage	(Note 1)	0.85	1.00	1.15	V
Discharge Current		0.85	1.00	1.15	mA
■ Synchronization					
Input Threshold		0.9	1.4	1.8	V
Output Pulse Width		200	320	450	ns
Output High Voltage	100μA Load	2.1	2.5	2.8	V
Input Resistance		35	70	140	kΩ
SYNC to Drive Delay	Time from SYNC to GATE Shutdown	100	140	180	ns
Output Drive Current	R_{SYNC} = 1Ω	1.00	1.50	2.25	mA
■ GATE Driver					
High Saturation Voltage	V_C-GATE, V_C = 10V, I_{SOURCE} = 200mA		1.5	2.0	V
Low Saturation Voltage	GATE-PGnd, I_{SINK} = 200mA		1.2	1.5	V
High Voltage Clamp		11.0	13.5	16.0	V
Output Current	1 nF load (Note 1)		1	1.25	A
Output UVL Leakage	GATE = 0V		1	50	μA
Rise Time	1nF load, V_C = 20V, 1V < GATE < 9V		60	100	ns
Fall Time	1nF load, V_C = 20V, 9V < GATE < 1V		25	50	ns
Max Gate Voltage during UVL/Sleep	I_{GATE} = 500μA	.4	.7	1.0	V
■ FeedForward (FF)					
Discharge Voltage	I_{FF} = 2mA		0.3	0.7	V
Discharge Current	FF = 1V	2	16	30	mA
FF to GATE Delay		50	75	125	ns

Electrical Characteristics: -40˚C < T_A < 85˚C; -40˚C < T_J < 125˚C; 3V < V_C < 15V; 4.7V < V_{CC} < 15V; Rt=12K, Ct=390pF Unless otherwise stated.

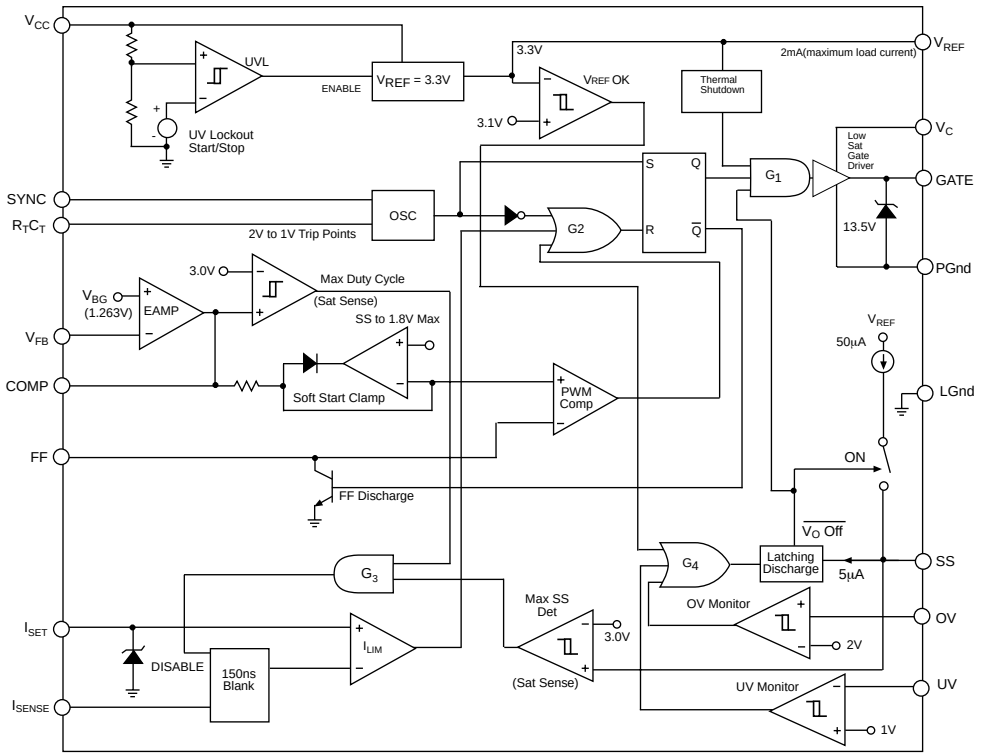
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Overcurrent Protection					
Overcurrent Threshold	I_{SET} = 0.5V, Ramp I_{SENSE}	0.475	0.500	0.525	V
I_{SENSE} to GATE Delay		50	90	125	ns
■ External Voltage Monitors					
Overvoltage Threshold	OV increasing	1.9	2.0	2.1	V
Overvoltage Hysteresis Current	OV = 2.15V	10.0	12.5	15.0	µA
Undervoltage Threshold	UV increasing	0.95	1.00	1.05	V
Undervoltage Hysteresis		25	75	125	mV
■ Soft Start (SS)					
Charge Current	SS = 2V	40	50	70	µA
Discharge Current	SS = 2V	4	5	7	µA
Charge Voltage		2.8	3.0	3.4	V
Discharge Voltage		0.25	0.3	0.35	V
Soft Start Clamp Offset	FF = 1.25V	1.15	1.25	1.35	V
Soft Start Fault Voltage	OV = 2.15V or LV = 0.85V		0.1	0.2	V
■ Blanking					
Blanking Time		50	150	250	ns
SS Blanking Disable Threshold	V_{FB} < 1	2.8	3.0	3.3	V
COMP Blanking Disable Threshold	V_{FB} < 1, SS > 3V	2.8	3.0	3.3	V
■ Thermal Shutdown					
Thermal Shutdown	(Note 1)	125	150	180	˚C
Thermal Hysteresis	(Note 1)	5	10	15	˚C

Note 1: Guaranteed by design, not 100% tested in production.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
16L PDIP & 16L SO Narrow		
1	GATE	External power switch driver with 1.0A peak capability. Rail to rail output occurs when the capacitive load is between 470pF and 10nF.
2	I_{SENSE}	Current sense comparator input.
3	SYNC	Bidirectional synchronization. Locks to highest frequency.
4	FF	PWM ramp.
5	UV	Undervoltage protection monitor.
6	OV	Overvoltage protection monitor.
7	R_T/C_T	Timing resistor R_T and capacitor C_T determine oscillator frequency and maximum duty cycle, D_{MAX}.
8	I_{SET}	Voltage at this pin sets pulse-by-pulse overcurrent threshold.
9	V_{FB}	Feedback voltage input. Connected to the error amplifier inverting input.
10	COMP	Error amplifier output.
11	SS	Charging external capacitor restricts error amplifier output voltage during the power up or fault conditions.
12	LGnd	Logic Ground.
13	V_{REF}	3.3V reference voltage output. Decoupling capacitor can be selected from 0.01μF to 10μF.
14	V_{CC}	Logic supply voltage.
15	PGnd	Output power stage ground.
16	V_C	Output power stage supply voltage.

Block Diagram



Theory of Operation

Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal has fixed rising and falling slope. The feedback signal is derived solely from the output voltage. Consequently, voltage mode control has inferior line regulation and audio susceptibility.

Feed forward voltage mode control derives the ramp signal from the input line, as shown in Fig.1. Therefore, the ramp of the slope varies with the input voltage. At the start of each switch cycle, the capacitor connected to the FF pin is charged through a resistor connected to the input voltage. Meanwhile, the Gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output V_{COMP}, the PWM comparator turns off the Gate, which in turn opens the external switch. Simultaneously, the FF capacitor is quickly discharged to 0.3V.

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. As illustrated in Fig. 2, with a fixed input voltage the output voltage is regulated solely by the error amplifier. For example, an elevated output voltage reduces V_{COMP} which in turn causes duty cycle to decrease. However, if the input voltage varies, the slope of the ramp signal will react immediately which provides a much improved line transient response. As an example shown in Fig.3, when the input voltage goes up, the rising edge of the ramp signal increases which reduces duty cycle to counteract the change.

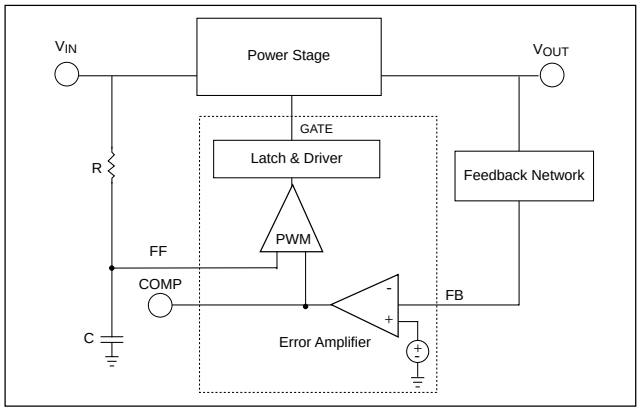


Figure 1: Feed Forward Voltage Mode Control.

The feed forward feature can also be employed to provide a volt-second clamp, which limits the maximum product of input voltage and turn on time. This clamp is used in circuits, such as Forward and Flyback converter, to prevent the transformer from saturating. Calculations used in the design of the volt-second clamp are presented in the Design Guidelines section.

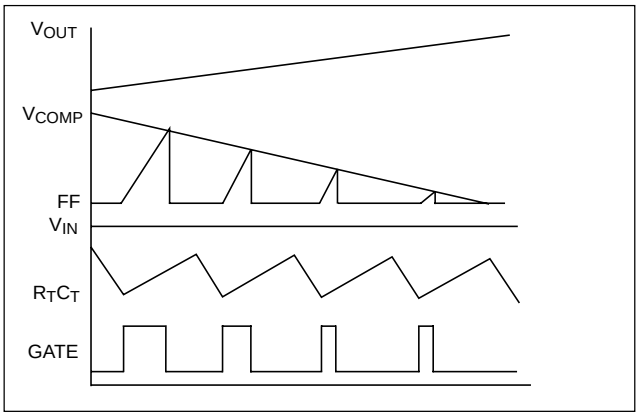


Figure 2: Pulse Width Modulated by Output Current with Constant Input Voltage.

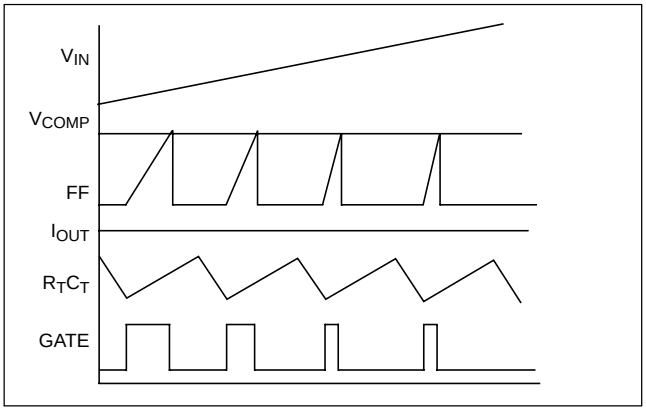


Figure 3: Pulse Width modulated by Input Voltage with constant Output Current.

Powering the IC & UVL

The Under Voltage Lockout (UVL) comparator has two voltage references; the start and stop thresholds. During power-up, the UVL comparator disables V_{REF} (which in-turn disables the entire IC) until the controller reaches its V_{CC} start threshold. During power-down, the UVL comparator allows the controller to operate until the V_{CC} stop threshold is reached. The CS51221 requires only 50μA during startup. The output stage is held at a low impedance state in lock out mode.

During power up and fault conditions, the soft-start clamps the Comp pin voltage and limits the duty cycle. The power up transition tends to generate temporary duty cycles much greater than the steady state value due to the low output voltage. Consequently, excessive current stresses often take place in the system. Soft Start technique alleviates this problem by gradually releasing the clamp on the duty cycle to eliminate the in-rush current. The duration of the Soft Start can be programmed through a capacitance connected to the SS pin. The constant charging current to the SS pin is 50μA (typ).

Application Information: continued

The V_{REF} (ok) comparator monitors the 3.3V V_{REF} output and latches a fault condition if V_{REF} falls below 3.1V. The fault condition may also be triggered when the OV pin voltage rises above 2V or the UV pin voltage falls below 1V. The under-voltage comparator has a built-in hysteresis of 75mV (typ). The hysteresis for the OV comparator is programmable through a resistor connected to the OV pin. When an OV condition is detected, the over-voltage hysteresis current of 12.5μA (typ) is sourced from the pin.

In Fig.4, the fault condition is triggered by pulling the UV pin to the ground. Immediately, the SS capacitor is discharged with 5μA of current (typ) and the GATE output is disabled until the SS voltage reaches the discharge voltage of 0.3V (typ). The IC starts the Soft Start transition again if the fault condition has recovered as shown in Fig.4. However, if the fault condition persists, the SS voltage will stay at 0.10V until the removal of the fault condition.

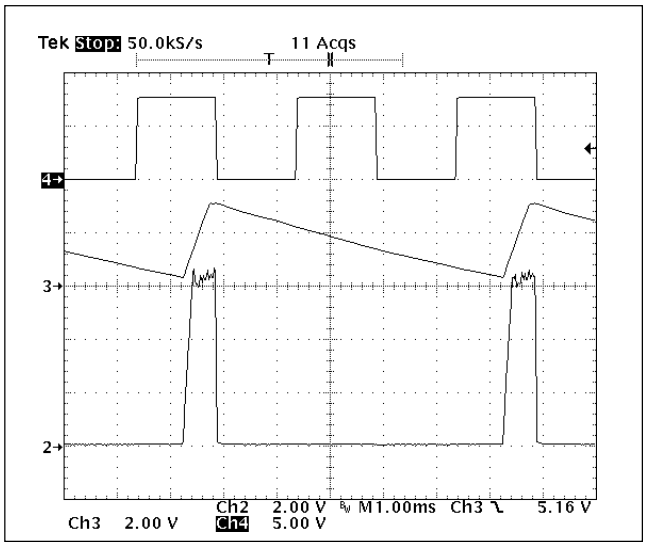


Figure 4: The fault condition is triggered when the UV pin voltage falls below 1V. The Soft Start capacitor is discharged and the GATE output is disabled. CH2: Envelop of GATE output, CH3: SS pin with 0.01µF capacitor, CH4: UV pin.

Current Sense and Over Current Protection

The current can be monitored by the I_{SENSE} pin to achieve pulse by pulse current limit. Various techniques, such as a using current sense resistor or current transformer, can be adopted to derive current signals. The voltage of the I_{SET} pin sets the threshold for maximum current. As shown in Fig. 5, when the I_{SENSE} pin voltage exceeds the I_{SET} voltage, the current limit comparator will reset the GATE latch flip-flop to terminate the GATE pulse.

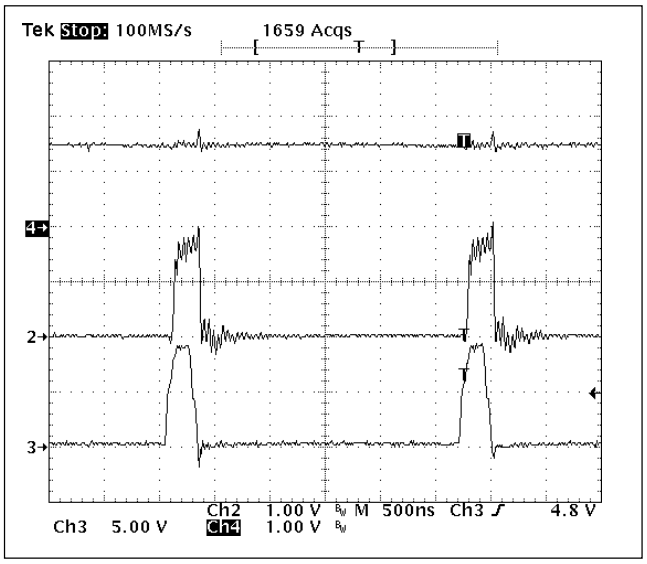


Figure 5: The GATE output is terminated when the I_{SENSE} pin voltage reaches the threshold set by the I_{SET} pin. CH2: I_{SENSE} pin, CH4: I_{SET}pin, CH3: GATE pin

The current sense signal is prone to leading edge spikes caused by the switching transition. A RC low-pass filter is usually applied to the current signals to avoid premature triggering. However, the low pass filter will inevitably change the shape of the current pulse and also add cost. The CS51221uses leading edge blanking circuitry that blocks out the first 150ns (typ) of each current pulse. This removes the leading edge spikes without altering the current waveform. The blanking is disabled during Soft Start and when the V_{COMP} is saturated high so that the minimum on-time of the controller does not have the additional blanking period. The max SS detect comparator keeps the blanking function disabled until SS charges fully. The output of the max Duty Cycle detector goes high when the error amplifier output gets saturated high, indicating that the output voltage has fallen well below its regulation point and the power supply may be under load stress.

Oscillator and Synchronization

The switching frequency is programmable through a RC network connected to the R_TC_T Pin. As shown in Fig.6, when the R_TC_T pin reaches 2V, the capacitor is discharged by a 1mA current source and the Gate signal is disabled. When the R_TC_T pin decreases to 1V, the Gate output is turned on and the discharge current is removed to let the R_TC_T pin ramp up. This begins a new switching cycle. The C_T charging time over the switch period sets the maximum duty cycle clamp which is programmable through the R_T value as shown in the Design Guidelines. At the beginning of each switching cycle, the SYNC pin generates a 2.5V, 320nS (typ) pulse. This pulse can be utilized to synchronize other power supplies.

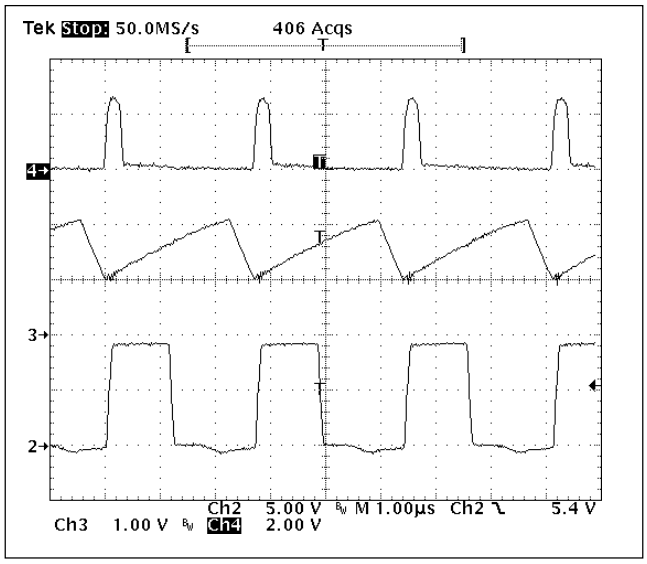


Figure 6: The Sync pin generates a sync pulse at the beginning of each switching cycle. CH2: GATE Pin, CH3: R_TC_T, CH4: SYNC pin.

The bi-directional SYNC pin can also receive an external sync signal of a greater frequency. As show in Fig.7, when the SYNC pin is triggered by an incoming signal, the IC immediately discharges C_T. The GATE signal is turned on once the R_TC_T pin reaches the valley voltage. Because of the steep falling edge, this valley voltage falls below the regular 1V threshold. However, the R_TC_T pin voltage is then quickly raised by a clamp. When the R_TC_T pin reaches the 0.95V(typ) Valley Clamp Voltage, the clamp is disconnected after a brief delay and C_T is charged through R_T.

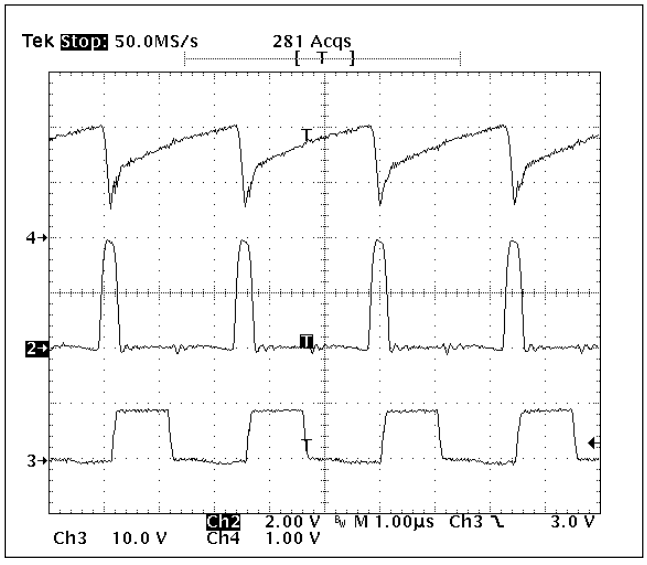


Figure 7: Operation with external sync. CH 2: SYNC pin, CH3: Gate pin, G4: R_TC_T pin.

Design Guidelines

Switch Frequency and Maximum Duty Cycle Calculations

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal sets the Gate output to the low state, thus providing a user selectable maximum duty cycle clamp. Charge and discharge times are determined by following general formulas;

$$t_C = R_TC_T\ln\left(\frac{(V_{REF} - V_{VALLEY})}{(V_{REF} - V_{PEAK})}\right)$$

$$t_d = R_TC_T\ln\left(\frac{(V_{REF} - V_{PEAK} - I_dR_T)}{(V_{REF} - V_{VALLEY} - I_dR_T)}\right),$$

where

t_C = charging time;

t_d = discharging time;

V_{VALLEY} = valley voltage of the oscillator;

V_{PEAK} = peak voltage of the oscillator.

Substituting in typical values for the parameters in the above formulas:

$V_{REF} = 3.3V$, $V_{VALLEY} = 1V$, $V_{PEAK} = 2V$, $I_d = 1mA$

$$t_C = 0.57R_TC_T$$

$$t_d = R_TC_T\ln\left(\frac{1.3 - 0.001R_T}{2.3 - 0.001R_T}\right)$$

$$D_{max} = \frac{0.57}{0.57 + \ln\left(\frac{1.3 - 0.001R_T}{2.3 - 0.001R_T}\right)}$$

It is noticed from the equation that for the oscillator to function properly, R_T has to be greater than 2.3k.

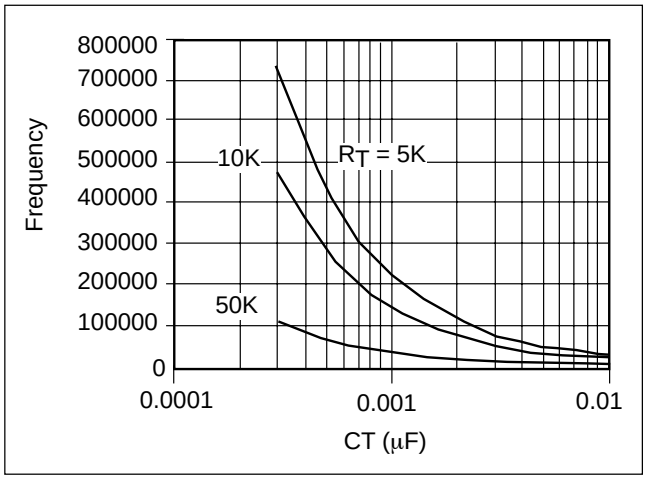


Figure 8: Typical Performance Characteristics: Oscillator frequency vs C_T

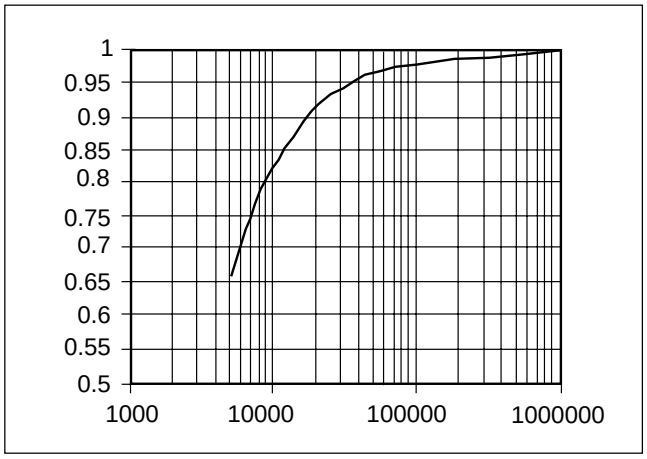


Figure 9: Typical Performance Characteristics: Oscillator duty cycle vs R_T

Select RC for Feed Forward Ramp

If the line voltage is much greater than the FF pin Peak Voltage, the charge current can be treated as a constant and is equal to V_{IN}/R. Therefore, the volt-second value is determined by:

$$V_{IN} \times T_{ON} = (V_{COMP} - V_{FF(d)}) \times R \times C$$

where V_{COMP} = COMP pin voltage
$V_{FF(d)}$ = FF pin discharge voltage.

As shown in the equation, the volt-second clamp is set by the V_{COMP} clamp voltage which is equal to 1.8V. In Forward or Flyback circuits, the volt-second clamp value is designed to prevent transformers from saturation.

In a buck or forward converter, volt-second is equal to

$$V_{IN} \times T_{ON} \approx \left(\frac{V_{OUT} \times T_S}{n} \right)$$

n = transformer turns ratio

which is a constant determined by the regulated output voltage, switching period and transformer turns ration (use 1 for buck converter). It is interesting to notice from the aforementioned two equations that during steady state, V_{COMP} doesn't change for input voltage variations. This intuitively explains why FF voltage mode control has superior line regulation and line transient response. Knowing the nominal value of V_{IN} and T_{ON}, one can also select the value of RC to place V_{COMP} at the center of its dynamic range.

Select Feedback Voltage Divider

As shown in Fig.10, the voltage divider output feeds to the FB pin, which connects to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a 1.27V (typ) reference voltage. The FB pin has an input current which has to be considered for accurate DC outputs. The following equation can be used to calculate the R1 and R2 value

$$\left(\frac{R2}{R1 + R2} \right) V_{OUT} = 1.27 - \nabla$$

where ∇ is the correction factor due to the existence of the FB pin input current Ier.

$\nabla = (Ri + R1//R2)Ier$

Ri = DC resistance between the FB pin and the voltage divider output.

Ier = V_{FB} input current, 1.3μA typical.

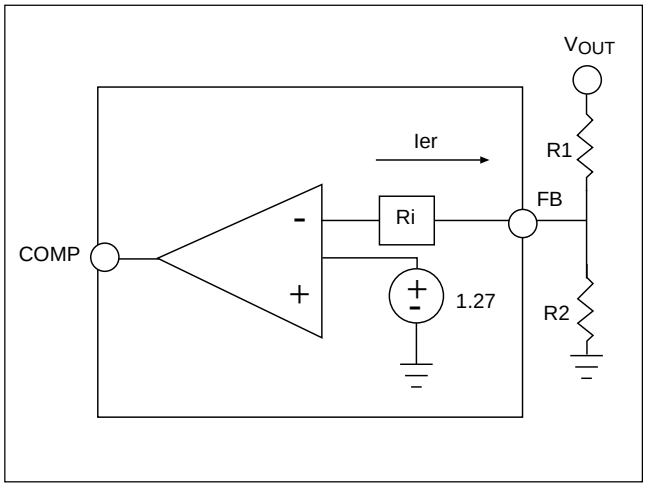


Figure 10. The design of feedback voltage divider has to consider the error amplifier input current.

Design voltage dividers for OV and UV detection

In Fig.11, the voltage divider uses three resistors in series to set OV and UV threshold seen from the input voltage. The values of the resistors can be calculated from the following three equations, where the third equation is derived from OV hysteresis requirement.

$$V_{IN(LOW)} \times \left(\frac{R2 + R3}{R2 + R3 + R1} \right) = 1V \qquad (A)$$

$$V_{IN(HIGH)} \times \left(\frac{R3}{R2 + R3 + R1} \right) = 2V \qquad (B)$$

$$12.5\mu A \times (R1 + R2) = V_{HYST} \qquad (C)$$

where

$V_{LINE(LOW)}$, $V_{LINE(HIGH)}$ = input voltage OV and UV threshold

V_{HYST} = OV hysteresis seen at V_{IN}

It is self-evident from equation A and B that to use this design, $V_{IN(HIGH)}$ has to be two times greater than $V_{IN(LOW)}$. Otherwise, two voltage dividers have to be used to program OV and UV separately.

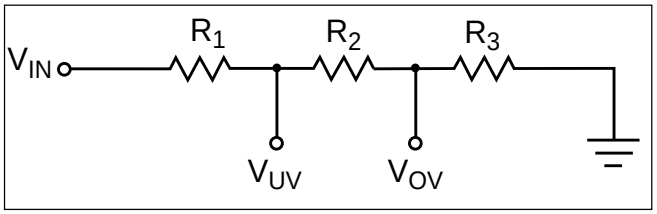


Figure 11. OV/UV Monitor Divider.

Package Specification

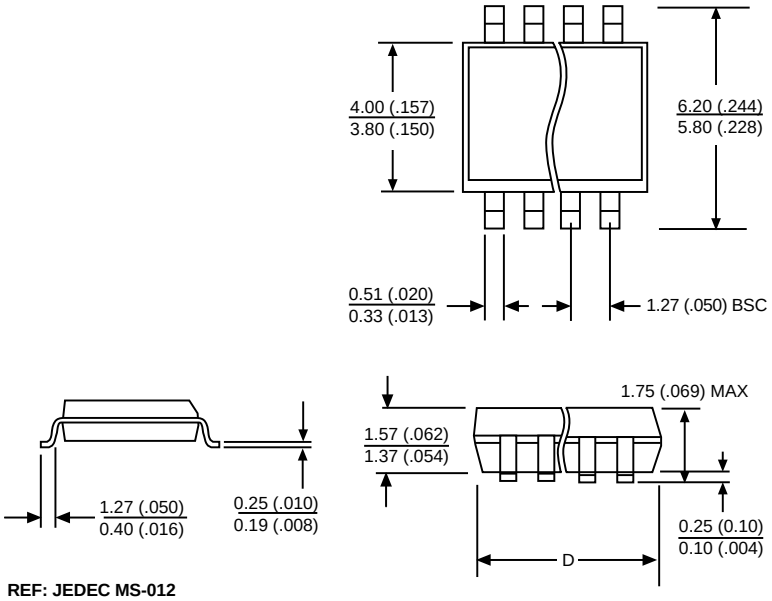
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L SO Narrow	10.00	9.80	.394	.386
16L PDIP	19.69	18.67	.775	.735

PACKAGE THERMAL DATA

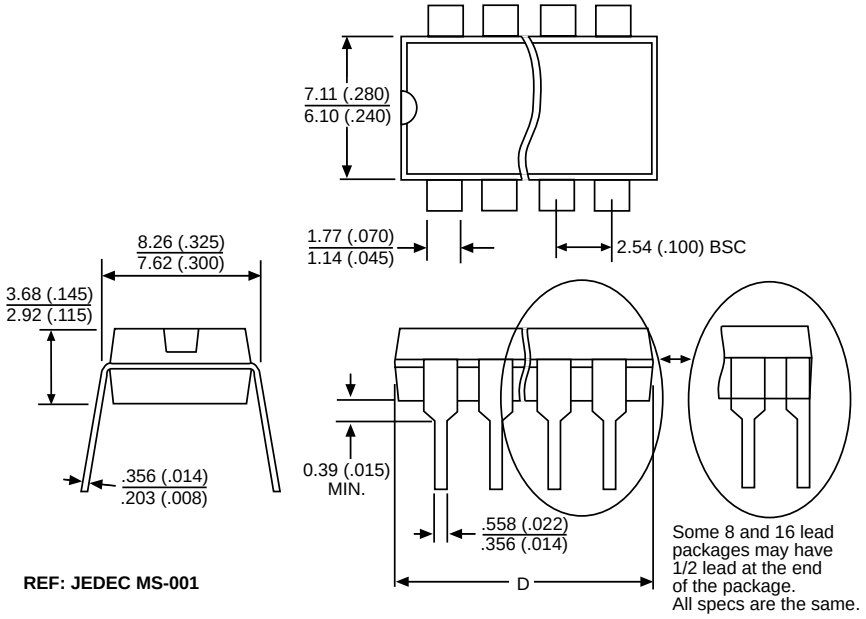
Thermal Data		16L SO Narrow	16L PDIP	
$R_{\Theta JC}$	typ	28	42	°C/W
$R_{\Theta JA}$	typ	115	80	°C/W

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

Plastic DIP (N); 300 mil wide



REF: JEDEC MS-001

Ordering Information

Part Number	Description
CS51221ED16	16L SO Narrow
CS51221EDR16	16L SO Narrow *(tape & reel)*
CS51221EN16	16L PDIP

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.