CS42L50

Low Voltage, Stereo CODEC with Headphone Amp

Features

- 28-Pin CASON package
- 1.8 to 3.3 Volt supply
- 24-Bit conversion / 96 kHz sample rate
- 96 dB ADC/DAC dynamic range at 3 V supply
- -88/-85 dB ADC/DAC THD+N
- 19 mW playback power consumption @ 1.8 V
- Microphone or Line input amplifier with up to 32dB of gain
- 2:1 stereo mux
- Digital volume control on inputs and outputs
  – 96 dB attenuation, 1 dB step size
- Digital bass and treble boost on outputs
  – Selectable corner frequencies
- Dynamic range compression and limiting
- De-emphasis for 32 kHz, 44.1 kHz, and 48 kHz
- Headphone amplifier
  – 26 mW power output into 16 W load @ 3.0V supply
  – -80 dB THD+N
  – 34 dB analog attenuation and mute
- ATAPI mixing functions

Description

The CS42L50 is a highly integrated, 24-bit, 96 kHz audio codec.

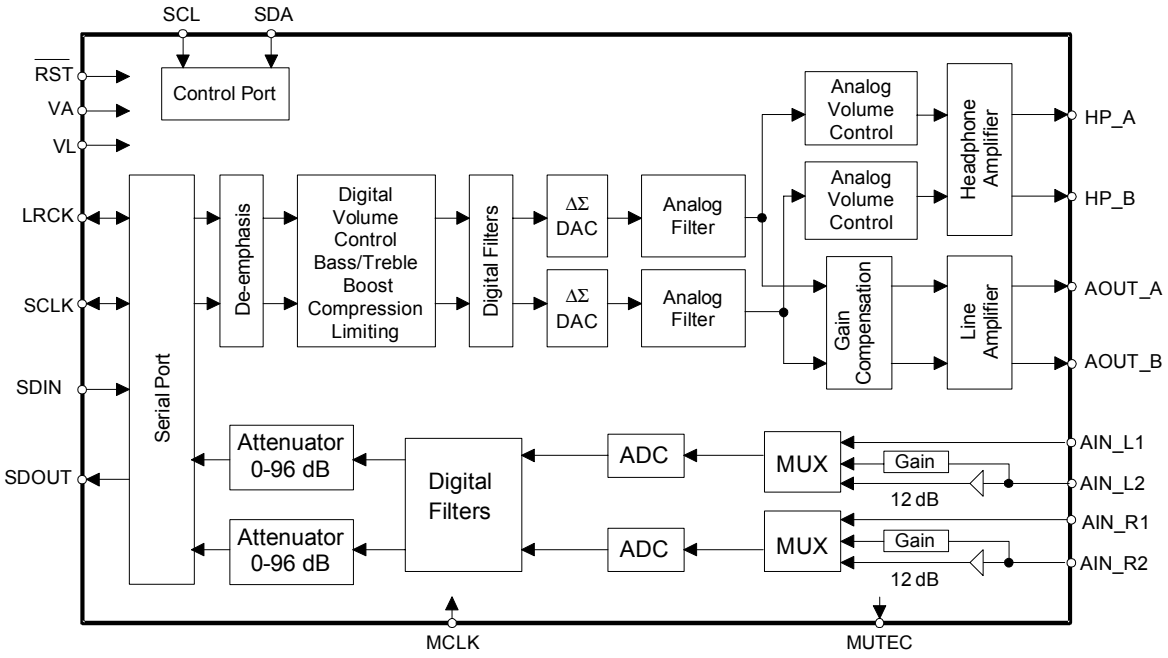
This device is based on delta-sigma modulation allowing infinite adjustment of the sample rate between 8 kHz and 100 kHz simply by changing the master clock frequency.

The CS42L50 contains a 2:1 stereo mux, programmable analog gain control, and digital attenuation on the analog inputs. The output D/A converters include digital bass and treble boost, dynamic range compression, limiting, mixing, volume control and de-emphasis.

The CS42L50 operates from a +1.8 V to +3.3 V supply. These features are ideal for portable MP3 and MD recorders, CD and DVD recorders, digital camcorders, and other portable systems that require extremely low power consumption in a minimal amount of space.

ORDERING INFORMATION

CS42L50-KN	28-pin CASON, -10 to 70 °C
CDB42L50	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Parameter	Symbol	Single Speed Mode			Double Speed Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics for VA = 1.8 V								
Dynamic Range A-weighted		TBD	93	-	TBD	94	-	dB
unweighted		TBD	90	-	TBD	91	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit -1 dB		-	-88	TBD	-	-88	TBD	dB
-20 dB		-	-70	-	-	-71	-	dB
-60 dB		-	-30	-	-	-31	-	dB
16-Bit -1 dB		-	-86	-	-	-86	-	dB
-20 dB		-	-68	-	-	-68	-	dB
-60 dB		-	-28	-	-	-28	-	dB
Dynamic Range (PGA on)*								
0 dB Gain A-weighted		-	90	-	-	89	-	dB
unweighted		-	87	-	-	86	-	dB
12 dB Gain A-weighted		-	85	-	-	86	-	dB
unweighted		-	82	-	-	83	-	dB
Total Harmonic Distortion + Noise (PGA on)*	THD+N							
(Note 1) 0 dB Gain, 18 to 24-Bit -1 dB		-	85	-	-	84	-	dB
12 dB Gain, 18 to 24-Bit -1 dB		-	83	-	-	82	-	dB
Analog Input Characteristics for VA = 3.0 V								
Dynamic Range A-weighted		TBD	96	-	TBD	98	-	dB
unweighted		TBD	93	-	TBD	95	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit -1 dB		-	-88	TBD	-	-85	TBD	dB
-20 dB		-	-73	-	-	-75	-	dB
-60 dB		-	-33	-	-	-35	-	dB
16-Bit -1 dB		-	-86	-	-	-83	-	dB
-20 dB		-	-68	-	-	-65	-	dB
-60 dB		-	-28	-	-	-28	-	dB
Dynamic Range (PGA on)*								
0 dB Gain A-weighted		-	93	-	-	92	-	dB
unweighted		-	90	-	-	89	-	dB
12 dB Gain A-weighted		-	88	-	-	89	-	dB
unweighted		-	85	-	-	86	-	dB
Total Harmonic Distortion + Noise (PGA on)*	THD+N							
(Note 1) 0 dB Gain, 18 to 24-Bit -1 dB		-	78	-	-	77	-	dB
12 dB Gain, 18 to 24-Bit -1 dB		-	73	-	-	76	-	dB

*PGA : Programmable Gain Amplifier

Parameter	Symbol	Single Speed Mode			Double Speed Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics for VA = 1.8 - 3.3V								
Interchannel Isolation 1 kHz		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error (with HPF Active)		-	-	0	-	-	0	LSB
Full Scale Input Voltage		TBD	VA/3.6	TBD	TBD	VA/3.6	TBD	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
Programmable Gain Characteristics								
Gain Step Size		-	1.0	-	-	1.0	-	dB
Absolute Gain Step Error		-	-	TBD	-	-	TBD	dB
A/D Decimation Filter Characteristics **(Note 2)**								
Passband (Note 3)		0	-	23.5	0	-	47.5	kHz
Passband Ripple		-0.08	-	+0.17	-0.09	-	0	dB
Stopband (Note 3)		27.5	-	-	64.1	-	-	kHz
Stopband Attenuation (Note 4)		-60.3	-	-	-48.4	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 5)	t_{gd}	-	10/Fs	-	-	2.7/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.03	-	-	0.007	µs
High Pass Filter Characteristics								
Frequency Response -3 dB (Note 2)		-	3.7	-	-	3.7	-	Hz
-0.1 dB		-	24.2	-	-	24.2	-	Hz
Phase Deviation @ 20 Hz (Note 2)		-	10	-	-	10	-	Degree
Passband Ripple (Note 2)		-	-	0.17	-	-	0.09	dB

*PGA : Programmable Gain Amplifier

ANALOG OUTPUT CHARACTERISTICS

(T_A = 25° C; Logic "1" = VL = 1.8 V; Logic "0" = GND = 0 V; Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for Single Speed Mode = 48 kHz, SCLK = 3.072 MHz. Fs for Double Speed Mode = 96 kHz, SCLK = 6.144 MHz. Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 23) for line out, R_L = 16 Ω, C_L = 10 pF (see Figure 24) for headphone out.

Parameter			Symbol	Single Speed Mode Min	Typ	Max	Double Speed Mode Min	Typ	Max	Unit
Line Output Dynamic Performance for VA = 1.8 V										
Dynamic Range		(Note 6)								
	18 to 24-Bit	unweighted		TBD	91	-	TBD	89	-	dB
		A-Weighted		TBD	94	-	TBD	92	-	dB
	16-Bit	unweighted		-	89	-	-	87	-	dB
		A-Weighted		-	92	-	-	90	-	dB
Total Harmonic Distortion + Noise		(Note 6)	THD+N							
	18 to 24-Bit	0 dB		-	-80	TBD	-	-80	TBD	dB
		-20 dB		-	-71	-	-	-69	-	dB
		-60 dB		-	-31	-	-	-29	-	dB
	16-Bit	0 dB		-	-78	-	-	-78	-	dB
		-20 dB		-	-69	-	-	-67	-	dB
		-60 dB		-	-29	-	-	-27	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	-	100	-	dB
Headphone Output Dynamic Performance for VA = VA_HP = 1.8 V										
Dynamic Range		(Note 6)								
	18 to 24-Bit	unweighted		TBD	88	-	TBD	88	-	dB
		A-Weighted		TBD	91	-	TBD	91	-	dB
	16-Bit	unweighted		-	86	-	-	86	-	dB
		A-Weighted		-	89	-	-	89	-	dB
Total Harmonic Distortion + Noise		(Note 6)	THD+N							
	18 to 24-Bit	0 dB		-	-82	TBD	-	-85	TBD	dB
		-20 dB		-	-68	-	-	-68	-	dB
		-60 dB		-	-28	-	-	-28	-	dB
	16-Bit	0 dB		-	-80	-	-	-83	-	dB
		-20 dB		-	-66	-	-	-66	-	dB
		-60 dB		-	-26	-	-	-26	-	dB
Interchannel Isolation		(1 kHz)		-	66	-	-	66	-	dB

Notes:
1. Referenced to typical full-scale input voltage.
2. Filter response is not tested but is guaranteed by design.
3. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
4. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
5. Group delay for Fs = 48 kHz, t_{gd} = 10/48 kHz = 208 µs.
6. One-half LSB of triangular PDF dither is added to data.

ANALOG OUTPUT CHARACTERISTICS (Continued)

Parameter			Symbol	Single Speed Mode Min	Typ	Max	Double Speed Mode Min	Typ	Max	Unit
Line Output Dynamic Performance for VA = 3.0 V										
Dynamic Range		(Note 6)								
	18 to 24-Bit	unweighted		TBD	93	-	TBD	93	-	dB
		A-Weighted		TBD	96	-	TBD	96	-	dB
	16-Bit	unweighted		-	91	-	-	91	-	dB
		A-Weighted		-	94	-	-	94	-	dB
Total Harmonic Distortion + Noise		(Note 6)	THD+N							
	18 to 24 Bit	0dB		-	-85	TBD	-	-85	TBD	dB
		-20dB		-	-73	-	-	-73	-	dB
		-60dB		-	-33	-	-	-33	-	dB
	16-Bit	0dB		-	-83	-	-	-83	-	dB
		-20dB		-	-71	-	-	-71	-	dB
		-60dB		-	-31	-	-	-31	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	-	100	-	dB
Headphone Output Dynamic Performance for VA = VA_HP = 3.0 V										
Dynamic Range		(Note 6)								
	18 to 24-Bit	unweighted		TBD	90	-	TBD	90	-	dB
		A-Weighted		TBD	93	-	TBD	93	-	dB
	16-Bit	unweighted		-	88	-	-	88	-	dB
		A-Weighted		-	91	-	-	91	-	dB
Total Harmonic Distortion + Noise		(Note 6)	THD+N							
	18 to 24 Bit	0dB		-	-76	TBD	-	-73	TBD	dB
		-20dB		-	-70	-	-	-70	-	dB
		-60dB		-	-30	-	-	-30	-	dB
	16-Bit	0dB		-	-74	-	-	-71	-	dB
		-20dB		-	-68	-	-	-68	-	dB
		-60dB		-	-28	-	-	-28	-	dB
Interchannel Isolation		(1 kHz)		-	66	-	-	66	-	dB

ANALOG OUTPUT CHARACTERISTICS (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Analog Output						
Full Scale Line Output Voltage	(Note 7)	V_{FS_LINE}	TBD	G x VA	TBD	Vpp
Line Output Quiescent Voltage		V_{Q_LINE}	-	0.5 x VA_LINE	-	VDC
Full Scale Headphone Output Voltage		V_{FS_HP}	TBD	0.55 x VA	TBD	Vpp
Headphone Output Quiescent Voltage		V_{Q_HP}	-	0.5 x VA_HP	-	VDC
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Drift			-	100	-	ppm/°C
Maximum Line Output AC-Current	VA=1.8 V	I_{LINE}	-	0.1	-	mA
	VA=3.0 V		-	0.15	-	mA
Maximum Headphone Output AC-Current	VA=VA_HP=1.8 V	I_{HP}	-	31	-	mA
	VA=VA_HP=3.0 V		-	52	-	mA

Parameter		Symbol	Single Speed Mode Min	Typ	Max	Double Speed Mode Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response (Note 8)									
Passband	(Note 9)								
	to -0.05 dB corner		0	-	.4535	-	-	-	Fs
	to -0.1 dB corner		-	-	-	0	-	.4426	Fs
	to -3 dB corner		0	-	.4998	0	-	.4984	Fs
Frequency Response 10 Hz to 20 kHz	(Note 10)		-.02	-	+.08	0	-	+0.11	dB
StopBand			.5465	-	-	.577	-	-	Fs
StopBand Attenuation	(Note 11)		50	-	-	55	-	-	dB
Group Delay		tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation	0 - 40 kHz		-	-	-	-	±1.39/Fs	-	s
	0 - 20 kHz		-	±0.36/Fs	-	-	±0.23/Fs	-	s
De-emphasis Error	Fs = 32 kHz		-	-	+.2/-.1				dB
(Relative to 1 kHz)	Fs = 44.1 kHz		-	-	+.05/-.14		(Note 12)		dB
	Fs = 48 kHz		-	-	+0/-.22				dB

Notes:
7. See Section 4.2.7 for details.
8. Filter response is not tested but is guaranteed by design.
9. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 14 through 21) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Referenced to a 1 kHz, full-scale sine wave.
11. For Single Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
12. De-emphasis is not available in Double Speed Mode.

POWER AND THERMAL CHARACTERISTICS

(GND = 0 V; All voltages with respect to ground. All measurements taken with all zeros input and open outputs, unless otherwise specified.)

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current-	VA=1.8 V	I_A	-	13.3	-	mA
Normal Operation	VA_HP=1.8 V	I_{A_HP}	-	1.5	-	mA
	VL=1.8 V	I_{D_L}	-	154	-	µA
Power Supply Current-	VA=3.0 V	I_A	-	20	-	mA
Normal Operation	VA_HP=3.0 V	I_{A_HP}	-	1.5	-	mA
	VL=3.0 V	I_{D_L}	-	270	-	µA
Power Supply Current-	All Supplies=1.8 V		-	150	-	µA
Power Down Mode (Note 13)	All Supplies =3.0V		-	350	-	µA
Total Power Dissipation-	All Supplies=1.8 V		-	27	TBD	mW
Normal Operation	All Supplies=3.0 V		-	65	TBD	mW
Maximum Headphone Power Dissipation						
(1 kHz full-scale sine wave	VA=1.8 V		-	15	-	mW
into 16 ohm load)	VA=3.0 V		-	26	-	mW
Package Thermal Resistance		θ_{JA}	-	55	-	°C/Watt
Power Supply Rejection Ratio (Note 14)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes: 13. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

14. Valid with the recommended capacitor values on FILT+_ADC, FILT+_DAC, VQ_DAC, and VQ_ADC as shown in Figure 4. Increasing the capacitance will also increase the PSRR. Note that care should be taken when selecting capacitor type, as any leakage current in excess of 1.0 µA will cause degradation in analog performance. A small ceramic capacitor in parallel with a larger electrolytic is recommended.

DIGITAL CHARACTERISTICS (T_A = 25° C; VL = 1.7 V - 3.3 V; GND = 0 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	0.7 x VL	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.3 x VL	V
Input Leakage Current		I_{in}	-	-	±10	µA
High-Level Output Voltage		V_{OH}	0.7 x VL	-	-	V
Low-Level Output Voltage		V_{OL}	-	-	0.3 x VL	V
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Capability	VA=1.8 V		-	TBD	-	mA
	VA=3.0 V		-	3	-	mA
MUTEC High-Level Output Voltage			-	VA	-	V
MUTEC Low-Level Output Voltage			-	0	-	V

ABSOLUTE MAXIMUM RATINGS (GND = 0V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supplies:	Analog&Headphone	VA&VA_HP	-0.3	4.0	V
	Digital I/O	VL	-0.3	4.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0V; all voltages with respect to ground.)

Parameters			Symbol	Min	Typ	Max	Units
Ambient Temperature			T_A	-10	-	70	°C
DC Power Supplies:	Analog&Headphone	(Note 15)	VA&VA_HP	1.7	-	3.6	V
	Digital I/O		VL	1.7	-	3.6	V

Notes: 15. VA and VA_HP should be tied to the same supply as shown in Figure 4.

SWITCHING CHARACTERISTICS (T_A = -10 to 70° C; VA = 1.7 V - 3.3 V; Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Single Speed Mode	Fs	2	-	50	kHz
	Double Speed Mode	Fs	50	-	100	kHz
MCLK Pulse Width High	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 384 or 192		25	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 384 or 192		25	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 256 or 128		35	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 256 or 128		35	-	-	ns
Master Mode						
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDOUT Valid		t_{sdo}	0	-	20	ns
SCLK Duty Cycle			40	50	60	%
Slave Mode						
LRCK Duty Cycle			40	50	60	%
Rise Time of Both LRCK and SCLK		t_r	-	-	10	ns
Fall Time of Both LRCK and SCLK		t_f	-	-	10	ns
SCLK Period (Note 16)	Single Speed Mode	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
	Double Speed Mode	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDOUT Valid	Single Speed Mode	t_{dss}	-	-	$\frac{1}{(512)Fs}$	ns
	Double Speed Mode	t_{dss}	-	-	$\frac{1}{(256)Fs}$	ns

16. There must be exactly 32, 48, 64, or 128 SCLK periods per LRCK transition.

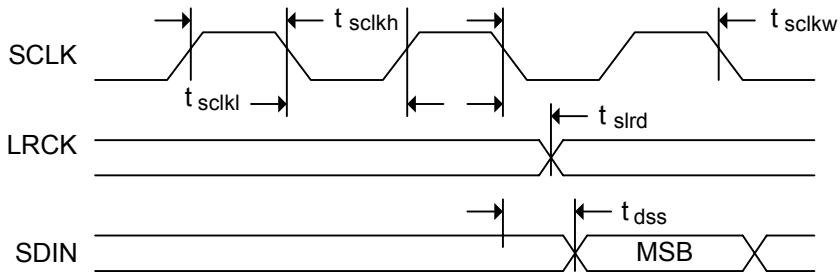


Figure 1. SCLK to LRCK and SDIN, Slave Mode

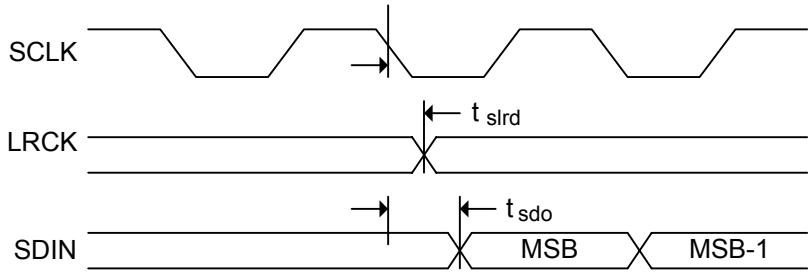


Figure 2. SCLK to LRCK and SDIN, Master Mode

SWITCHING CHARACTERISTICS - CONTROL PORT

(T_A = 25° C; VL = 1.7 V - 3.3 V; Inputs: logic 0 = GND, logic 1 = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	KHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 17)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL	t_{rc}	-	25	ns
Fall Time of SCL	t_{fc}	-	25	ns
Rise Time of SDA	t_{rd}	-	1	µs
Fall Time of SDA	t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Note: 17. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

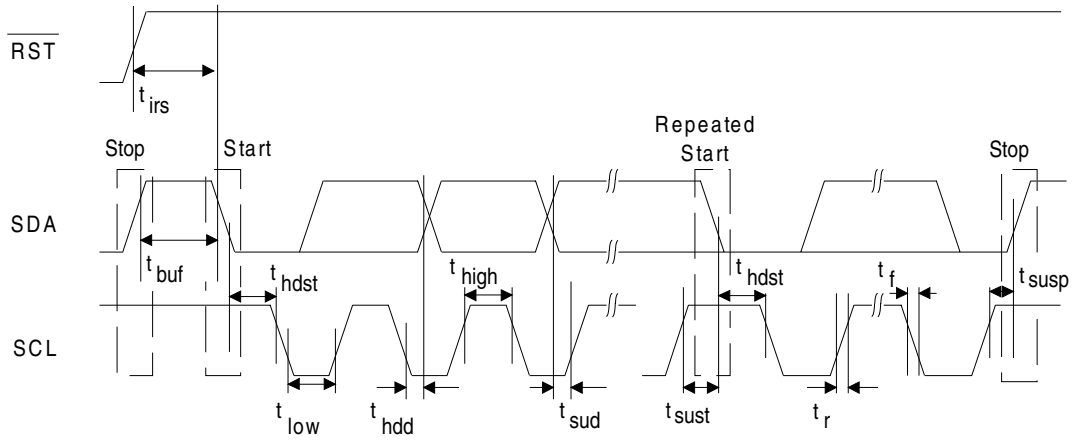


Figure 3. Control Port Timing - I²C®

2. TYPICAL CONNECTION DIAGRAM

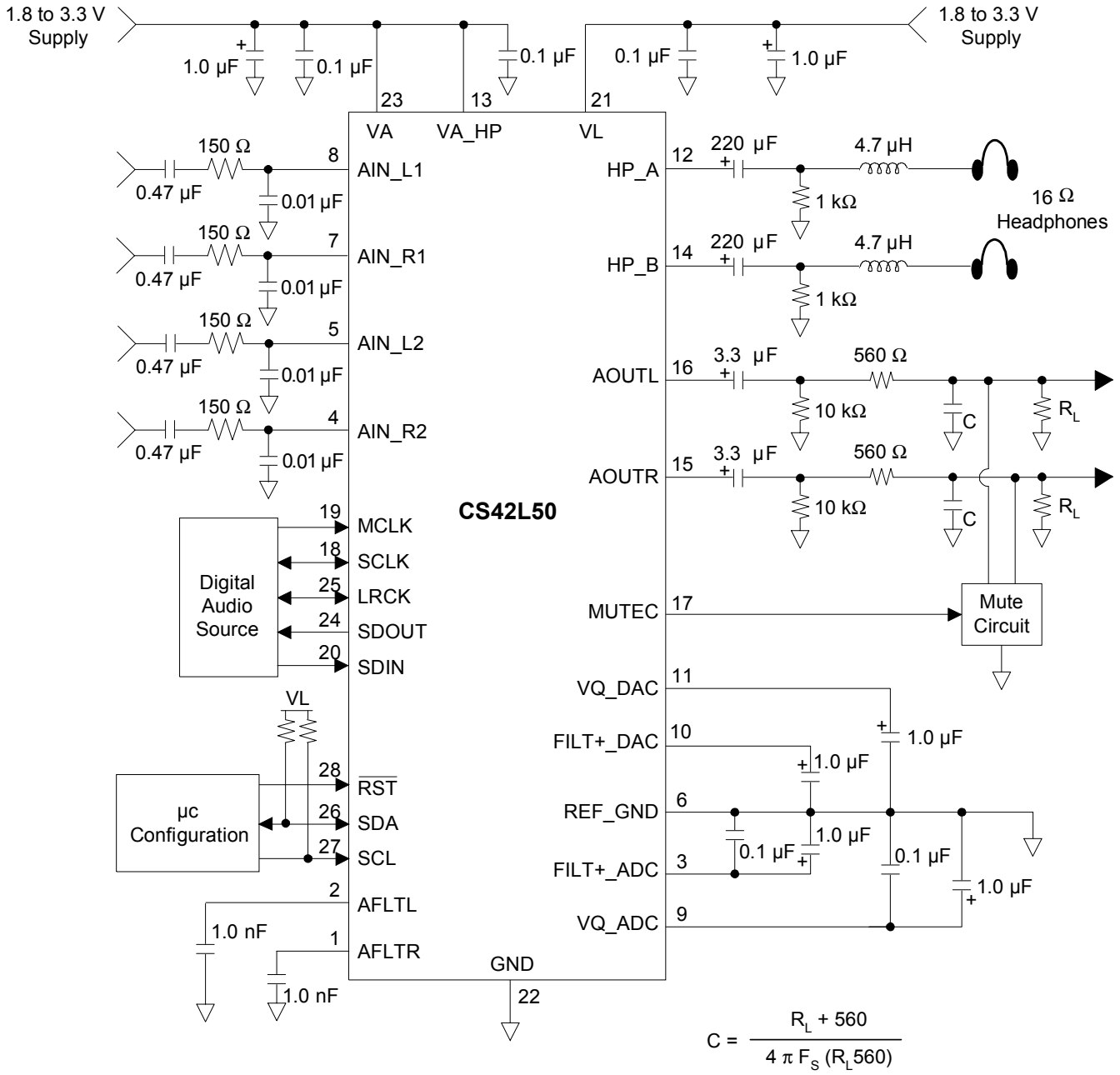


Figure 4. CS42L50 Typical Connection Diagram

3. REGISTER QUICK REFERENCE

ADC (Address = 0010000)

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	I/O and Power Control	Reserved	BOOST	AINMUX1	AINMUX0	Reserved	Reserved	PDN	CP_EN
	default	0	0	0	0	0	0	1	0
2h	Interface Control	Reserved	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0
	default	0	0	0	0	0	0	0	0
3h	Analog I/O Control	MUTEL	MUTER	SZC1	SZC0	Reserved	INDVC	L=R	HPFREEZE
	default	0	0	1	1	0	0	0	0
4h	Left Channel Digital Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
5h	Right Channel Digital Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
6h	Analog Gain Control	LVOL3	LVOL2	LVOL1	LVOL0	RVOL3	RVOL2	RVOL1	RVOL0
	default	0	0	0	0	0	0	0	0
7h	Clip Detection Status	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CLIP_L	CLIP_R
	default	0	0	0	0	0	0	0	0

DAC (Address = 0010001)

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	Power and Muting Control	AMUTE	SZC1	SZC0	Reserved	PDNHP	PDNLN	PDN	CP_EN
	default	1	1	0	1	0	0	1	0
2h	Channel A Analog Headphone Attenuation Control	HVOLA7	HVOLA6	HVOLA5	HVOLA4	HVOLA3	HVOLA2	HVOLA1	HVOLA0
	default	0	0	0	0	0	0	0	0
3h	Channel B Analog Headphone Attenuation Control	HVOLB7	HVOLB6	HVOLB5	HVOLB4	HVOLB3	HVOLB2	HVOLB1	HVOLB0
	default	0	0	0	0	0	0	0	0
4h	Channel A Digital Volume Control	DVOLA7	DVOLA6	DVOLA5	DVOLA4	DVOLA3	DVOLA2	DVOLA1	DVOLA0
	default	0	0	0	0	0	0	0	0
5h	Channel B Digital Volume Control	DVOLB7	DVOLB6	DVOLB5	DVOLB4	DVOLB3	DVOLB2	DVOLB1	DVOLB0
	default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
6h	Tone Control	BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
	default	0	0	0	0	0	0	0	0
7h	Mode Control	BBCF1	BBCF0	TBCF1	TBCF0	A=B	DEM1	DEM0	VCBYP
	default	0	0	0	0	0	0	0	0
8h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	1	0	0	0	0
9h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	1	0	0	0	0	0
Ah	Volume and Mixing Control	TC1	TC0	TC_EN	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	0	1	0	0	1
Bh	Mode Control 2	MCLKDIV	LINE1	LINE0	Reserved	Reserved	DIF2	DIF1	DIF0
	default	0	0	0	0	0	0	0	0

4. REGISTER DESCRIPTION

4.1 ADC (Address = 0010000)

4.1.1 I/O and Power Control (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN
0	0	0	0	0	0	1	0

4.1.2 20DB GAIN BOOST (BOOST)

Default = 0
0 - Disabled
1 - Enabled

Function:

Applies a 20dB digital gain to the input signal, regardless of the input path.

4.1.3 ANALOG INPUT MULTIPLEXER (AINMUX)

Default = 00
00 - Channel 1 direct to A/D
01 - Channel 2 direct to A/D
10 - Channel 2 through PGA to A/D
11 - Reserved

Function:

The analog input multiplexer selects the input channel as well as the input path associated with various gain stages.

4.1.4 POWER DOWN (PDN)

Default - 1
0 - Disabled
1 - Enabled

Function:

The entire ADC device will enter a low-power state whenever this function is activated. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained when this mode is enabled.

4.1.5 CONTROL PORT ENABLE (CP_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The ADC will enter control port mode when this bit is enabled. This bit must be set prior to writing to the control port.

4.1.6 Interface Control (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0
0	0	0	0	0	0	0	0

4.1.7 MASTER CLOCK DIVIDE (MCLKDIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

Divides ADC MCLK by two prior to all other chip circuitry.

4.1.8 MASTER CLOCK RATIO (RATIO)

Default = 00
00 - 128x
01 - 192x
10 - 256x
11 - 384x

Function:

Sets the ratio of MCLK to LRCK for the ADC.

4.1.9 MASTER MODE (MASTER)

Default = 0
0 - Slave Mode
1 - Master Mode

Function:

Configures the CS42L50 for master or slave operation.

4.1.10 DIGITAL INTERFACE FORMAT (DIF)

Default = 000
000 - I^2S, up to 24-bit data, data valid on positive edge of SCLK
001 - Left Justified, up to 24-bit data, data valid on positive edge of SCLK
010 - Reserved
011 - Right Justified, 16-bit data, data valid on positive edge of SCLK
100 - Right Justifed, 24-bit data, data valid on positive edge of SCLK
101 - Right Justified, 18-bit data, data valid on positive edge of SCLK
110 - Right Justified, 20-bit data, data valid on positive edge of SCLK
111 - Reserved

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 25 through 30. It is recommended that the ADC and the DAC are configured for the same Digital Interface Format.

4.1.11 Analog I/O Control (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SZC1	SZC0	RESERVED	INDVC	L=R	HPFREEZE
0	0	1	1	0	0	0	0

4.1.12 LEFT/RIGHT CHANNEL MUTE (MUTE)

Default = 0
0 - Disabled
1 - Enabled

Function:

Digital mute of the left and right ADC channels.

4.1.13 SOFT RAMP AND ZERO CROSS ENABLE (SOFT/ZC)

Default = 11
00 - Change volume immediately
01 - Change volume at next zero cross time
10 - Change volume in 1dB steps
11 - Change volume in 1dB steps at every zero cross time

Function:

Soft Ramp Enable :
Soft Ramp allows level changes, both muting and attenuation, to be implemented via an incremental ramp. Digital volume control is ramped from the current level to the new level at a rate of 1/8 dB per left/right clock period. Analog volume control is ramped in 1 dB steps every 8 left/right clock periods in Single Speed mode, and 1dB every 16 left/right clock periods in Double Speed mode.

Zero Cross Enable :
Zero Cross enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 512 sample periods in Single Speed mode or 1024 sample periods in Double Speed mode (approximately 10.7ms at 48kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable :
Soft Ramp and Zero Cross enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1 dB steps and be implemented on a signal zero crossing. The level change will occur after a timeout period of 512 sample periods in Single Speed mode or 1024 sample periods in Double Speed mode (approximately 10.7 ms at 48kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

4.1.14 INDEPENDENT VOLUME CONTROL ENABLE (INDVC)

Default = 0
0 - Disabled
1 - Enabled

Function:

When this function is disabled, the AIN_L and AIN_R volume levels are controlled by the Left and Right Volume Control registers and the Independent Analog Gain Control registers are ignored.
When this function is enabled, the volume levels are determined by both the Volume Control registers and the Independent Analog Gain Control registers.

4.1.15 LEFT CHANNEL VOLUME = RIGHT CHANNEL VOLUME (L=R)

Default = 0
0 - Disabled
1 - Enabled

Function:

When this function is disabled, the left channel volume is determined by the left channel volume control register and right channel volume is determined by the right channel volume control register.

When enabled, the left and right channel volumes are determined by the left channel volume control register and the right channel volume control register is ignored.

4.1.16 HIGH-PASS FILTER FREEZE (HPFREEZE)

Default = 0
0 - Frozen
1 - Enabled

Function:

The high-pass filter works by continuously subtracting a measure of the dc offset from the output of the decimation filter. If the HPFREEZE bit is taken low during normal operation, the current value of the dc offset is frozen and this dc offset will continue to be subtracted from the conversion result.

4.1.17 Volume Control: Left Channel (address 04h) & Right Channel (address 05h)

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

Default = 0 (No attenuation)

Binary Code	Decimal Value	Volume Setting
00001010	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Function:

The volume control allows the user to alter the signal level in 1 dB increments from +12 to -96 dB, when the INDVC bit is disabled. When INDVC is enabled, the volume control can be altered in 1 dB increments from 0 to -96dB. Volume settings are decoded as shown above, using a 2's complement code. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Analog I/O Control register. All volume settings less than -96dB are equivalent to muting the channel.

4.1.18 Left/Right Analog Gain (address 06h)

7	6	5	4	3	2	1	0
LVOL3	LVOL2	LVOL1	LVOL0	RVOL3	RVOL2	RVOL1	RVOL0
0	0	0	0	0	0	0	0

Default = 0 (No gain)

Binary Code	Decimal Value	Volume Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Function:

The level of the left and right analog channels can be adjusted in 1dB increments as dictated by the Soft Ramp and Zero Cross bits from 0 to +12dB when routed through the PGA via the AINMUX bits. Levels are decoded as shown above. Levels above +12dB are interpreted as +12dB.

4.1.19 Clip Detection Status (address 07h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CLIP_L	CLIP_R
0	0	0	0	0	0	0	0

Default = 0 (No clipping detected)

Function:

The Clip Flags indicate when there is an over-range condition anywhere in the CS42L50 internal signal path. These bits are “sticky”. They constantly monitor the ADC signal path and are set to 1 when an over-range condition occurs. They are reset to 0 when read.

4.2 DAC (Address = 0010001)

4.2.1 Power and Muting Control (address 01h)

7	6	5	4	3	2	1	0
AMUTE	SZC1	SZC0	POR	PDNHP	PDNLN	PDN	CP_EN
1	1	0	1	0	0	1	0

4.2.2 AUTO-MUTE (AMUTE)

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Power and Muting Control register.

4.2.3 SOFT RAMP AND ZERO CROSS CONTROL (SZC)

Default = 10
00 - Immediate Change
01 - Zero Cross Digital and Analog
10 - Ramped Digital and Analog
11 - Reserved

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross Digital and Analog

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Ramped Digital and Analog

Soft Ramp allows digital level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. Analog level changes will occur in 1 dB steps on a signal zero crossing. The analog level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Note: Ramped Digital and Analog is not available in Double Speed Mode.

4.2.4 POWER DOWN HEADPHONE AMPLIFIER (PDNHP)

Default = 0
0 - Disabled
1 - Enabled

Function:

The headphone amplifier will independently enter a low-power state when this function is enabled.

4.2.5 POWER DOWN LINE AMPLIFIER (PDNLN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The line output amplifier will independently enter a low-power state when this function is enabled.

4.2.6 POWER DOWN (PDN)

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire DAC device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation will begin.

4.2.7 CONTROL PORT ENABLE (CP_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The DAC will enter control port mode when this bit is enabled. This bit must be set prior to writing to the control port.

4.2.8 Channel A Analog Headphone Attenuation Control (address 02h) (HVOLA)

4.2.9 Channel B Analog Headphone Attenuation Control (address 03h) (HVOLB)

7	6	5	4	3	2	1	0
HVOLx7	HVOLx6	HVOLx5	HVOLx4	HVOLx3	HVOLx2	HVOLx1	HVOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Analog Headphone Attenuation Control operates independently from the Digital Volume Control. The Analog Headphone Attenuation Control registers allow attenuation of the headphone output signal for each channel in 1 dB increments from 0 to -25 dB. Attenuation settings are decoded using a 2's complement code, as shown in Table 1. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. All volume settings greater than zero are interpreted as zero.

Note: The Analog Headphone Attenuation only affects the headphone outputs. When set for levels greater than -10dB, the actual attenuation deviates from the register setting by more than 1 dB.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
11110110	-10	-10 dB
11110001	-15	-15 dB

Table 1. Example Analog Volume Settings

4.2.10 Channel A Digital Volume Control (address 04h) (DVOLA)

4.2.11 Channel B Digital Volume Control (address 05h) (DVOLB)

7	6	5	4	3	2	1	0
DVOLx7	DVOLx6	DVOLx5	DVOLx4	DVOLx3	DVOLx2	DVOLx1	DVOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1 dB increments from +18 to -96 dB. Volume settings are decoded using a 2's complement code, as shown in Table 2. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. All volume settings less than -96 dB are equivalent to muting the channel via the ATAPI bits (see Section 4.46).

Note: The digital volume control affects both the line outputs and the headphone outputs. Setting this register to values greater than +18 dB will cause distortion in the audio outputs.

Binary Code	Decimal Value	Volume Setting
00001010	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Table 2. Example Digital Volume Settings

4.2.12 Tone Control (address 06h)

7	6	5	4	3	2	1	0
BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
0	0	0	0	0	0	0	0

4.2.13 BASS BOOST LEVEL (BB)

Default = 0 dB (No Bass Boost)

Function:

The level of the shelving bass boost filter is set by Bass Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 3. Levels above +12 dB are interpreted as +12 dB.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 3. Example Bass Boost Settings

4.2.14 TREBLE BOOST LEVEL (TB)

Default = 0 dB (No Treble Boost)

Function:

The level of the shelving treble boost filter is set by Treble Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 4. Levels above +12 dB are interpreted as +12 dB.

Note: Treble Boost is not available in Double Speed Mode.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 4. Example Treble Boost Settings

4.2.15 Mode Control (address 07h)

7	6	5	4	3	2	1	0
BBCF1	BBCF0	TBCF1	TBCF0	A=B	DEM1	DEM0	VCBYP
0	0	0	0	0	0	0	0

4.2.16 BASS BOOST CORNER FREQUENCY (BBCF)

Default = 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - Reserved

Function:

The bass boost corner frequency is user selectable as shown above.

4.2.17 TREBLE BOOST CORNER FREQUENCY (TBCF)

Default = 00
00 - 2 kHz
01 - 4 kHz
10 - 7 kHz
11 - Reserved

Function:

The treble boost corner frequency is user selectable as shown above.

Note: Treble Boost is not available in Double Speed Mode.

4.2.18 CHANNEL A VOLUME = CHANNEL B VOLUME (A=B)

Default = 0
0 - Disabled
1 - Enabled

Function:

The AOUTA/HP_A and AOUTB/HP_B volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA/HP_A and AOUTB/HP_B are determined by the A Channel Attenuation and Volume Control Bytes, and the B Channel Bytes are ignored when this function is enabled.

4.2.19 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 μs/50 μs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (see Figure 31)

Note: De-emphasis is not available in Double Speed Mode.

4.2.20 DIGITAL VOLUME CONTROL BYPASS (VCBYP)

Default = 0
0 - Disabled
1 - Enabled

Function:

The digital volume control section is bypassed when this function is enabled. This disables the digital volume control, muting, bass boost, treble boost, limiting and ATAPI functions. The analog headphone attenuation control will remain functional.

4.2.21 Volume and Mixing Control (address 0Ah)

7	6	5	4	3	2	1	0
TC1	TC0	TC_EN	LIM_EN	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

4.2.22 TONE CONTROL MODE (TC)

Default = 00
00 - All settings are taken from user registers
01 - 12 dB of Bass Boost at 100 Hz and 6 dB of Treble Boost at 7 kHz
10 - 8 dB of Bass Boost at 100 Hz and 4 dB of Treble Boost at 7 kHz
11 - 4 dB of Bass Boost at 100 Hz and 2 dB of Treble Boost at 7 kHz

Function:

The Tone Control Mode bits determine how the Bass Boost and Treble Boost features are configured. The user defined settings from the Bass and Treble Boost Level and Corner Frequency registers are used when these bits are set to '00'. Alternately, one of three pre-defined settings may be used.

4.2.23 TONE CONTROL ENABLE (TC_EN)

Default = 0
0 - Disabled
1 - Enabled

Function:

The Bass Boost and Treble Boost features are active when this function is enabled.

4.2.24 ATAPI CHANNEL MIXING AND MUTING (ATAPI)

Default = 1001 - AOUTA/HP_A = L, AOUTB/HP_B = R (Stereo)

Function:

The CS42L50 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 5 and Figure 32 for additional information.

Note: All mixing functions occur prior to the digital volume control.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA/HP_A	AOUTB/HP_B
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 5. ATAPI Decode

4.2.25 Mode Control 2 (address 0Bh)

7	6	5	4	3	2	1	0
MCLKDIV	LINE1	LINE0	RESERVED	RESERVED	DIF2	DIF1	DIF0
0	0	0	0	0	0	0	0

4.2.26 MASTER CLOCK DIVIDE ENABLE (MCLKDIV)

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other DAC circuitry.

4.2.27 LINE AMPLIFIER GAIN COMPENSATION (LINE)

Default = 00
00 - 0.785 x VA
01 - 0.943 x VA
10 - Reserved

11 - Line Mute

Function:

The Line Amplifier Gain Compensation bits allow the user to scale the full-scale line output level according to the power supply voltage used. The full-scale line output level will be equal to {gain factor}xVA, where {gain factor} is selected from options above.

The Line Mute option is available to allow muting of the line output when the headphone output is still in use and the line amp is still powered up. To use this feature, first mute the outputs via the ATAPI bits. Next, set the LINE GAIN to Line Mute. Finally, un-mute the outputs with the ATAPI bits. Following these steps will ensure a click free mute.

4.2.28 DIGITAL INTERFACE FORMAT (DIF)

Default = 000 - Format 0 (I^2S, up to 24-bit data)

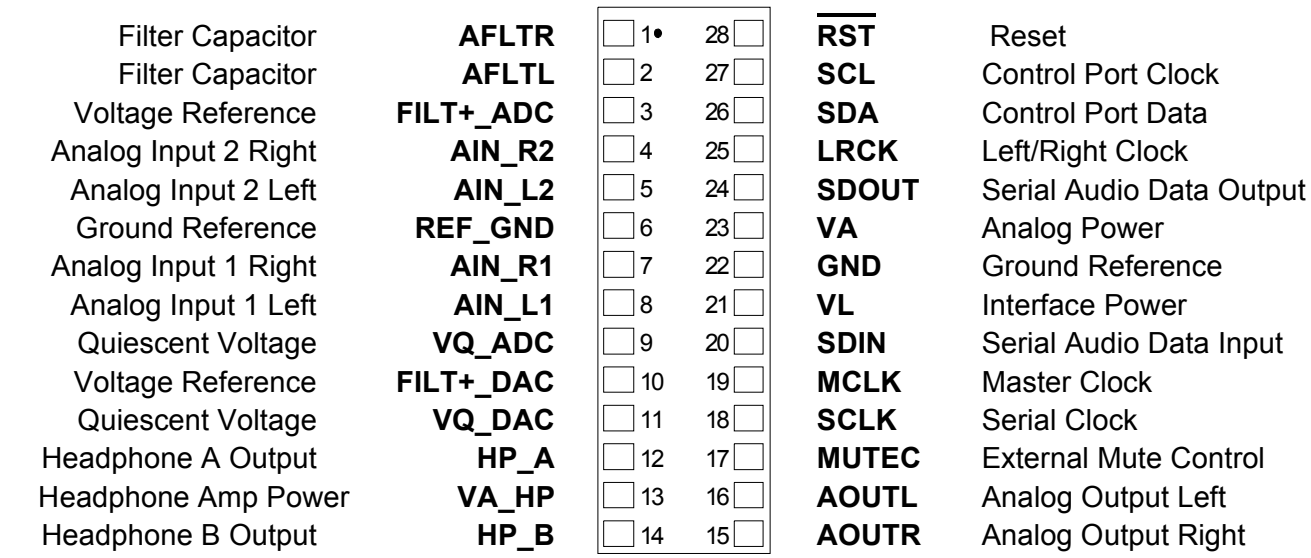
Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 25-30. It is recommended that the ADC and the DAC is configured for the same Digital Interface Format.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	I^2S, up to 24-bit data	0	30
0	0	1	Reserved	-	-
0	1	0	Left Justified, up to 24-bit data,	2	25
0	1	1	Right Justified, 24-bit data	3	27
1	0	0	Right Justified, 20-bit data	4	29
1	0	1	Right Justified, 16-bit data	5	26
1	1	0	Right Justified, 18-bit data	6	28
1	1	1	Identical to Format 0	0	30

Table 6. Digital Interface Format

5. PIN DESCRIPTIONS



Pin Name	#	Pin Description
VA	23	**Analog Power** (*Input*) **-** Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VL	21	**Logic Power** (*Input*) **-** Determines the required signal level for the digital input/output. Refer to the Recommended Operating Conditions for appropriate voltages.
VA_HP	13	**Headphone Amp Power** (*Input*) - Positive power supply for the headphone amplifier. Refer to the Recommended Operating Conditions for appropriate voltages.
VQ_ADC **VQ_DAC**	9,11	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage. VQ must be capacitively coupled to analog ground, as shown in the Typical Connection Diagram. The nominal voltage level is specified in the Analog Characteristics and Specifications section. VQ presents an appreciable source impedance and any current drawn from this pin will alter device performance. However, VQ can be used to bias the analog circuitry assuming there is no AC signal component and the DC current is less than 10uA.
REF_GND	6	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits and must be connected to analog ground.
GND	22	**Ground** (*Input*) - Ground reference. Should be connected to analog ground.
Serial Audio Interface		
MCLK	19	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
SCLK	18	**Serial Clock** (*Input*/*Output*) - Serial clock for the serial audio interface.
LRCK	25	**Left Right Clock** (*Input*/*Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN	20	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
SDOUT	24	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.

Analog Input/Output		
AIN_Rx **AIN_Lx**	4, 5, 7,8	**Analog Inputs** (*Input*) - The full scale analog input level is specified in the Analog Input Characteristics specification table.
AOUTL **AOUTR**	15, 16	**Analog Outputs** (*Output*) - The full scale analog line output level is specified in the Analog Output Characteristics specifications table.
HP_A **HP_B**	12, 14	**Headphone Outputs** (*Output*) **-** The full scale analog headphone output level is specified in the Analog Output Characteristics specifications table.
Control Port Interface		
SCL	27	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage as shown in the Typical Connection Diagram.
SDA	26	**Serial Control Data** (*Input/Output*) - SDA is a data I/O line and requires an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram.
Control & Misc.		
AFLTR **AFLTL**	1,2	**Anti-Aliasing Capacitors** *(Output)* - Anti-aliasing capacitors for the left and right channels. An external capacitor is required from AFLTR and AFLTL to ground, as shown in the Typical Connections Diagram. AFLTR and AFLTL are not intended to supply external current, and any current drawn from these pins will alter device performance.
FILT+_ADC	3	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to AGND as shown in the Typical Connection Diagram.
FILT+_DAC	10	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to AGND as shown in the Typical Connection Diagram.
MUTEC	17	**Mute Control** (*Output*) - The Mute Control pin goes low during power-up initialization, reset, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. The use of an external mute circuit is not mandatory but may be desired for designs requiring the absolute minimum in extraneous clicks and pops.
$\overline{\text{RST}}$	28	**Reset** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings when low. When high, the control port becomes operational and the CP_EN bits must be set and the PDN bits must be cleared before normal operation will occur. The control port cannot be accessed when Reset is low.

6. APPLICATIONS

6.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS42L50 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 shows the recommended power arrangement with VA, VA_HP, and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be used on each supply pin.

6.2 Clock Modes

The CS42L50 operates in one of two clocking modes. Single Speed Mode supports input sample rates up to 50 kHz, and Double Speed Mode supports input sample rates up to 100 kHz. All clock modes use 64x oversampling.

6.3 EP73xx Serial Port Interface

Special considerations must be made when interfacing the CS42L50 with the EP73xx series of ARM processors. To receive stereo data from the ADC, connect the MCLK pin (pin 19) of the CS42L50 to the BUZ pin (pin 93) of the EP73xx, and run the serial port in 64Fs mode with MCLK generation enabled on the EP73xx. Any other configuration, either hardware or software modes, will result in mono data being produced from the ADC of the CS42L50.

6.4 De-Emphasis

The CS42L50 includes on-chip digital de-emphasis. Figure 31 shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction.

6.5 Recommended Power-up Sequence

1) Hold $\overline{\text{RST}}$ low until the power supply, master clock and left/right clock are stable. In this state, the control port is reset to its default settings and VQ_ADC and VQ_DAC will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state and VQ_ADC and VQ_DAC remain low. The control port will be accessible at this time and the desired register settings can be loaded after setting the CP_EN bits and while keeping the PDN bits set to 1.
3) Once the registers are configured as desired, set the PDN bits to 0, initiating the power-up sequence.

6.6 Optional External Headphone Mute

An external headphone mute circuit, as shown in the CDB42L50 datasheet schematic, is recommended to minimize the effects of output transients during power-up and power-down. This technique minimizes the audio transients commonly produced by single-ended, single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs.

Use of the Mute Control function on the line outputs is recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios only limited by the external mute circuit. See the CDB42L50 datasheet for a suggested mute circuit.

7. CONTROL PORT INTERFACE

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if

no operation is required. Please note that the internal registers are separated into two unique chip address blocks, one for the control of the ADC and one for the control of the DAC portion of the codec.

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 5. The upper 6 bits of the 7 bit address field must be 001000. To communicate with the CS42L50, the chip address should match that of the ADC (0010000) or DAC (0010001) address. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, the contents of the register pointed to by the MAP will be output after the chip address.

The CS42L50 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

7.1 Memory Address Pointer (MAP)

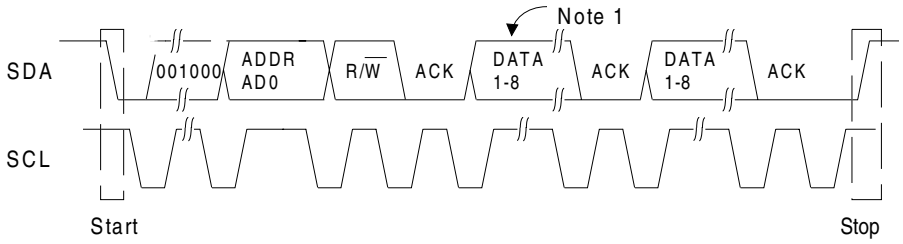
7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

7.2 INCR (AUTO MAP INCREMENT ENABLE)

Default = '0'
0 - Disabled
1 - Enabled

7.3 MAP0-3 (MEMORY ADDRESS POINTER)

Default = '0000'



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 5. Control Port Timing

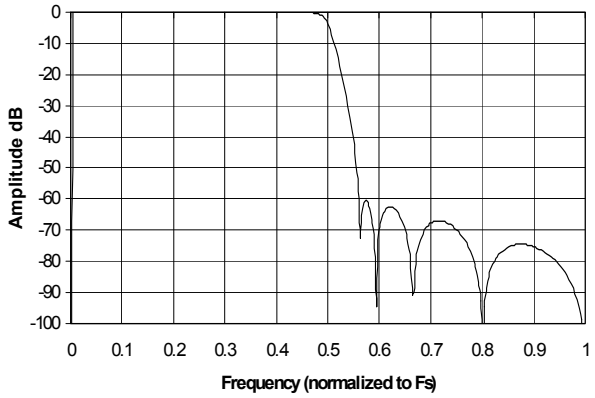


Figure 6. Decimation Filter Single Speed Stopband Rejection

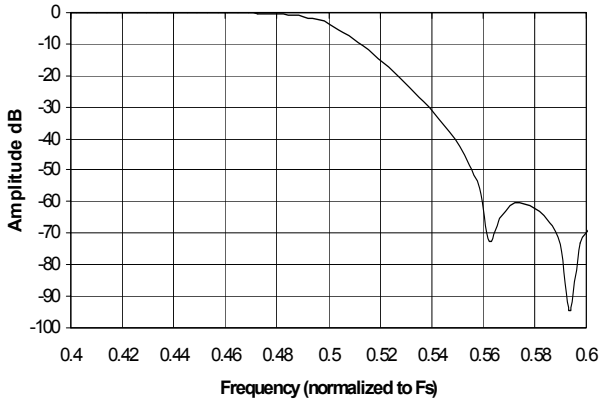


Figure 7. Decimation Filter Single Speed Transition Band

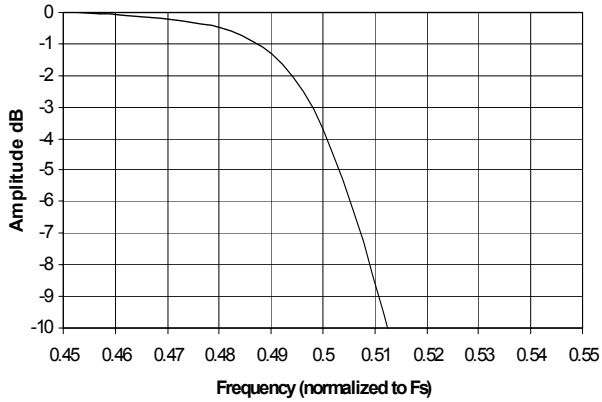


Figure 8. Decimation Filter Single Speed Transition Band (Detail)

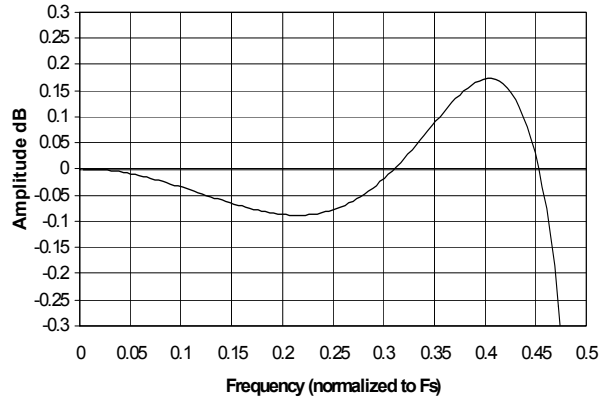


Figure 9. Decimation Filter Single Speed Passband Ripple

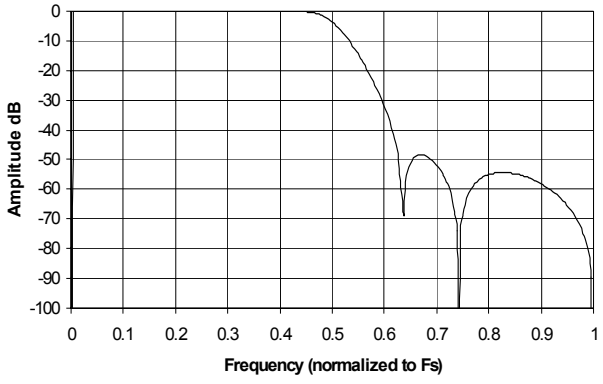


Figure 10. Decimation Filter Double Speed Stopband Rejection

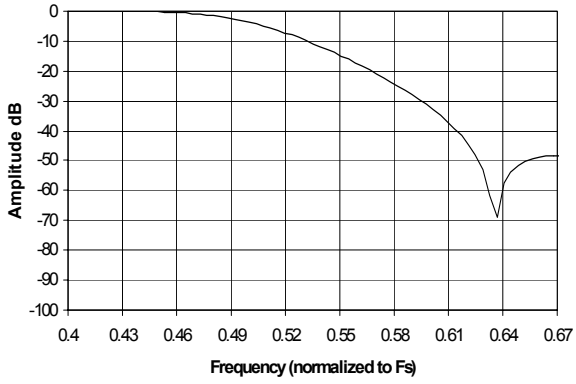


Figure 11. Decimation Filter Double Speed Transition Band

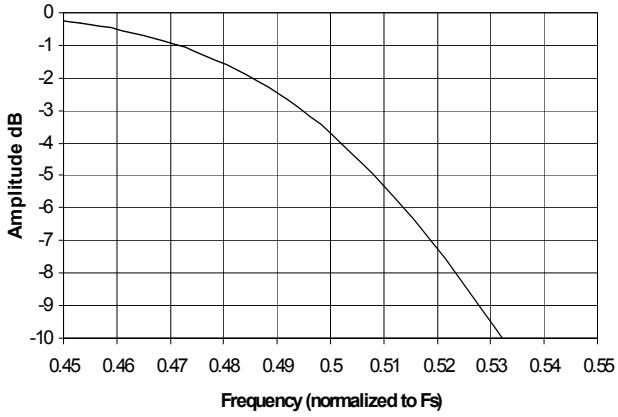


Figure 12. Decimation Filter Double Speed Transition Band (Detail)

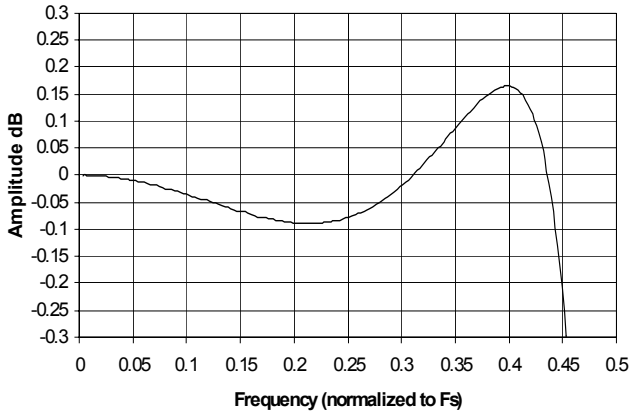


Figure 13. Decimation Filter Double Speed Passband Ripple

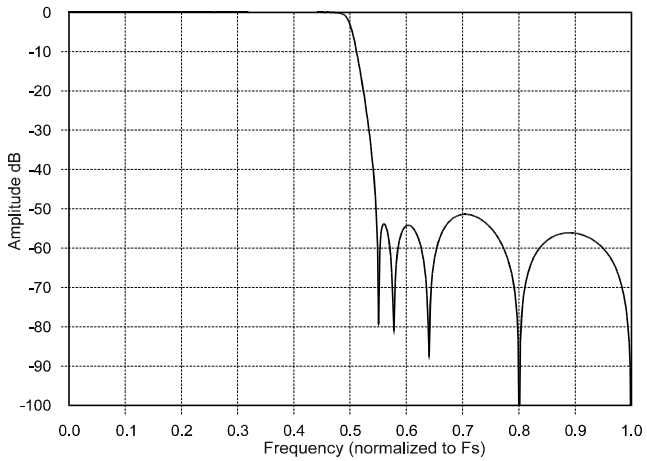


Figure 14. Interpolation Filter Single Speed Stopband Rejection

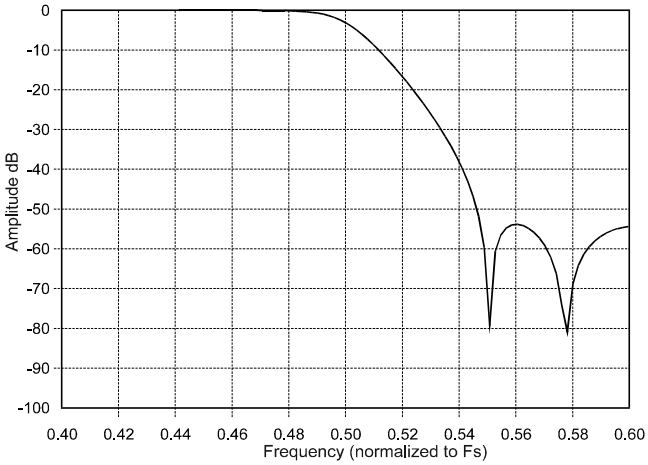


Figure 15. Interpolation Filter Single Speed Transition Band

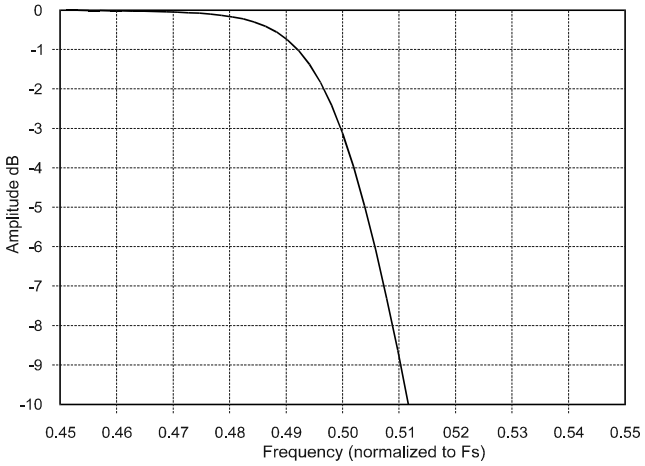


Figure 16. Interpolation Filter Single Speed Transition Band (Detail)

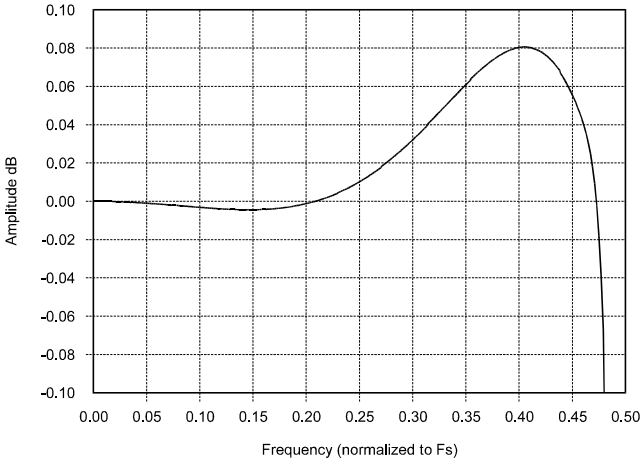


Figure 17. Interpolation Filter Single Speed Passband Ripple

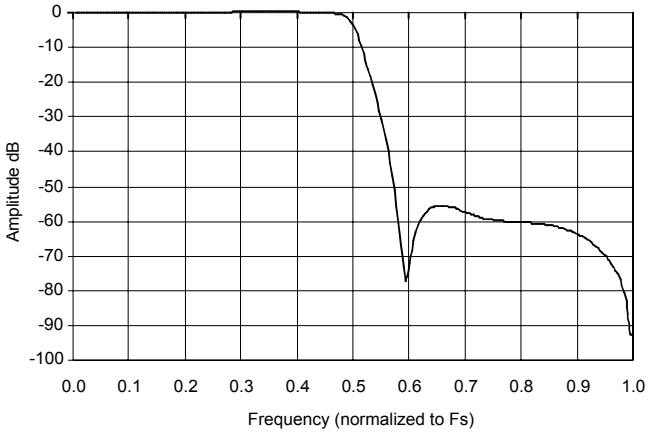


Figure 18. Interpolation Filter Double Speed Stopband Rejection

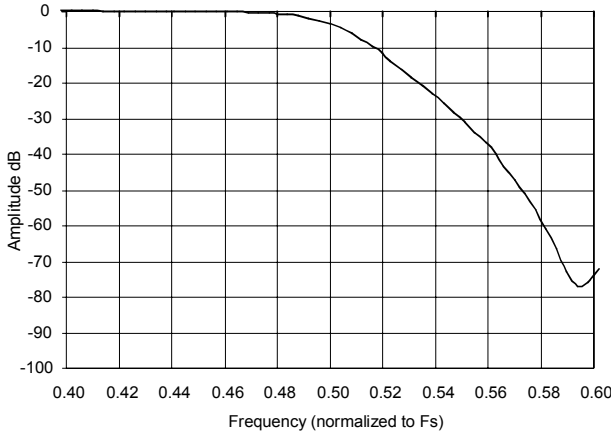


Figure 19. Interpolation Filter Double Speed Transition Band

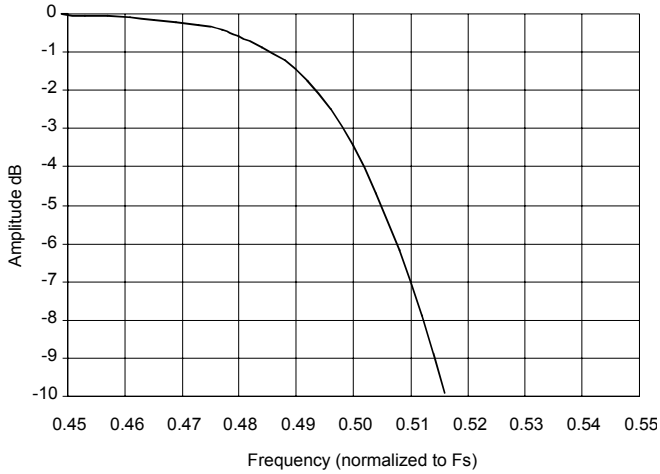


Figure 20. Interpolation Filter Double Speed Transition Band (Detail)

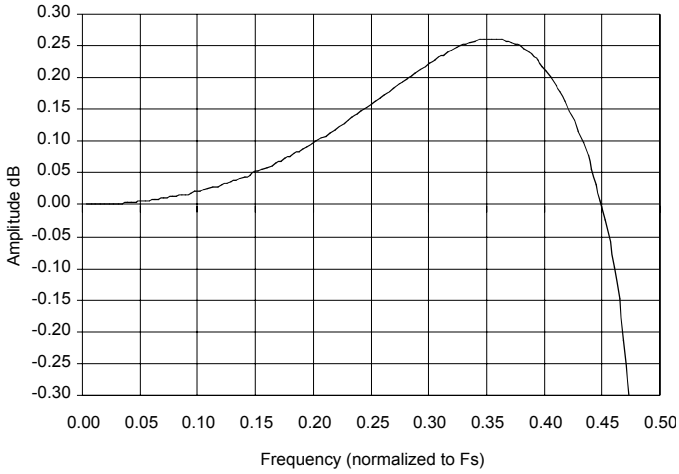


Figure 21. Interpolation Filter Double Speed Passband Ripple

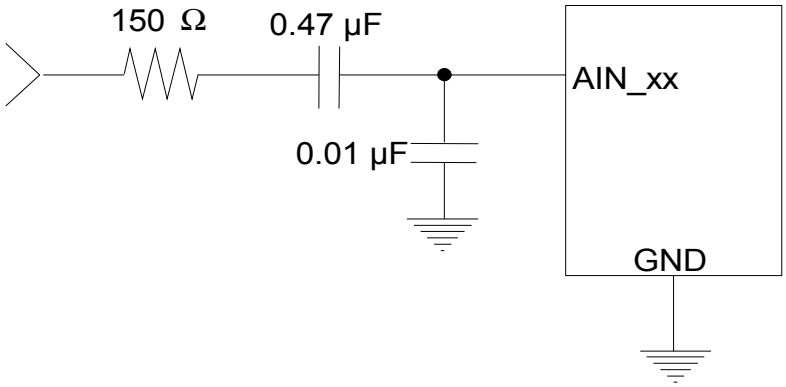


Figure 22. Line Input Test Circuit

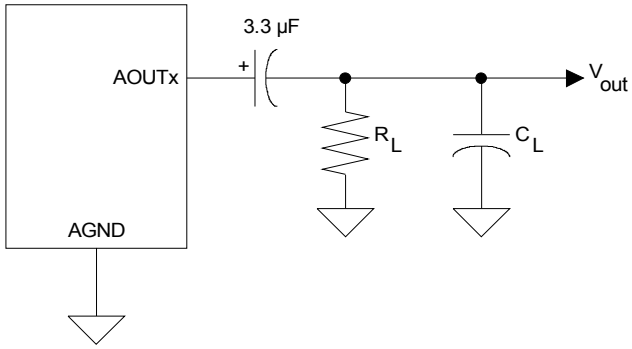


Figure 23. Line Output Test Load

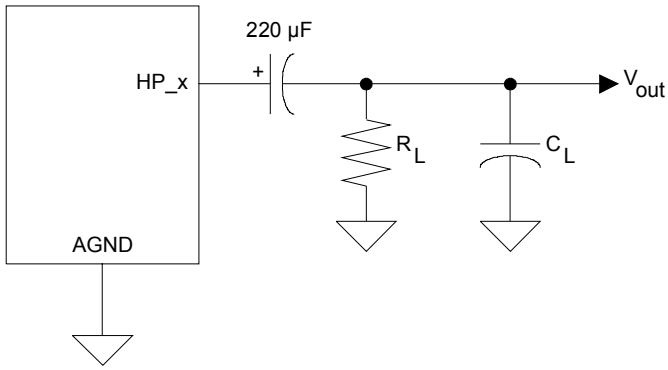
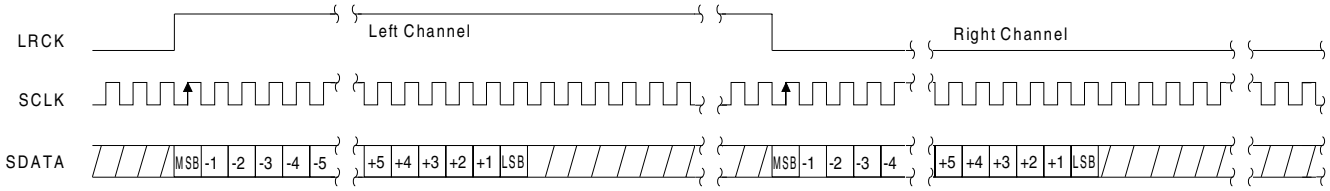
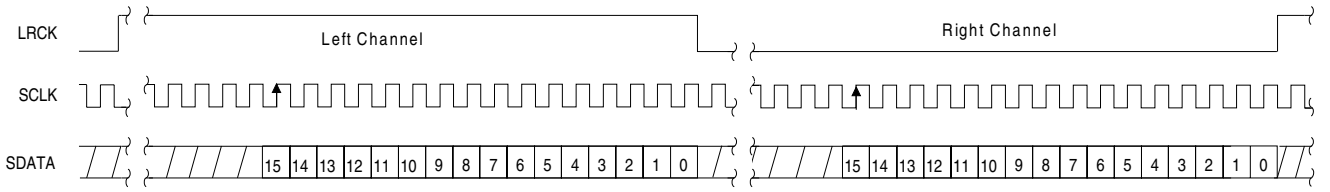


Figure 24. Headphone Output Test Load



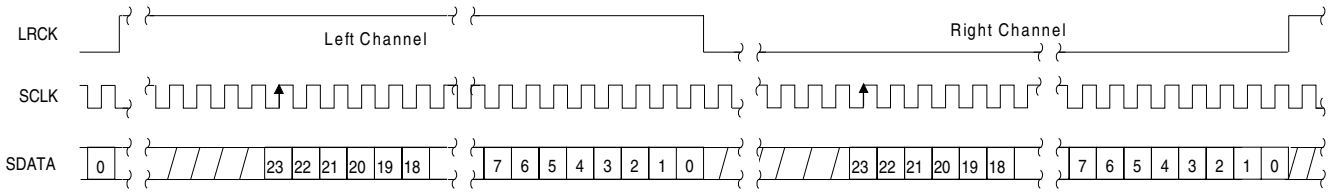
Left Justified, up to 24-Bit Data. Data Valid on Rising Edge of SCLK.

Figure 25. Left Justified, up to 24-bit data



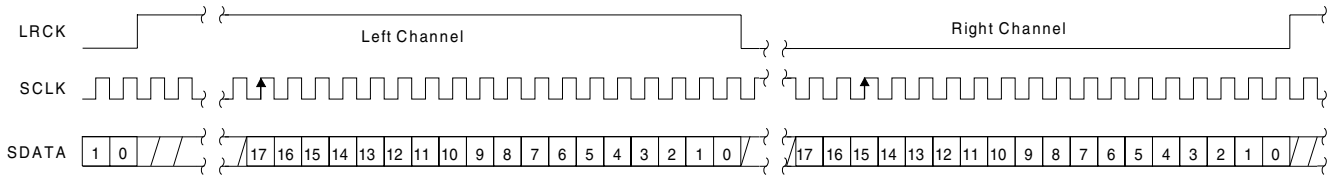
Right Justified, 16-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 32 Cycles per LRCK Period.

Figure 26. Right Justified, 16-bit data



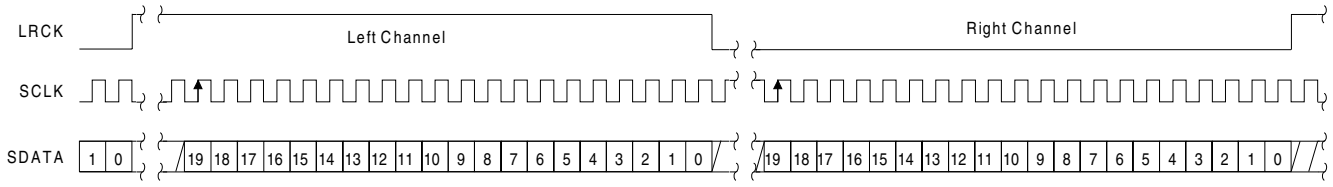
Right Justified, 24-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 48 Cycles per LRCK Period.

Figure 27. Right Justified, 24-bit data



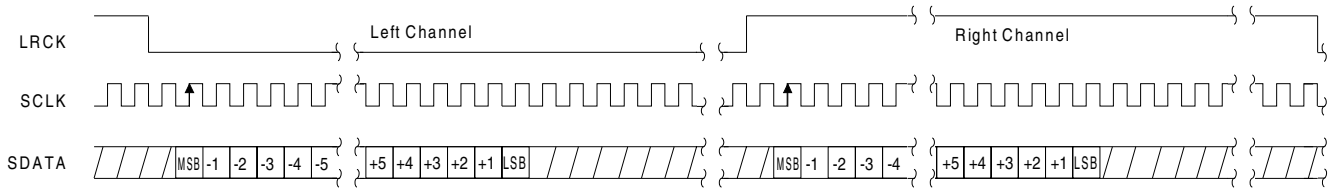
Right Justified, 18-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 36 Cycles per LRCK Period.

Figure 28. Right Justified, 18-bit data



Right Justified, 20-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 40 Cycles per LRCK Period.

Figure 29. Right Justified, 20-bit data



I^2S, up to 24-Bit Data. Data Valid on Rising Edge of SCLK

Figure 30. I^2S, up to 24-bit data

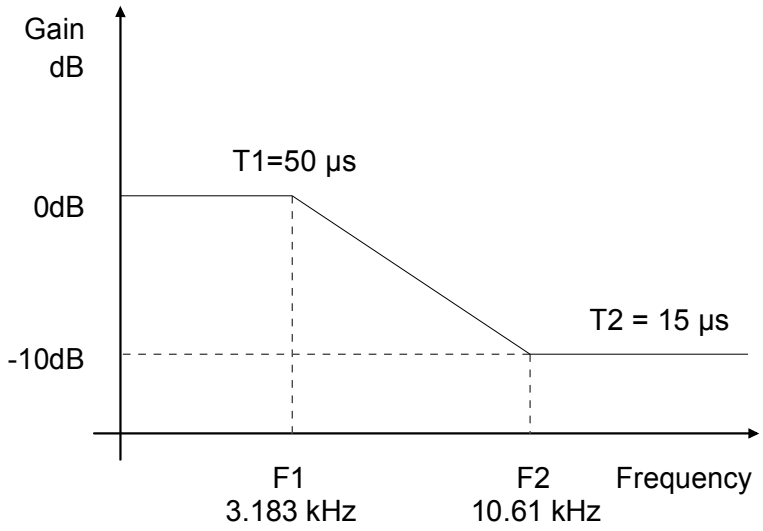


Figure 31. De-Emphasis Curve

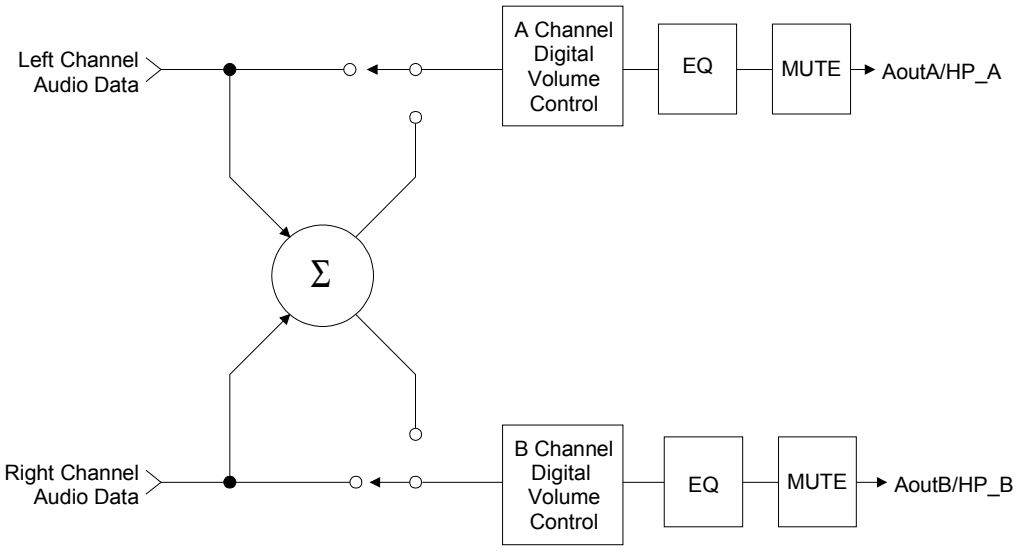


Figure 32. ATAPI Block Diagram

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

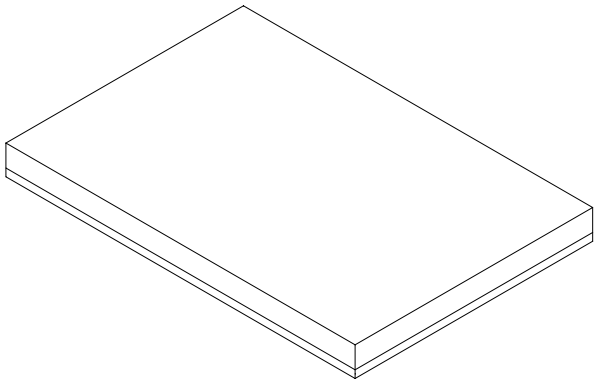
The change in gain value with temperature. Units in ppm/°C.

9. REFERENCES

1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

1) "The I^2C-Bus Specification: Version 2.1" Philips Semiconductors, January 2000. http://semiconductors.philips.com

10. PACKAGE DIMENSIONS



3. REFERENCE SPECIFICATIONS:
   A. AAWW SPEC #001−0531−2234: PACKING OPERATION PROCEDURE
   B. AAWW SPEC #001−0519−2062: MARKING.

2. THE BASIC METAL LAND GRID PITCH IS 0.65mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M−1994.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS DECIMAL: X.X ±0.1, X.XX ±0.05, X.XXX ±0.030 ANGULAR ±1° INTERPRET DIM AND TOL PER ASME Y14.5M − 1994	THIRD ANGLE PROJECTION		TITLE: PACKAGE OUTLINE − CTSON 28, 6.60mm X 9.70mm X 0.81mm, 0.60mm MOLD CAP, 0.5mmX1.3mm PAD, 0.65mm PITCH, LAMINATE SUBSTRATE, AWW			
MATERIAL: N/A	APPROVALS	DATE	SIZE: A3	SID NUMBER: N/A	DWG NUMBER: 82780	REV: 0A
FINISH: N/A	DESIGNED: NALHA	05/11/01	STRIP DWG NUMBER/REV: N/A	PKG OUTLINE DWG NO.: N/A	SCALE: NONE	SHEET: 1 OF 3
DO NOT SCALE DRAWING	CHECKED: GREME	05/11/01				
	PRODUCT MANAGER: EGARD	05/11/01				
	RELEASED					

Figure 33. Package Dimensions

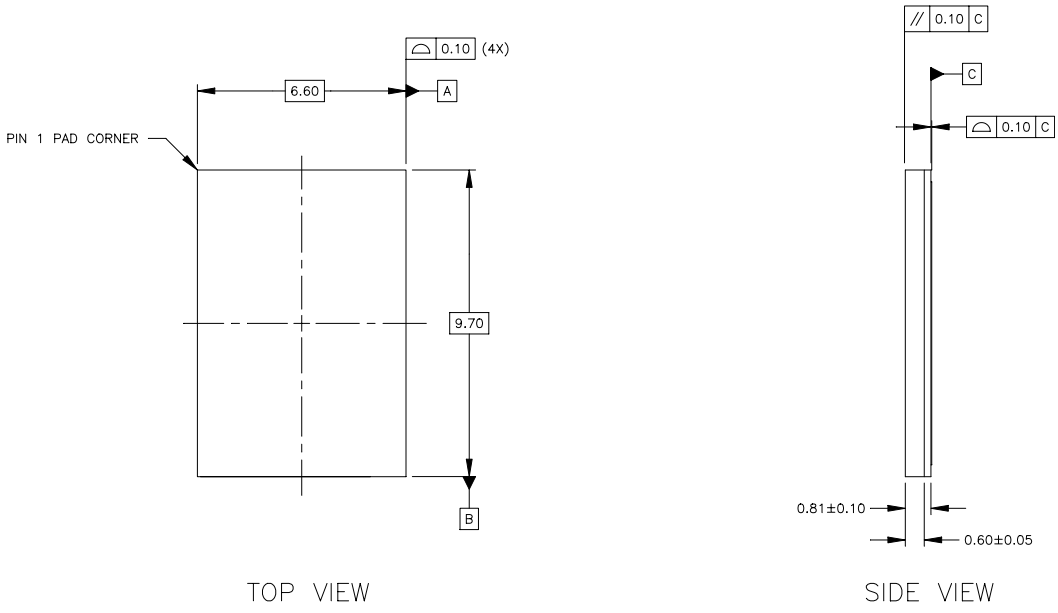


Figure 34. Package Top and Side Views

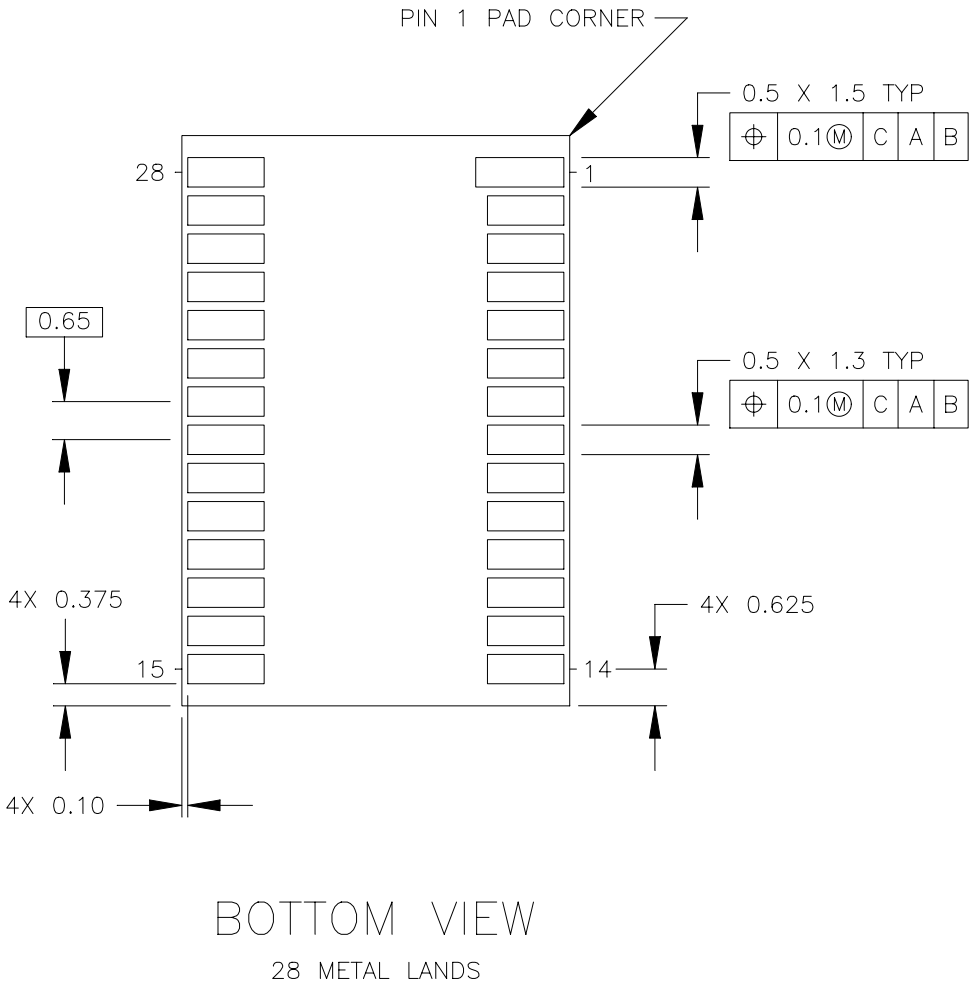


Figure 35. Package Bottom View


SMART
Analog
™