A DIVISION OF CIRRUS LOGIC

CS5181

ΔΣ Modulator & 400 kHz to 625 kHz 16-Bit ADC

Features

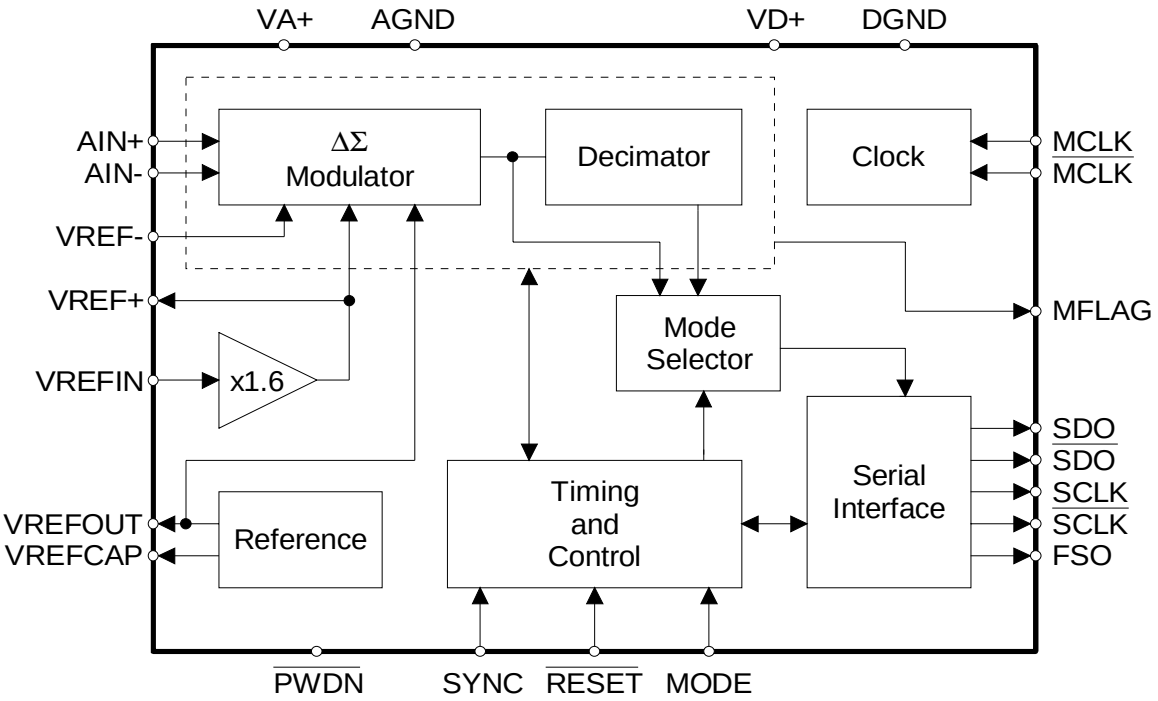
- 16-Bit Delta-Sigma A/D Converter
- Fully Differential Input with 4.0 V_{pp} Range
- Dynamic Range: 93 dB
- Spurious Free Dynamic Range: 90 dBc
- Harmonic Distortion: 89 dB
- Up to 625 kHz Output Word Rate
- No Missing Codes
- Non-Aliasing Low-Pass Digital Filter
- High Speed 3-Wire Serial Interface
- Supply Requirements:
  - VA+ = 5 V, VD+ = 3.3 V: 570 mW
- Modulator Output Mode
- Power-Down Mode

Description

CS5181 is a fully calibrated high-speed ΔΣ analog-to-digital converter, capable of 625 kSamples/second output word rate (OWR). The OWR scales with the master clock. It consists of a 5th order ΔΣ modulator, decimation filter, and serial interface. The chip can use the 2.375 V on-chip voltage reference, or an external 2.5 V reference. The input voltage range is 1.6 × VREFIN V_{pp} fully differential. Multiple CS5181s can be fully synchronized in multi-channel applications with a sync signal. The part has a power-down mode to minimize power consumption at times of system inactivity. The high speed digital I/O lines have complementary signals to help reduce radiated noise from traces on the PC board layout. The CS5181 can also be operated in modulator-only mode which provides the delta-sigma modulator bitstream as the output.

ORDERING INFORMATION

CS5181-BL	-40 °C to +85 °C	28-pin PLCC



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

Cirrus Logic, Inc.
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

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Contacting Cirrus Logic Support

For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

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CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = -40 to 85 °C; VA+ = 5 V ±5%, VD+ = 3.3 V ±0.3V; AGND = DGND = 0 V; MCLK = 40.0 MHz; VREFIN = VREFOUT; MODE = VD+; Analog Source Impedance = 301 Ohms with 2200 pF to AGND; Full-Scale input Sinewave at 22 kHz; Unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Performance						
Dynamic Range	(Note 1)	DR	89	93	-	dB
Total Harmonic Distortion @ 22 kHz	(Note 1)	THD	84	89	-	dB
Signal to (Noise + Distortion)		SINAD	82	87	-	dB
Spurious Free Dynamic Range		SFDR	84	90	-	dBc
Static Performance						
Integral Nonlinearity	(Note 2)	INL	-	±2	-	LSB
Differential Non-Linearity	(Note 2)	DNL	-	-	±0.5	LSB
Full Scale Error	(Note 6)		-	±8	-	LSB
Full Scale Drift with Internal Reference	(Notes 2 and 5)		-	±50	-	ppm/°C
Offset Error	(Note 6)		-	±8	-	LSB
Offset Drift	(Note 2)		-	±6.0	-	µV/°C
Analog Input						
Differential Input Voltage Range	(Note 3)		-	1.6 X VREFIN	-	V_{pp}
Common Mode Range		CMR	1	-	VREFIN + 0.25	V
Input Capacitance			-	4.0	-	pF
Differential Input Impedance (capacitive)			-	300	-	kΩ
Common Mode Rejection Ratio	(Note 2)	CMRR	50	-	-	dB
Common Mode Input Current			-	±160	±320	µA
Reference Input						
VREFIN			2.25	2.375	2.6	V
VREFIN Current	(Note 4)		-	1	±320	µA
Reference Output						
VREFOUT Voltage			2.25	2.375	2.5	V
VREFOUT Output Current			-	-	±500	µA
VREFOUT Impedance			-	0.1	-	Ω

Notes:
1. Dynamic range is tested with a 22 kHz input signal 60 dB below full scale.
2. Specification guaranteed by design, characterization, and/or test.
3. Full scale fully-differential input span is nominally 1.6 X the VREFIN voltage. The peak negative excursion of the signals at AIN+ or AIN- should not go below AGND for proper operation.
4. VREFIN current is less than 1 µA under normal operation, but can be as high as ±320 µA during calibration.
5. Drift of the on-chip reference alone is typically about ±30 ppm/°C. If using an external reference, total full scale drift will be that of the external reference plus an additional ±20 ppm/°C, which is the typical drift of the X1.6 buffer.
6. Applies after self-calibration at final operating ambient temperature.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies					
Power Supply Current (MODE = 1, $\overline{PWDN}$ = 1) (Note 7) VA1+, VA2+ = 5 V VD1+, VD2+ = 3.3 V		 - -	 53 92.4	 65 100	 mA mA
Power Supply Current (MODE = 1, $\overline{PWDN}$ = 0) (Notes 7, 8) VA1+, VA2+ = 5 V VD1+, VD2+ = 3.3 V		 - -	 3.7 0.062	 6 0.2	 mA mA
Power Supply Current (MODE = 0, $\overline{PWDN}$ = 1) (Note 7) VA1+, VA2+ = 5 V VD1+, VD2+ = 3.3 V		 - -	 53 18.9	 65 22	 mA mA
Power Supply Current (MODE = 0, $\overline{PWDN}$ = 0) (Notes 7, 8) VA1+, VA2+ = 5 V VD1+, VD2+ = 3.3 V		 - -	 3.7 0.062	 6 0.2	 mA mA
Power Supply Rejection (Note 9)	PSRR	-	55	-	dB

Notes: 7. All outputs unloaded. All inputs except MCLK held static at VD+ or DGND.

8. Power consumption when $\overline{PWDN}$ = 0 applies only for no master clock applied (MCLK held high or low).

9. Measured with a 100 mV_{pp} sine wave on the VA+ supplies at a frequency of 100 Hz.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Modulator Sampling Frequency		-	MCLK	-	Hz
Output Word Rate		-	MCLK/64	-	Hz
Filter Characteristics ***(Note 2)***					
-3 dB Corner		-	MCLK/142.3804	-	Hz
Passband Ripple		-	-	±0.05	dB
Stopband Frequency		-	MCLK/128	-	Hz
Stopband Rejection		90	-	-	dB
Group Delay		-	2370/MCLK	-	s

DIGITAL CHARACTERISTICS (T_A = -40 to 85 °C; VD = 3.3V ±0.3V; AGND = DGND = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (I_O = -100 µA)	V_{OH}	2.7	-	-	V
Low-Level Output Voltage (I_O = 100 µA)	V_{OL}	-	-	0.3	V
Input Leakage Current	I_{in}	-	±1	±10	µA
Input Capacitance	Cin	-	6	-	pF

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = -40 to 85 °C; VA+ = 5 V ±5%, VD+ = 3.3 V ±0.3 V; AGND = DGND = 0 V; MODE = VD+)

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency (Note 2)	MCLK	0.512	25 to 40	41	MHz
Master Clock Duty Cycle		45	-	55	%
Rise Times (Notes 2, 10, and 11)	t_{rise}				
Any Digital Input, Except MCLK		-	-	100	ns
MCLK		-	-	.2/MCLK	s
Any Digital Output		-	20	-	ns
Fall Times (Notes 2, 10, and 11)	t_{fall}				
Any Digital Input, Except MCLK		-	-	100	ns
MCLK		-	-	.2/MCLK	s
Any Digital Output		-	20	-	ns
Calibration/Sync					
$\overline{\text{RESET}}$ rising to MCLK rising		-	3	-	ns
$\overline{\text{RESET}}$ rising recognized, to FSO falling		-	988205/MCLK	-	s
SYNC rising to MCLK rising		-	3	-	ns
SYNC rising recognized to FSO falling		-	5161/MCLK	-	s
$\overline{\text{PWDN}}$ rising recognized to FSO falling		-	5168/MCLK	-	s
SYNC high time		1/MCLK	-	-	s
$\overline{\text{RESET}}$ low time		1/MCLK	-	-	s
Serial Port Timing (Note 12)					
SCLK frequency		-	MCLK/3	-	Hz
SCLK high time	t_1	-	1/MCLK	-	s
SCLK low time	t_2	-	2/MCLK	-	s
FSO falling to SCLK rising	t_3	-	2/MCLK + 2E-9	-	s
SCLK falling to new data bit	t_4	-	1.5	-	ns
SCLK rising to FSO rising	t_5	-	1/MCLK - 2E-9	-	s

Notes: 10. Rise and Fall times are specified at 10% to 90% points on waveform.

11. $\overline{\text{RESET}}$, SYNC, and $\overline{\text{PWDN}}$ have Schmitt-trigger inputs.

12. Specifications applicable to complementary signals $\overline{\text{SCLK}}$ and $\overline{\text{SDO}}$.

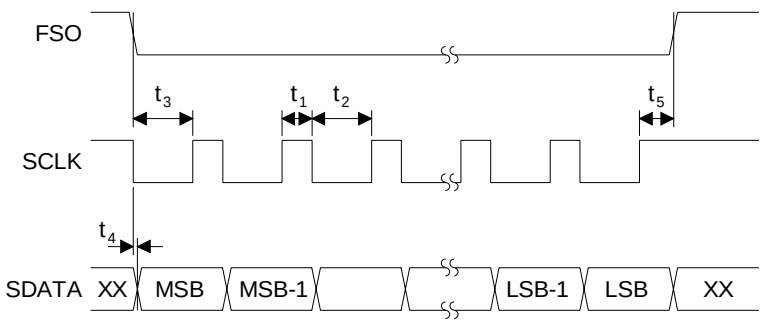


Figure 1. Serial Port Timing (not to scale)

RECOMMENDED OPERATING CONDITIONS (AGND = DGND = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Digital	VD+	3.0	3.3	3.6	V
	Analog	VA+	4.75	5	5.25	V
Analog Reference Voltage		VREFIN	2.25	2.5	2.6	V
AGND to DGND differential			-100	0	100	mV
Operating Junction Temperature		T_j	-	-	120	°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
DC Power Supplies	Ground	AGND/DGND	-0.3	(VD+) + 0.3	V
	Digital	VD+	-0.3	6.0	V
	Analog	VA+	-0.3	6.0	V
Input Current, Any pin except Supplies		I_{in}	-	±10	mA
Output Current		I_{out}	-	±25	mA
Power Dissipation (Total)			-	1000	mW
Analog Input Voltage		V_{INA}	-0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Specifications are subject to change without notice.

GENERAL DESCRIPTION

The CS5181 is a monolithic CMOS 16-bit A/D converter designed to operate in continuous mode after being reset.

The CS5181 can operate in modulator-only mode in which the bit stream from the modulator is the data output from the device.

THEORY OF OPERATION

The front page of this data sheet illustrates the block diagram of the CS5181.

Converter Initialization: Calibration and Synchronization

The CS5181 does not have an internal power-on reset circuit. Therefore when power is first applied to the device the $\overline{\text{RESET}}$ pin should be held low until power is established. This resets the converter's logic to a known state. When power is fully established the converter will perform a self-calibration, starting with the first MCLK rising edge after $\overline{\text{RESET}}$ goes high. The converter will use 988,205 MCLK cycles to complete the calibration and to allow the digital filter to fully settle, after which, it will output fully-settled conversion words. The converter will then continue to output conversion words at an output word rate equal to MCLK/64. Figure 2 illustrates the $\overline{\text{RESET}}$ and SYNC logic and timing for the converter.

The CS5181 is designed to perform conversions continuously with an output rate that is equivalent to MCLK/64. The conversions are performed and the serial port is updated independent of external controls. The converter is designed to measure differential bipolar input signals, and unipolar signals, with a common mode voltage of between 1.0 V and VREF + 0.25 V. Calibration is performed when the $\overline{\text{RESET}}$ signal to the device is released. If $\overline{\text{RESET}}$ is properly framed to MCLK, the converter can be synchronized to a specific MCLK cycle at the system level.

The SYNC signal can also be used to synchronize multiple converters in a system. When SYNC is used, the converter does not perform calibration. The SYNC signal is recognized on the first rising edge of MCLK after SYNC goes high. SYNC aligns the output conversion to occur every 64 MCLK clock cycles after the SYNC signal is recognized and the filter is settled. After the SYNC is initiated by going high, the converter will wait 5,161 MCLK cycles for the digital filter to settle before putting out a fully-settled conversion word. To synchronize multiple converters in a system, the SYNC pulse should rise on a falling edge of the MCLK signal. This ensures that the SYNC input to all CS5181s in the system will be recognized on the next rising edge of MCLK. Use of the SYNC input

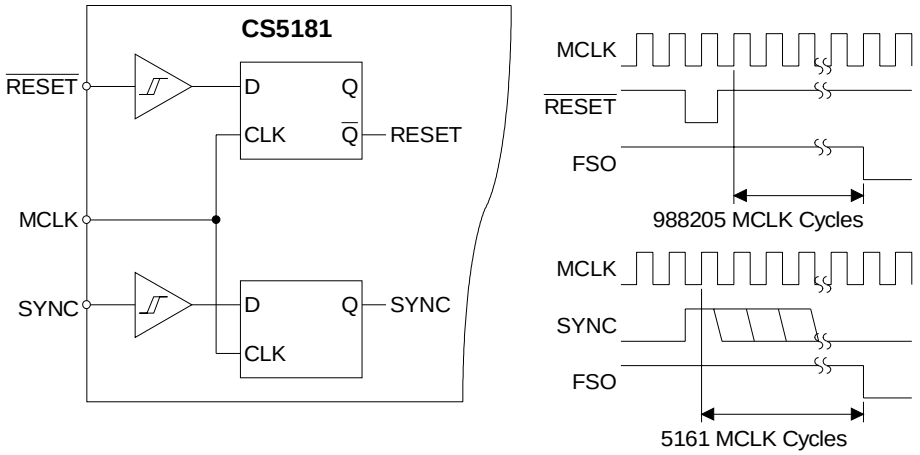


Figure 2. $\overline{\text{RESET}}$ and SYNC logic and timing.

is not necessary to make the converter operate properly. If it is unused it should be tied to DGND.

Conversion data is output from the SDO and $\overline{\text{SDO}}$ pins of the device. The data is output from the SDO pin MSB first, in two's complement format. The converter furnishes a serial clock SCLK and its complement $\overline{\text{SCLK}}$ to latch the data bits; and a data frame signal, Frame Signal Output (FSO), which frames the output conversion word. The SCLK output frequency is MCLK/3.

Clock Generator

The CS5181 must be driven from a CMOS-compatible clock at its MCLK pin. The MCLK input is powered from the VD+ supply and its signal input should not exceed this supply. The required MCLK is 64 × OWR (Output Word Rate). To achieve an Output Word Rate of 625 kHz, the MCLK frequency must be 64 × 625 kHz, or 40 MHz. A second clock input pin, $\overline{\text{MCLK}}$, is not actually used inside the device but allows the user to run a fully differential clock to the converter to minimize radiated noise from the PC board layout.

The CS5181 can be operated with MCLK frequencies from 512 kHz up to 40 MHz. The output word rate scales with the MCLK rate with OWR = MCLK/64.

Voltage Reference

The CS5181 can be configured to operate from either its internal voltage reference, or from an external voltage reference.

The on-chip voltage reference is nominally 2.375 V and is referenced to the AGND pins. This 2.375 V reference is output from the VREFOUT pin. It is then filtered and returned to the VREFIN pin. The VREFIN pin is connected to a buffer which has a typical gain of 1.6. This scales the on-chip reference of 2.375 V to 3.8 V. This value sets the peak-to-peak input voltage into the AIN pins of the converter. Figure 3 illustrates the CS5181 connected to use the internal voltage reference. Note that a 1.0 µF and 0.1 µF capacitor are shown connected to the VREFCAP pin to filter out noise. A larger capacitor can be used, but may require a longer reset period when first powering up the part to allow for the reference to stabilize before the part self-calibrates.

Alternatively, the CS5181 can be configured to use an external voltage reference. Figure 4 illustrates the CS5181 connected to use a 2.5 V external reference. In this case, the maximum peak-to-peak signal input at the AIN pins is 4.0 V.

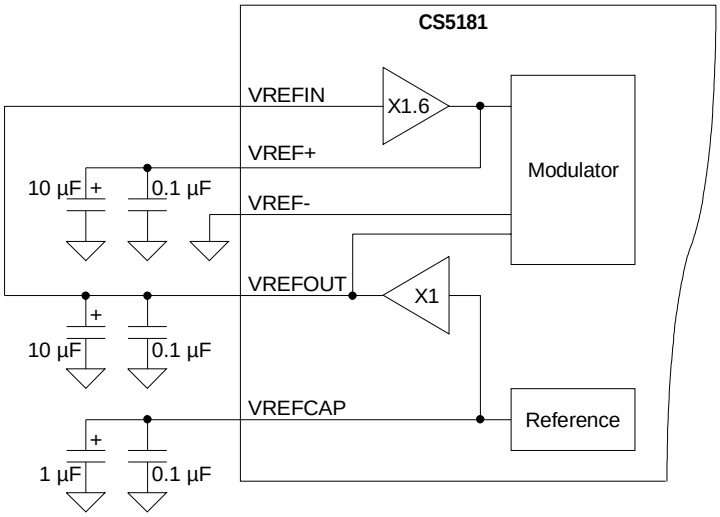


Figure 3. CS5181 connection diagram for using the internal voltage reference.

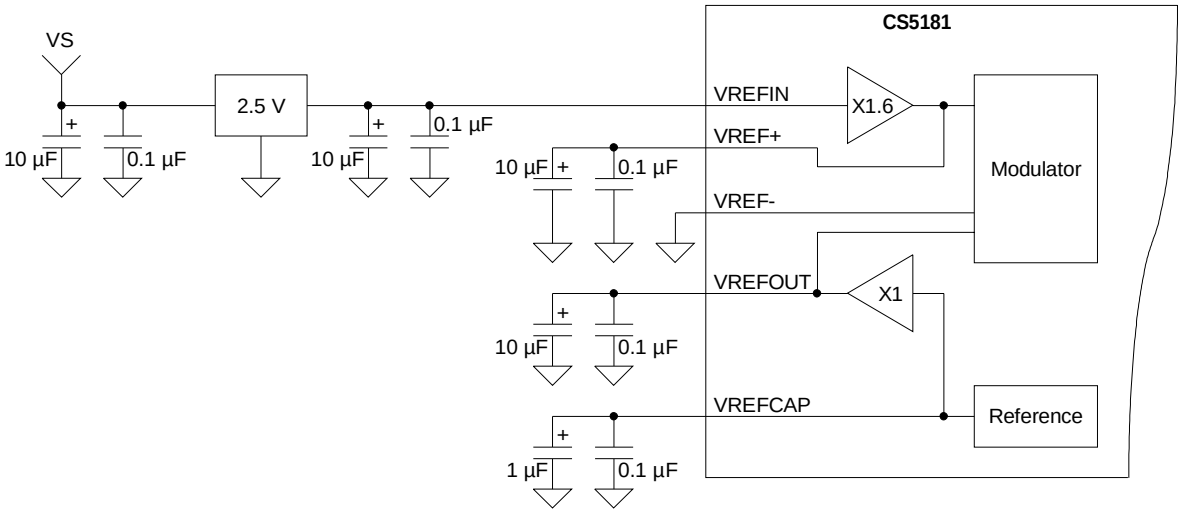


Figure 4. CS5181 connection diagram for using an external voltage reference.

Analog Input

The analog signal to the converter is input into the AIN+ and AIN- pins. The input signal is fully differential with the maximum peak-to-peak amplitude of VREFIN X 1.6 V. The signal needs to have a common mode voltage in a range from 1.0 V to VREF + 0.25 V for minimum distortion. A resistor-capacitor filter should be included on the AIN+ and AIN- inputs of the converter. This should consist of a 20 Ω resistor and a 2200 pF capacitor on each input to ground as illustrated in the system connection diagram (Figure 11).

Output Coding

Table 1 illustrates the output coding for the converter when operating with the digital filter (MODE = 1). The converter outputs its data from the serial port in twos complement format, MSB first.

The chip offers an MFLAG signal to indicate when the modulator has gone unstable. MFLAG is set when an overrange signal forces the modulator into an unstable condition. Under this condition, output codes from the converter will be locked to either plus or minus full scale as is appropriate for the overrange condition.

Fully Differential Bipolar Input Voltage[1]	Twos Complement
>(V_{FS} - 1.5 LSB)	7FFF
V_{FS} - 1.5 LSB	7FFF / 7FFE
-0.5 LSB	0000 / FFFF
-V_{FS} + 0.5 LSB	8001 / 8000
<(-V_{FS} + 0.5 LSB)	8000

Notes: 1. V_{FS} = VREFIN x 1.6

Table 1. Output Coding.

Modulator-Only mode

The CS5181 can be operated in modulator-only mode by connecting the MODE pin to a logic 0 (DGND).

In modulator-only mode the noise-shaped bitstream from the fifth-order delta-sigma modulator is output from the SDO and $\overline{SDO}$ (inverse bitstream) pins.

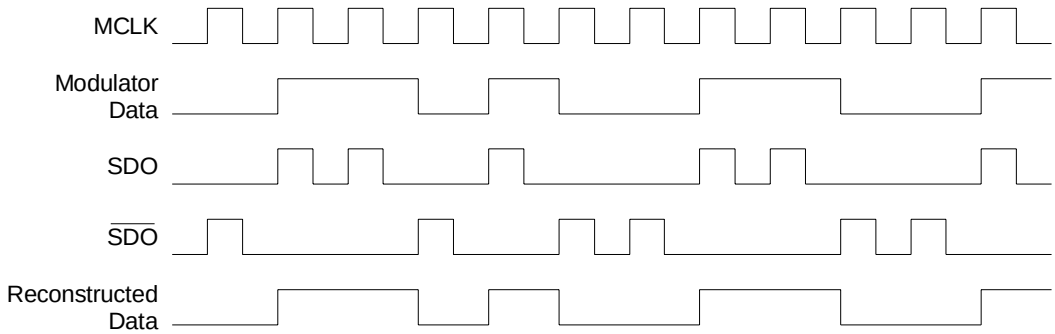


Figure 5. Modulator Only Mode Data RTZ Format.

The data from the modulator is output from SDO/SDO in RTZ (Return to Zero) format. The circuit in Figure 6 can be used to reconstruct the data so it can be captured with the rising or falling edge of MCLK.

Table 2 illustrates the magnitude of the input signal into the chip versus the ones density out of the modulator. The table does not take into account the potential offset and gain errors of the modulator and their effect on the ones density.

Fully Differential Bipolar Input Voltage[2]	Modulator Ones Density[3]
V_{FS}	75%
0	50%
$-V_{FS}$	25%

Notes: 2. V_{FS} = VREFIN x 1.6
3. Ones density is approximate; it does not take offset and gain errors into consideration.

Table 2. Modulator-Only Mode Ones Density.

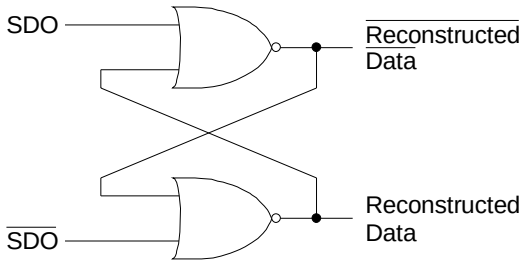


Figure 6. Circuit to Reconstruct Return-to-Zero (RTZ) Data from SDO/SDO into Original Modulator Bitstream.

Figure 7 and Figure 8 illustrate magnitude versus frequency plots of the modulator bitstream when running at 40.0 MHz.

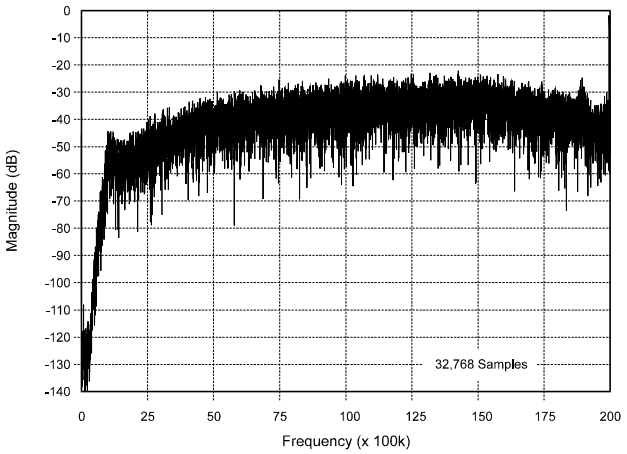


Figure 7. Magnitude versus frequency spectrum of modulator bitstream (MCLK = 40.0 MHz).

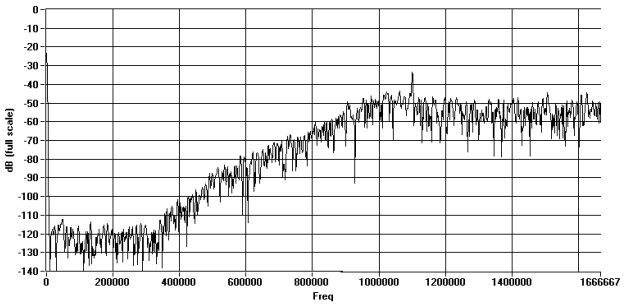


Figure 8. Expanded view of the magnitude versus frequency spectrum of modulator bitstream (MCLK = 40 MHz).

Instability Indicator

The MFLAG signal is functional in both modes of operation of the part and indicates when the modulator has been overdriven into an unstable condition. In the modulator only mode (MODE = 0), the MFLAG signal will remain set for 3 MCLK cycles when the modulator goes unstable, before being returned to the reset state. While the input condition causing modulator instability persists, the MFLAG signal will continually get set for 3 MCLK cycles and then get reset.

When the decimation filter on the part is operational (MODE = 1), the MFLAG signal is set when the modulator goes unstable. In this mode, however, the MFLAG signal stays set until 5,120 MCLK cycles after the input condition causing modulator instablility is removed. This delay is provided to allow the digital filter time to settle, and the part will output fully settled conversion words after the MFLAG signal goes low.

Digital Filter Characteristics

Figure 9 illustrates the magnitude versus frequency plot of the converter when operating at a 625 kHz output word rate. The filter is a non-aliasing 4265 tap filter with a -3 dB corner at 0.4495 of the output word rate and an out-of-band attenuation of at least 90 dB at frequencies above one half the output word rate. The passband ripple is less than ±0.05 dB up to the -3 dB corner frequency. Figure 10 illustrates the phase response of the digital filter with the converter operating at 625 kHz output word rate. The filter characteristics change proportional to changes in the MCLK rate.

The group delay of the digital filter is 2370 MCLK cycles (59.3 µs with MCLK = 40 MHz), and the settling time is 4740 MCLK cycles (118.5 µs).

Serial Interface

The CS5181 has a serial interface through which conversion words are output in a synchronous self-clocking format. The serial port consists of the Serial Data Output pin (SDO), and its complement ($\overline{SDO}$); Serial Clock (SCLK), and its complement ($\overline{SCLK}$); and the Frame Sync Output (FSO). FSO falls at the beginning of an output word. Data is output in twos complement format, MSB first. FSO stays low for 16 SCLK cycles. SCLK is output at a rate equal to MCLK/3.

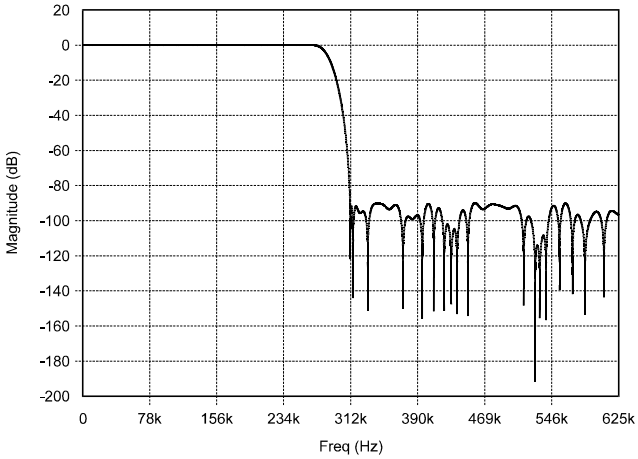


Figure 9. CS5181 Digital Filter Magnitude Response (MCLK = 40 MHz)

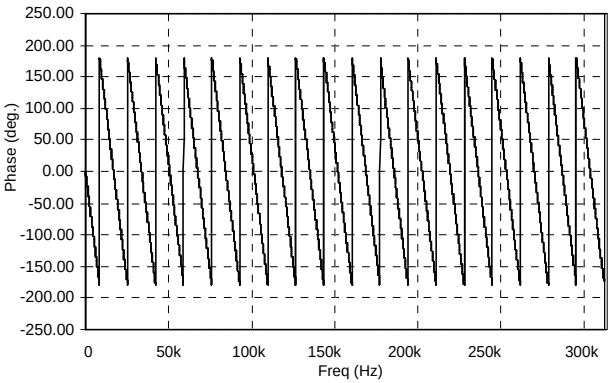


Figure 10. CS5181 Digital Filter Phase Response (MCLK = 40 MHz)

Power Supplies / Board Layout

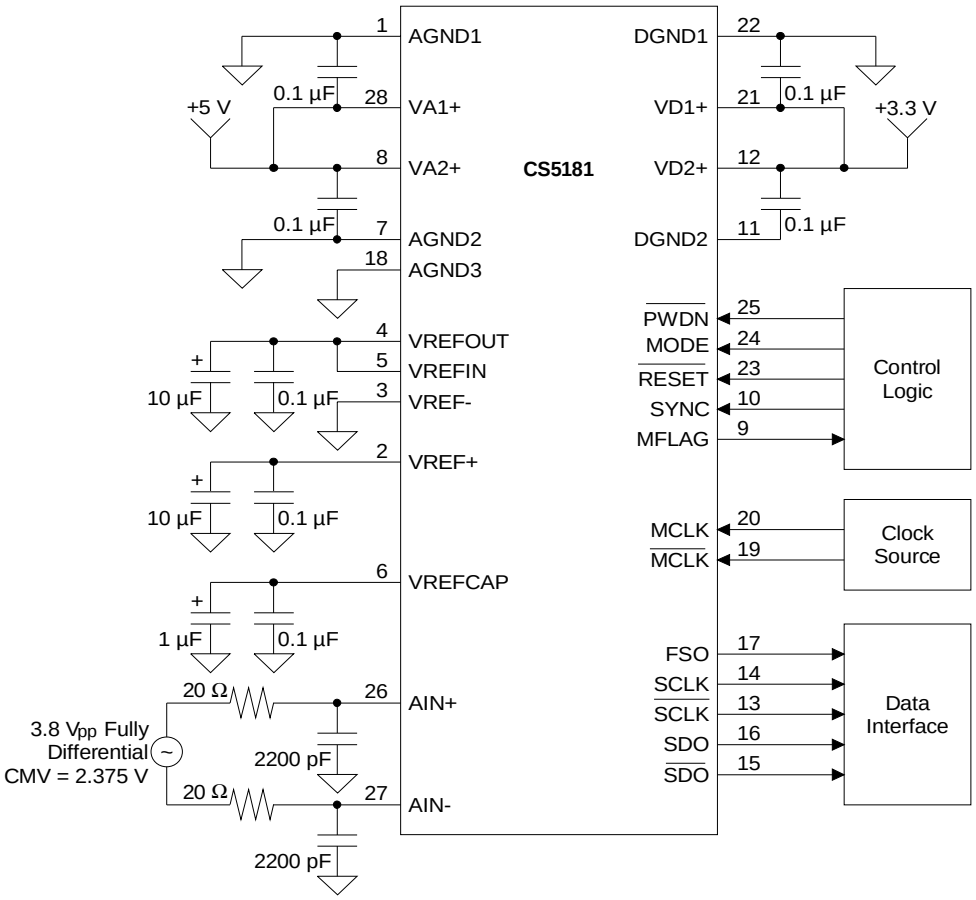
The CS5181 requires an analog supply voltage of 5.0 Volts and a digital supply voltage of 3.3 Volts (nominal) for proper operation.

Figure 11 illustrates the system connection diagram for the chip. For best performance, each of the supply pins should be bypassed to the nearest ground pin on the chip. The bypass capacitors should be located as close to the chip as possible. If the chip is surface mounted the bypass capacitors should be on the same side of the circuit card as the chip.

The CS5181 is a high speed component that requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include the use of ground and power planes, using low noise power supplies in conjunction with proper supply decoupling, minimizing circuit trace lengths, and physical separation of digital and analog components and circuit traces.

It is preferred that any clock oscillator circuitry be located on a ground plane separate from the digital plane in order to ensure that digital noise does not induce clock jitter.

For additional insight, see the CDB5181 evaluation board for more details. Also refer to Application Note AN18 which covers layout and design rules for high resolution data converters.



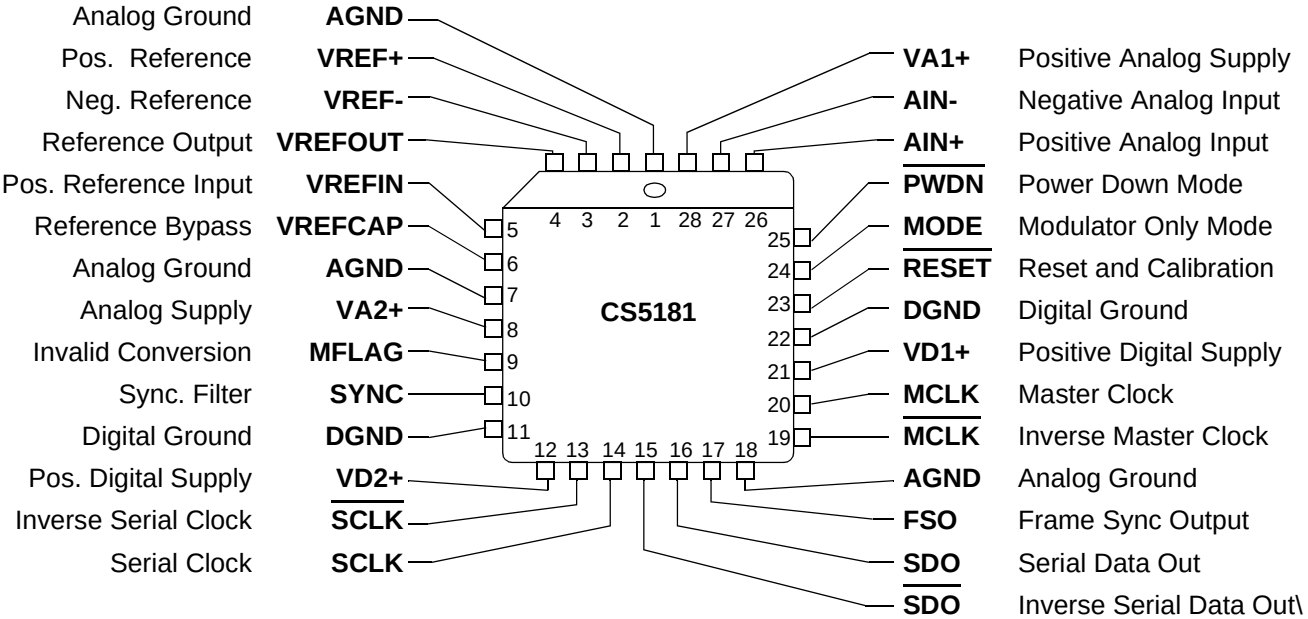
The 3.8 V_{pp} fully differential input span is set by the converter's internal voltage reference at 2.375 V.
An input span of 4.0 V_{pp} fully differential would result if an external voltage reference of 2.5 V is used.

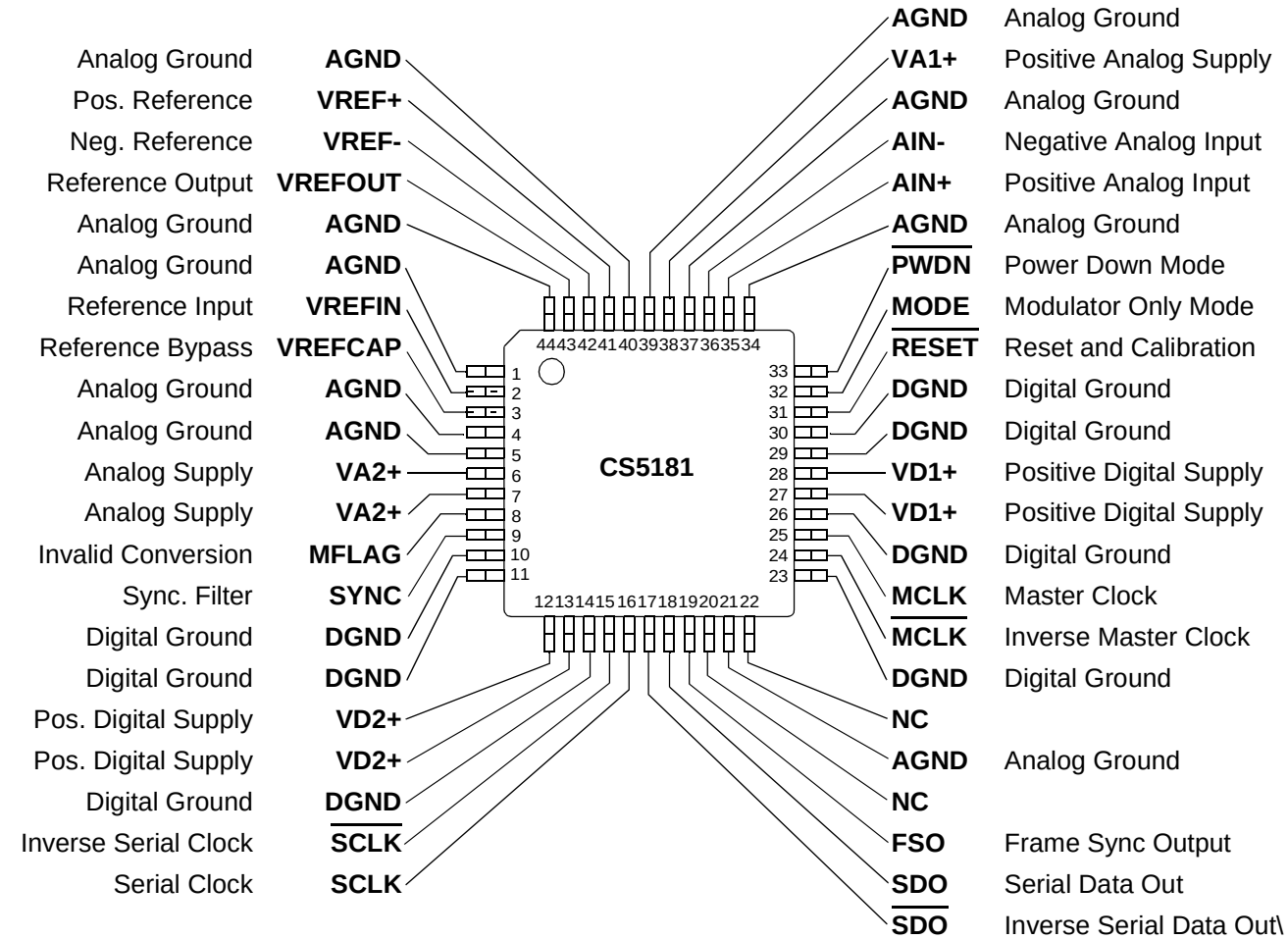
Figure 11. CS5181 System Connection Diagram

Power-down Mode

The CS5181 has a $\overline{\text{PWDN}}$ (power-down) function. When active low, power to most of the converter's circuitry will be reduced. If MCLK is to be stopped to save power, it should not be stopped until at least ten clock cycles after $\overline{\text{PWDN}}$ is taken low. The ten clock cycles are required to allow the part to turn off it's internal circuitry. If the part does not get the full ten clock cycles, it will still go into a power down state, but the power dissipation could be more than is listed in the specifications for the full power down condition. When $\overline{\text{PWDN}}$ is active, the calibration information inside of the converter is maintained. When coming out of the power-down state, the converter is not recalibrated and will start-up similar to when SYNC is initiated.

PIN DESCRIPTIONS





Supply Inputs

VA1+, VA2+ — Positive Analog Supply

Input for the positive analog supply is +5.0 V typical when AGND is 0 V.

AGND — Analog Ground

Analog ground for circuits supplied by VA+.

VD1+, VD2+ — Positive Digital Supply

Input for positive digital supply is +3.3 V typical when DGND is 0 V.

DGND — Digital Ground

Digital ground for circuits supplied by VD+.

Signal and Reference Related Inputs

AIN+, AIN- — Differential Analog Inputs

Fully differential signal inputs.

VREFIN — Voltage Reference Input

VREFOUT or an external reference is connected to VREFIN. Analog input voltage (full scale fully differential peak-to-peak) into the converter is 1.6 times this value.

VREF+ — Positive Voltage Reference

Filter capacitor connection for the reference input buffer. The voltage on this pin equals VREFIN X 1.6.

VREF- — Negative Voltage Reference

VREF- is connected to AGND.

VREFOUT — Voltage Reference Output

Output pin for the 2.375 volt on-chip reference relative to AGND.

VREFCAP — Reference Bypass

Filter capacitor connection for internal reference.

Serial Interface I/O Signals

SCLK, $\overline{\text{SCLK}}$ — Serial Interface Clock

Serial Clock Output. A gated serial clock output from the converter at a rate equal to 1/3 the MCLK clock rate. The $\overline{\text{SCLK}}$ output is a complement of SCLK and helps reduce radiated noise if the two lines are run adjacent on the PC board layout and drive a balanced load.

SDO, $\overline{\text{SDO}}$ — Serial Data Out

Serial Data Output. Output pin for 16-bit serial data word. The $\overline{\text{SDO}}$ output is the complement of SDO and helps to reduce radiated noise if the two lines are run adjacent on the PC board layout. Output data is output in twos complement format MSB first.

FSO — Frame Sync Output

Frame Sync Output. The Frame Sync Output turns low to indicate the beginning of an output word from the SDO pin. It returns high after the 16 data bits have been clocked out.

Control Pins

$\overline{\text{RESET}}$ — Reset and Calibration

When the $\overline{\text{RESET}}$ pin is pulled to a logic low the converter will perform a reset of its digital logic. When the level on this pin is brought back to a logic high the chip starts normal operation, following a two clock cycle delay period. When MODE = 1, the chip goes through an internal gain and offset calibration routine following this reset sequence.

$\overline{\text{PWDN}}$ — Power Down Mode

A logic 0 on the $\overline{\text{PWDN}}$ pin will put the device into a power-down mode.

MODE — Modulator Only Mode

MODE is held at a logic high for normal operation. In normal operation the device utilizes the digital decimation filter and calibration ciruitry. MODE = 0 puts the part in modulator only mode whereby most of the digital circuitry is powered-down and the modulator bit-stream is output from the SDO and $\overline{\text{SDO}}$ pins.

SYNC — Synchronization of Filter

The SYNC input can be used to restart the digital filter of the converter at the beginning of its convolution cycle. The SYNC input is used to synchronize the filters of multiple converters in a system. When the SYNC signal goes high, the filter will be initialized and will begin its convolution cycle on the next rising edge of MCLK. If not used, tie SYNC to DGND.

MFLAG — Invalid Conversion Flag

MFLAG goes high if the modulator portion of the converter goes unstable. If MFLAG is high, the output data from the converter may be invalid.

MCLK, $\overline{\text{MCLK}}$ — Master Clock Signal

Master clock input accepts a CMOS level clock input to the converter with worst case duty cycle of 45-55% (typically 40 MHz). $\overline{\text{MCLK}}$ is not actually used inside the device, but can be used for radiated noise cancellation if MCLK and $\overline{\text{MCLK}}$ are run adjacent to each other on the PC board.

PARAMETER DEFINITIONS

Differential Non-Linearity Error - DNL

The deviation of a code's width from ideal. Units in LSBs.

Integral Non-Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Full-Scale Error - FSEP

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Offset Error - VOS

The deviation of the mid-scale transition from the ideal (1/2 LSB below 0 Volts). Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the full-scale signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Units in dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant harmonics (2nd thru 7th), to the rms value of the full-scale signal. Units in decibels.

Dynamic Range - DR

The ratio of the rms value of the inferred full-scale signal, to the rms sum of the broadband noise signals below the Nyquist rate (excepting dc and distortion terms). Expressed in decibels. Dynamic Range is tested with a 22 kHz input signal 60 dB below full scale. 60 dB is then added to the resulting number to refer the noise level to the full-scale signal. This technique ensures that the distortion components are below the noise level and do not affect the measurement.

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the full-scale signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Group Delay

The time delay through the digital filter section of the part. Units in seconds.

Resolution - N

The number of different output codes possible. Expressed as N, where 2^N is the number of available output codes.

Noise -

A measure of the variability of the converter's output when a fixed DC input (usually ground) is applied to the input and a large number of samples are taken. RMS noise is determined statistically as the Standard Deviation of the Probability Density Function derived from the histogram of the ADC with the differential inputs shorted together and tied to an appropriate common mode voltage.

Common Mode Rejection Ratio - CMRR

A measure of the device's ability to cancel out the effect of a common voltage applied to both of its differential inputs. CMRR is specified as the ratio of the differential signal gain to the gain for the common-mode signal. Units in dB.

Offset Drift -

Changes in the offset error of the part after self calibration due to changes in ambient temperature. Specified in microvolts per degree C, relative to the input signal.

Full Scale Drift -

Changes in the full scale error of the part after self calibration due to changes in ambient temperature. Specified in parts-per-million (PPM) of the full scale range per degree C.

APPENDIX A: CIRCUIT APPLICATIONS

Several amplifier circuits have been tested with the CS5181. Performance at higher frequencies is generally limited by the operational amplifiers used to drive the A/D converter.

Figure 12 illustrates a single operational amplifier circuit which can accept a single-ended ground-referenced signal and condition it for the input of the CS5181. The amplifier is AC-coupled to the signal source. In this circuit the AIN- input to the CS5181 is held at a constant DC value and the AIN+ input is driven (it is actually overdriven to achieve high dynamic range, but this sacrifices performance with regard to distortion). The common mode voltage for the CS5181 input should be designed to stay between 1 V and VREF + 0.25 V when driven at its AIN+ and AIN- inputs. The single amplifier circuit in figure 12 has the disadvantages that the common mode restriction limits the input signal range and also causes errors due to variation in the common mode voltage, as opposed to applying a balanced differential signal.

Figures 13 and 14 illustrate the performance of the amplifier of Figure 12 operating with a 3.8 V_{pp} input into the AIN+ input; and with 2.0 V_{pp} input into the AIN+ input respectively.

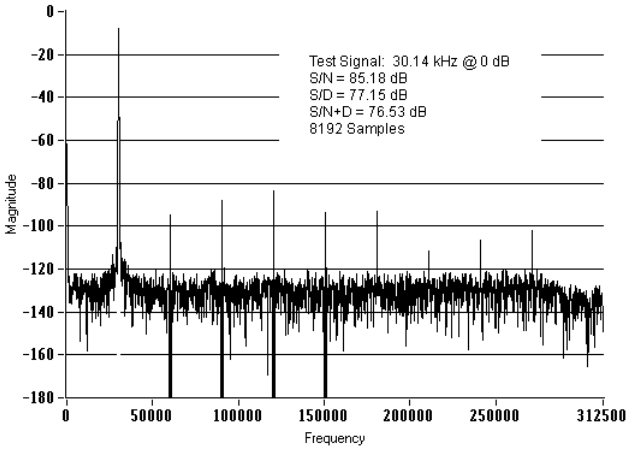


Figure 13. Performance of amplifier of Figure 12 overdriving AIN+ input to the CS5181 at 3.8 V_{PP}

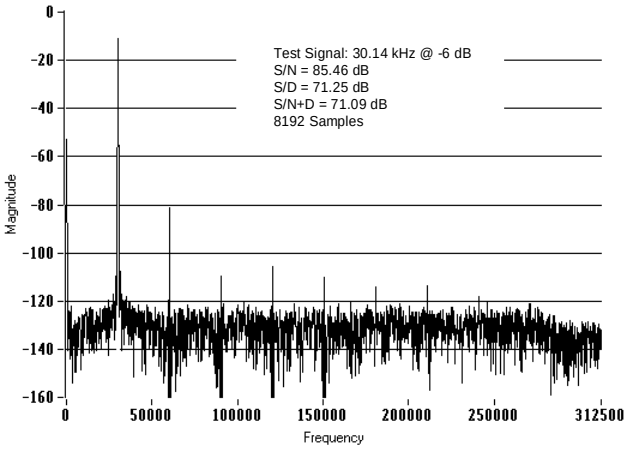


Figure 14. Performance of amplifier of Figure 12 with AIN+ driven at 2.0 V_{PP}

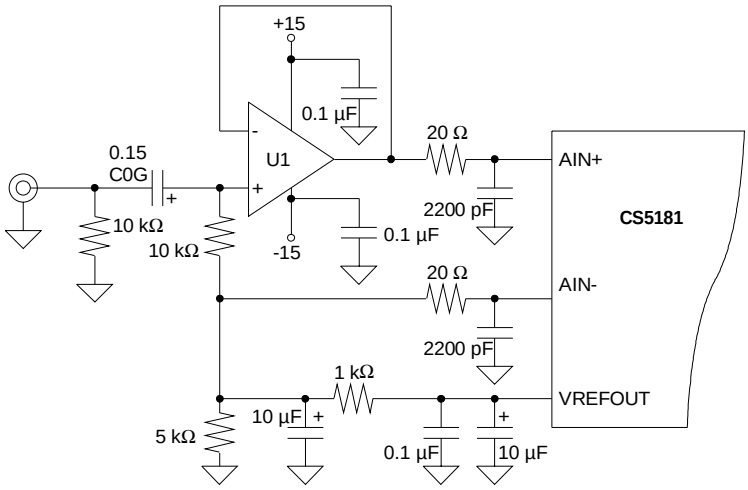


Figure 12. Single amplifier driving only AIN+, with AIN- held at a steady dc value

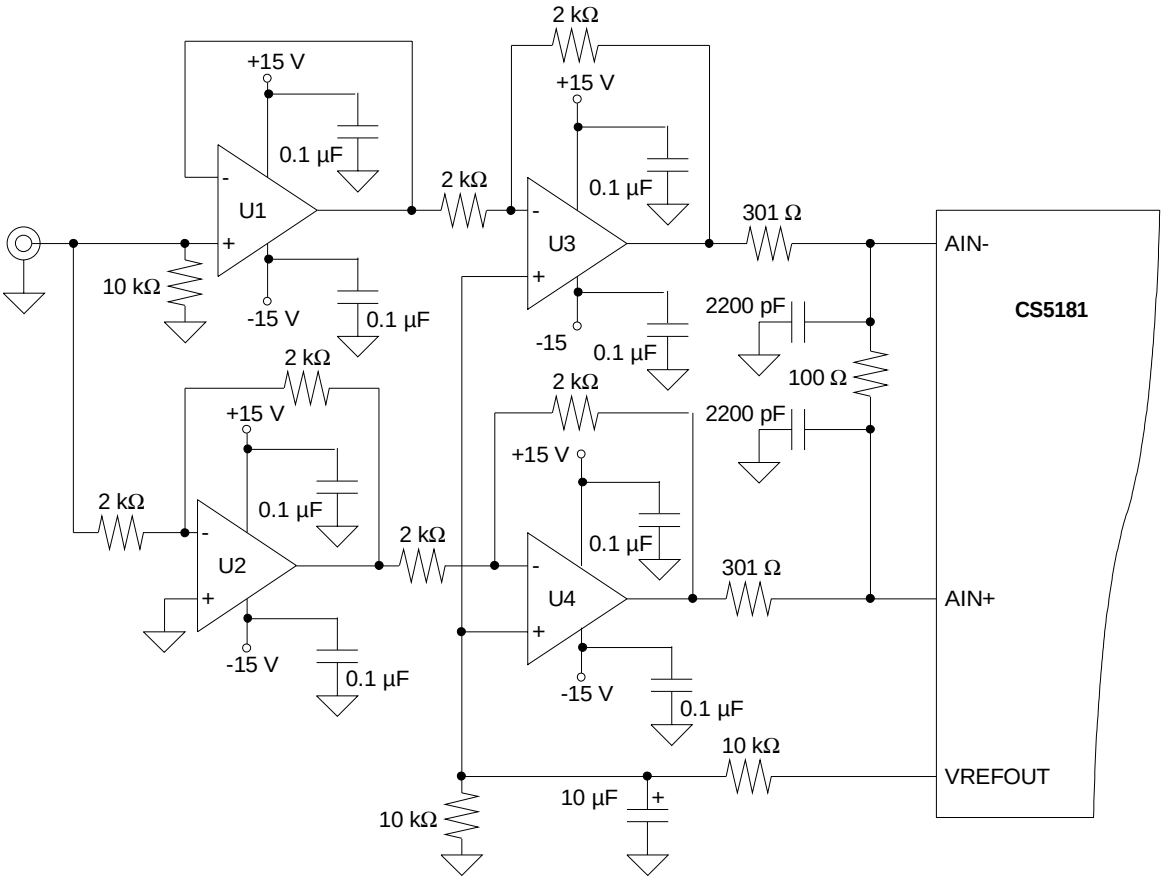


Figure 15. Four amplifier balanced driver.

Figure 15 illustrates a four amplifier circuit which gives the best performance by keeping everything balanced. Performance is generally limited by the amplifiers. Again, the output resistors are used to scale down the input signal. Figures 16 and 17 illustrate the performance of the CS5181 with this amplifier circuit.

Figure 18 illustrates a Differential Non-linearity plot of the converter. Data for the plot was taken using a repeating ramp. Figure 19 is a histogram of the DNL data in Figure 18.

Figure 20 illustrates a noise histogram of the converter with its inputs shorted and connected to a proper common mode voltage.

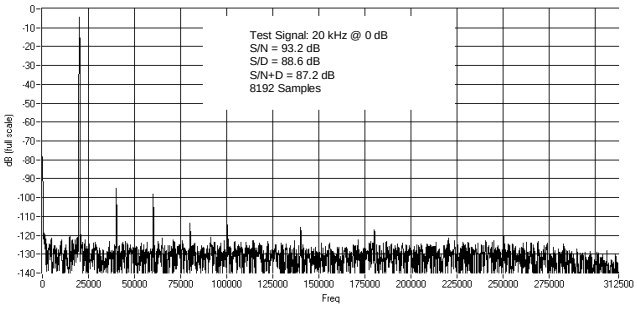


Figure 16. Performance of amplifier in Figure 15

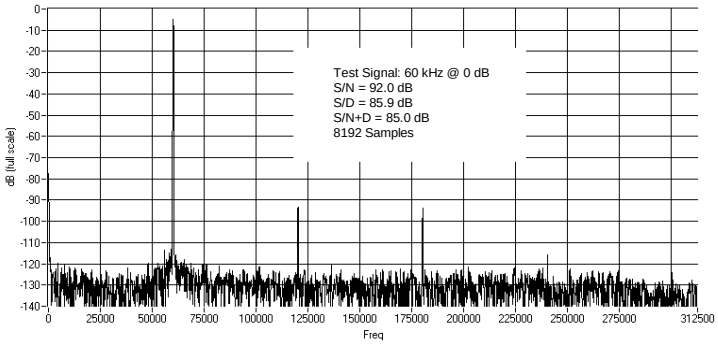


Figure 17. Performance of amplifier in Figure 15

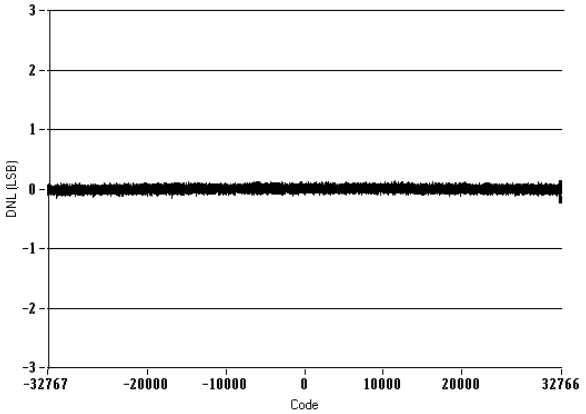


Figure 18. CS5181 Differential Non-linearity plot. (Data taken with repeating ramp)

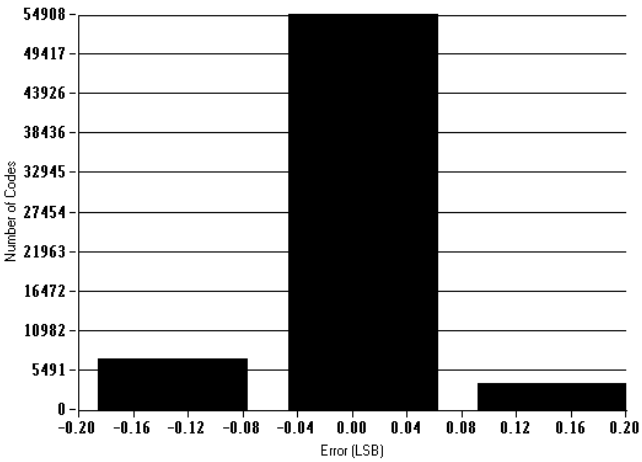


Figure 19. Histogram of DNL from Figure 18

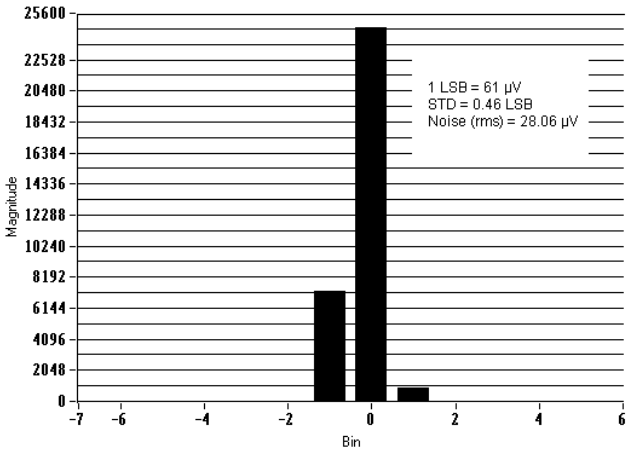
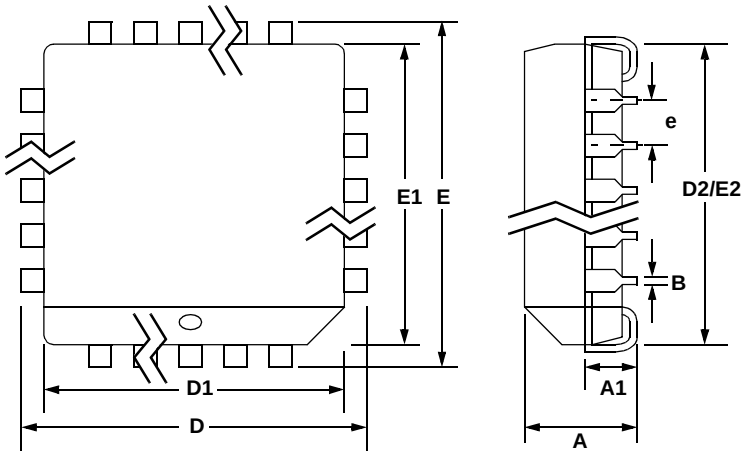


Figure 20. CS5181 Noise Histogram, 32768 samples.

PACKAGE OUTLINE DIMENSIONS

28L PLCC PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.485	0.495	11.883	12.573
D1	0.450	0.456	11.025	11.582
D2	0.390	0.430	9.555	10.922
E	0.485	0.495	11.883	12.573
E1	0.450	0.456	11.025	11.582
E2	0.390	0.430	9.555	10.922
e	0.040	0.060	0.980	1.524

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