A DIVISION OF CIRRUS LOGIC

CS5317

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

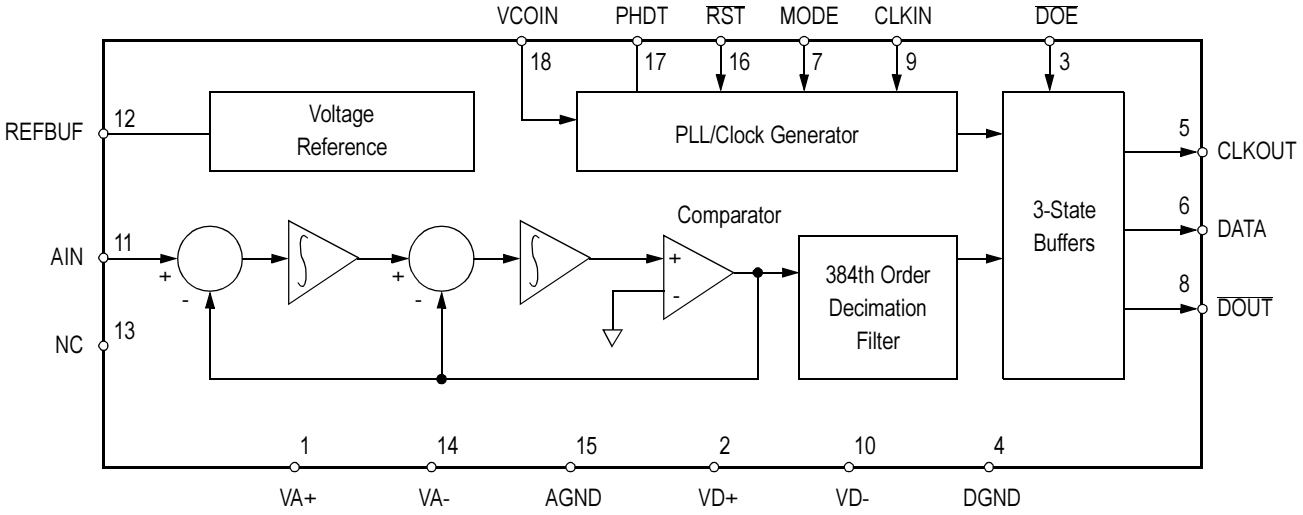
An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION

See page 20.



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ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ - T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%; CLKIN = 4.9152 MHz in CLKOR mode; 1kHz Input Sinewave; with 1.2 kΩ, .01 µF antialiasing filter.)

Parameter*		Min	Typ	Max	Units
Specified Temperature Range			0 to 70		°C
Resolution		16	-	-	Bits
Dynamic Performance					
Dynamic Rnage	(Note 1)	78	84	-	dB
Total Harmonic Distortion		72	80	-	dB
Signal to Intermodulation Distorition		-	84	-	dB
dc Accuracy					
Differential Nonlinearity	(Note2)	-	±0.4	-	LSB
Positive Full-Scale Error		-	±150	-	mV
Positive Full-Scale Drift		-	±500	-	µV/°C
Bipolar Offset Error		-	±10	-	mV
Bipolar Offset Drift		-	±50	-	µV/°C
Filter Characteristics					
Absolute Group Delay	(Note 3)	78.125	-	-	µs
Passband Frequency	(Note 4)	-	5	-	kHz
Input Characteristics					
AC Input Impedance	(1kHz)	-	80	-	kΩ
Analog Input Full Scale Signal Level		±2.75	-	-	V
Power Supplies					
Power Dissipation	(Note5)	-	220	300	mW

Notes:
1. Measured over the full 0 to 9.6kHz band with a -20dB input and extrapolated to full-scale. Since this includes energy in the stopband above 5kHz, additional post-filtering at the CS5317's output can typically achieve 88dB dynamic range by improving rejection above 5kHz. This can be increased to 90dB by bandlimiting the output to 2.5kHz.
2. No missing codes is guaranteed by design.
3. Group delay is constant with respect to input analog frequency; that is, the digital FIR filter has linear phase. Group delay is determined by the formula D_{grp} = 384/CLKIN in CLKOR mode, or 192/CLKOUT in any mode.
4. The digital filter's frequency response scales with the master clock. Its -3dB point is determined by f_{-3dB} = CLKIN/977.3 in CLKOR mode, or CLKOUT/488.65 in any mode.
5. All outputs unloaded. All inputs CMOS levels.

* Refer to the *Parameter Definitions* section after the Pin Description section.

ANALOG CHARACTERISTICS (continued)

Parameter			Min	Typ	Max	Units
Power Supply Rejection	VA+	(Note 6)	-	60	-	dB
	VA-		-	45	-	dB
	VD+		-	60	-	dB
	VD-		-	55	-	dB
Specified Temperature Range			0 to 70			°C
Phase-Lock Loop Characteristics						
VCO Gain Constant, Ko		(Note 7)	-4	-10	-30	Mrad/Vs
VCO Operating Frequency			1.28	-	5.12	MHz
Phase Detector Gain Control, Kd			-3	-8	-12	µA/rad
Phase Detector Prop. Delay		(Note 8)	-	50	100	ns

Notes: 6. With 300mV p-p, 1kHz ripple applied to each supply separately.
7. Over 1.28 MHz to 5.12 MHz VCO output range, where VCO frequency = 2 * CLKOUT.
8. Delay from an input edge to the phase detector to a response at the PHDT output pin.

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ - T_{MAX}; VA+, VD+ = 5V±10%; VA-, VD- = -5V±10%)

All measurements performed under static conditions.

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 9)	V_{OH}	(VD+)-1.0V	-	-	V
Low-Level Output Voltage	I_{OUT} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Note: 9. I_{out}=-100µA. This specification guarantees the ability to drive one TTL load (V_{OH}=2.4V @ I_{out}=-40µA.).

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0V, see Note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Master Clock Frequency		f_{clk}	0.01	-	5.12	MHz

Note: 10. All voltages with respect to ground.

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = T_{MIN}-T_{MAX}; C_L=50 pF; VD+ = 5V±10%; VD- = -5V±10%)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	CLKIN						
	CLKG1 Mode		f_{clkg1}	-	-	20	kHz
	CLKG2 Mode		f_{clkg2}	-	-	10	kHz
	CLKOR Mode		f_{clkor}	-	-	5.12	MHz
Output Word Rate:	DOUT		f_{dout}	-	-	20	kHz
Rise Times:	Any Digital Input		t_{risein}	-	20	1000	ns
	Any Digital Output		$t_{riseout}$	-	15	20	ns
Fall Times:	Any Digital Input		t_{fallin}	-	20	1000	ns
	Any Digital Output		$t_{fallout}$	-	15	20	ns
CLKIN Duty Cycle							
CLKG1 and CKLG2 Modes		Pulse Width Low	t_{pwl1}	200	-	-	ns
		Pulse Width High	t_{pwh1}	200	-	-	ns
CLKOR Mode		Pulse Width Low	t_{pwl1}	45	-	-	ns
		Pulse Width High	t_{pwh1}	45	-	-	ns
RST Pulse Width Low			t_{pwr}	400	-	-	ns
Set Up Times:	RST High to CLKIN High		t_{su1}	40	-	-	ns
	CLKIN High to RST High		t_{su2}	40	-	-	ns
Propagation Delays:							
DOE Falling to Data Valid			t_{phl1}	-	-	150	ns
CLKIN Rising to DOUT Falling		(Note 11)	t_{phl2}	-	1	-	CLKOUT
DOE Rising to Hi-Z Output			t_{plh1}	-	-	80	cycles
CLKOUT Rising to DOUT Falling			t_{plh2}	-	-	60	ns
CLKOUT Rising to DOUT Rising			t_{plh3}	-	-	60	ns
CLKOUT Rising to Data Valid			t_{plh4}	-	-	100	ns
CLKIN Rising to CLKOUT Falling		(Note 12)	t_{plh5}	-	-	200	ns
CLKIN Rising to CLKOUT Rising		(Note 12)	t_{plh6}	-	-	200	ns

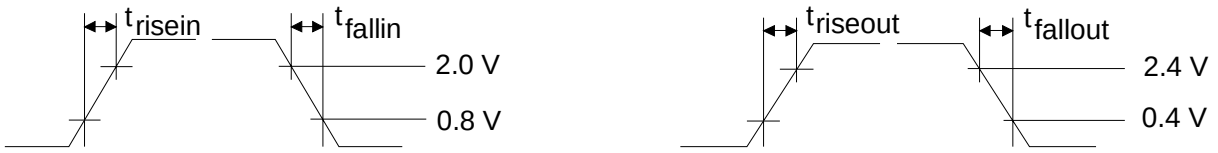
Notes: 11. CLKIN only pertains to CLKG1 and CLKG2 modes.
12. Only valid in CLKOR mode.

ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0V, all voltages with repect to groung)

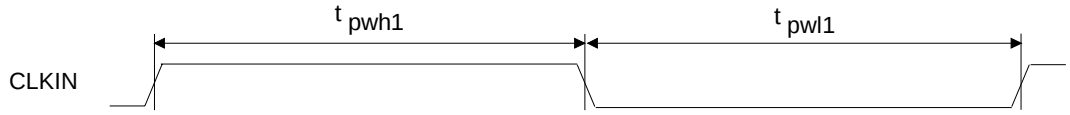
Parameter			Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital		VD+	-0.3	(VA+) + 0.3	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies		(Note 13)	I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)			V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage			V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Notes: 13. Transient currents up to 100mA will not cause SCR latch-up.

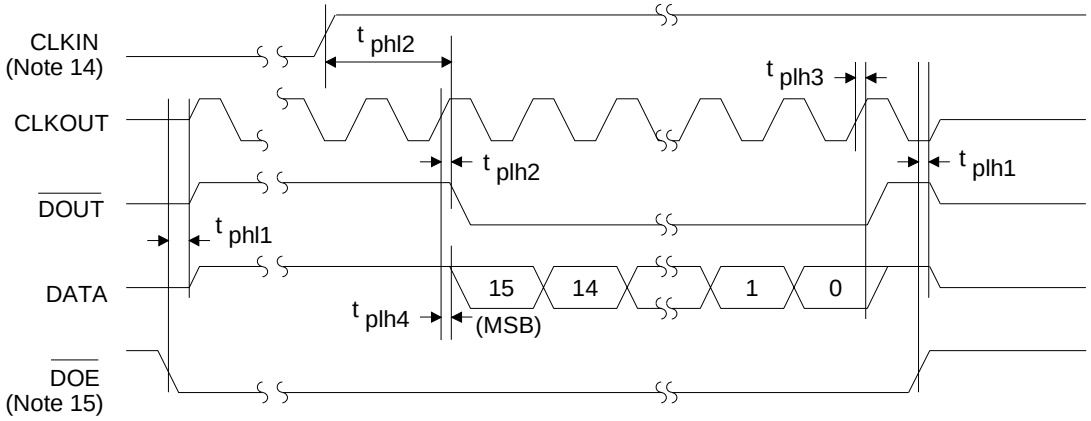
WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.



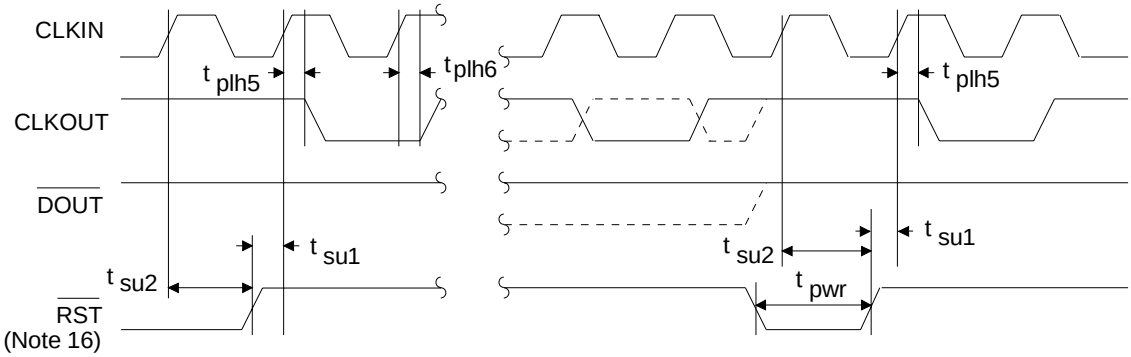
Rise and Fall Times



CLKIN Timing



Serial Output Timing



Reset Timing

Notes: 14. CLKIN only pertains to CLKG1 and CLKG2 modes.
15. If DOE is brought high during serial data transfer, CLKOUT, DOUT, and DATA will immediately 3-state and the rest of the serial data is lost.
16. RST must be held high except in the clock override (CLKOR) mode where it can be used to align the phases of all internal clocks.

GENERAL DESCRIPTION

The CS5317 functions as a complete data conversion subsystem for voiceband signal processing. The A/D converter, sample/hold, voltage reference, and much of the antialiasing filtering are performed on-chip. The CS5317's serial interface offers its 16-bit, 2's complement output in a format which easily interfaces with industry-standard micro's and DSP's.

The CS5317 also includes a phase-locked loop that simplifies the converter's application in systems which require sampling to be locked to an external signal source. The CS5317 continuously samples its analog input at a rate set by an external clock source. On-chip digital filtering, an integral part of the delta-sigma ADC, processes the data and updates the 16-bit output register at up to 20 kHz. The CS5317 can be read at any rate up to 20 kHz.

The CS5317 is a CS5316 with an on-chip sampling clock generator. As such, it replaces the CS5316 and should be considered for all new designs. In addition, a CS5316 look-alike mode is included, allowing a CS5317 to be dropped into a CS5316 socket.

THEORY OF OPERATION

The CS5317 utilizes the delta-sigma technique of executing low-cost, high-resolution A/D conversions. A delta-sigma A/D converter consists of two basic blocks: an analog modulator and a digital filter.

Conversion

The analog modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog negative feedback loop with high open-loop gain. The modulator samples and converts the analog input at a rate well above the bandwidth of interest (2.5 MHz for the CS5317). The modulator's 1-bit output conveys information in the form of duty cycle. The digital filter then processes the 1-bit signal and extracts a high resolution output at a much lower rate (that is, 16-bits at a 20 kHz word rate with a 5 kHz input bandwidth).

An elementary example of a delta-sigma A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty-cycle), which is then filtered (averaged) by the counter for higher resolution. In comparison, the CS5317 uses a more sophisticated multi-order modulator and more powerful FIR filtering to extract higher word rates, much lower noise, and more useful system-level filtering.

Filtering

At the system level, the CS5317's digital filter can be modeled exactly like an analog filter with a few minor differences. First, digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially saturate the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5317's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

An Application Note called "Delta Sigma Overview" contains more details on delta-sigma conversion and digital filtering.

SYSTEM DESIGN WITH THE CS5317

Like a tracking ADC, the CS5317 continuously samples and converts, always tracking the analog input signal and updating its output register at a 20 kHz rate. The device can be read at any rate to create any system-level sampling rate desired up to 20kHz.

Clocking

Oversampling is a critical function in delta-sigma A/D conversion. Although system-level *output* sample rates typically remain between 7kHz and 20kHz in voiceband applications, the CS5317 actually samples and converts the analog input at rates up to 2.56 MHz. This *internal* sampling rate is typically set by a master clock which is on the order of several megahertz. See Table1 for a complete description of the clock relationships in the various CS5317 operating modes.

Some systems such as echo-canceling modems, though, require the *output* sampling rate to be locked to a sampling signal which is 20 kHz or below. For this reason the CS5317 includes an on-chip phase-lock loop (PLL) which can generate its requisite 5.12 MHz master clock from a 20 kHz sampling signal.

The CS5317 features two modes of operation which utilize the internal PLL. The first, termed *Clock Generation 1* (CLKG1), accepts a sampling clock up to 20 kHz at the CLKIN pin and internally generates the requisite 5.12 MHz clock. The CS5317 then processes samples updating its output register at the rate defined at CLKIN, typically 20 kHz. For a 20 kHz clock input the digital filter's 3 dB corner is set at 5.239 kHz, so *CLKG1 provides a factor of 2X oversampling at the system level* (20 kHz is twice the minimum possible sampling frequency needed to reconstruct a 5 kHz input). The CLKG1 mode is initiated by tying the MODE input to +5V.

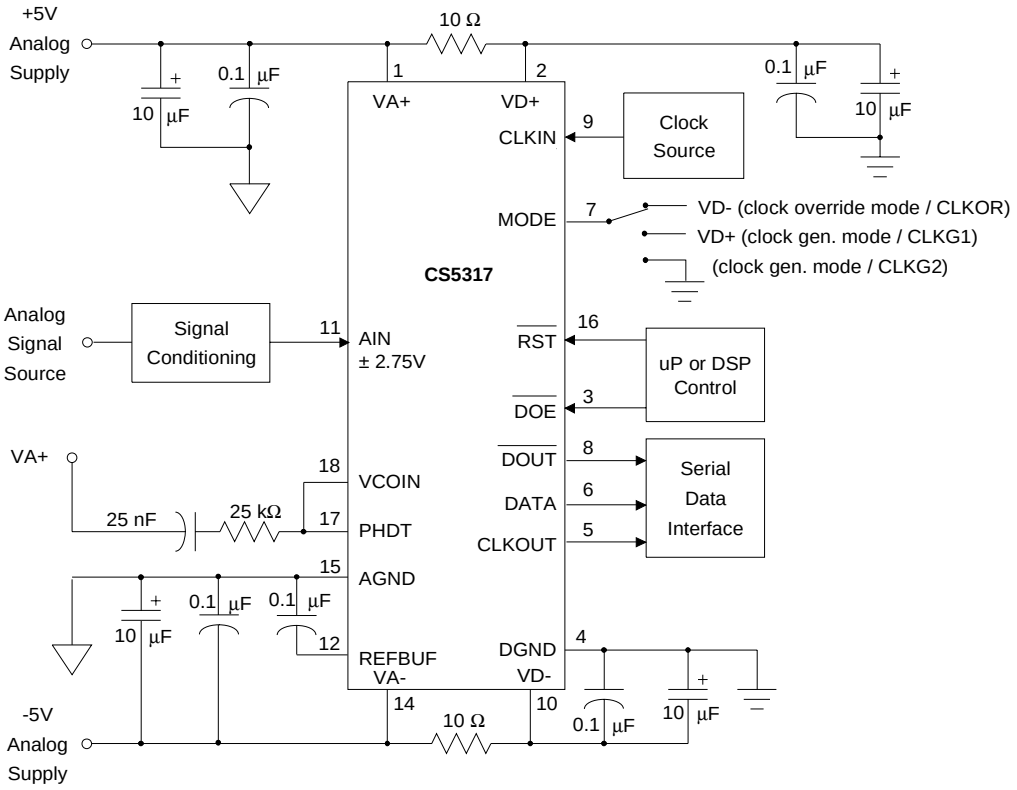


Figure 1. System Connection Diagram with Example PLL Components

Mode	Symbol	Mode Pin	RESET	Output Word Rate Provides System-level 2X Oversampling	CLKIN (kHz)	CLKOUT f_{sin} (MHz)	$\overline{DOUT}$ f_{sout} (kHz)	F (kHz)	t_{dcD}* (ns)
Clock Gen. 2	CLKG2 CLKG2 CLKG2	0V	HIGH	NO	7.2 9.6 10.0 (max)	1.8432 2.4576 2.56	7.2 9.6 10.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Gen. 1	CLKG1 CLKG1 CLKG1	+5V	HIGH	YES	14.4 19.2 20.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Override	CLKOR CLKOR CLKOR	-5V	SYNC	YES	3686.4 4915.2 5120.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	N/A N/A N/A
CS5316	CS5316	FSYNC	LOW	YES	5120.0 (max)	2.56	20.0	20.0	N/A

* t_{dcD} - Delay from CLKIN rising to $\overline{DOUT}$ falling = 1 CLKOUT cycle

Table 1. Mode Comparisons

The second PLL mode is termed *Clock Generation 2* (CLKG2) which generates its 5.12 MHz clock from a *10 kHz* external sampling signal. Again, output samples are available at the system sampling rate set by CLKIN, typically 10 kHz. For the full-rated 10 kHz clock CLKG2 still sets the filter's 3 dB point at 5 kHz. Therefore, *CLKG2 provides no oversampling* beyond the Nyquist requirement at the system level (10 kHz : 5 kHz) and its internal digital filter provides little anti-aliasing value. The CLKG2 mode is initiated by grounding the MODE pin.

The CS5317 features a third operating mode called *Clock Override* (CLKOR). Initiated by tying the MODE pin to -5V, CLKOR allows the 5.12 MHz master clock to be driven directly into the CLKIN pin. The CS5317 then processes samples updating its output register at $f_{clkin}/256$. Since all clocking is generated internally, the CLKOR mode includes a *Reset* capability which allows the output samples of multiple CS5317's to be synchronized.

The CS5317 also has a CS5316 compatible mode, selected by tying $\overline{RST}$ low, and using MODE (pin 7) as the FSYNC pin. See the CS5316 data sheet for detailed timing information.

Analog Design Considerations

DC Characteristics

The CS5317 was designed for signal processing. Its analog modulator uses CMOS amplifiers resulting in offset and gain errors which drift over temperature. If the CS5317 is being considered for low-frequency (< 10 Hz) measurement applications, Crystal Semiconductor recommends the CS5501, a low-cost, d.c. accurate, delta-sigma ADC featuring excellent 60 Hz rejection and a system-level calibration capability.

The Analog Input Range and Coding Format

The input range of the CS5317 is nominally ± 3V, with ± 250 mV possible gain error. Because of this gain error, analog input levels should be kept below ± 2.75V. The converter's serial output appears MSB-first in 2's complement format.

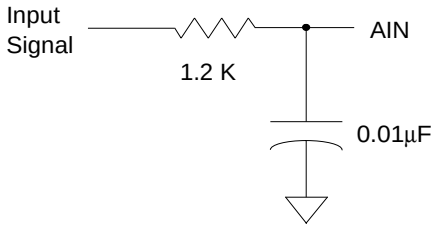
Antialiasing Considerations

In applying the CS5317, aliasing occurs during both the initial sampling of the analog input at $f_{s_{in}}$ (~2.5 MHz) and during the digital decimation process to the 16-bit output sample rate, $f_{s_{out}}$.

Initial Sampling

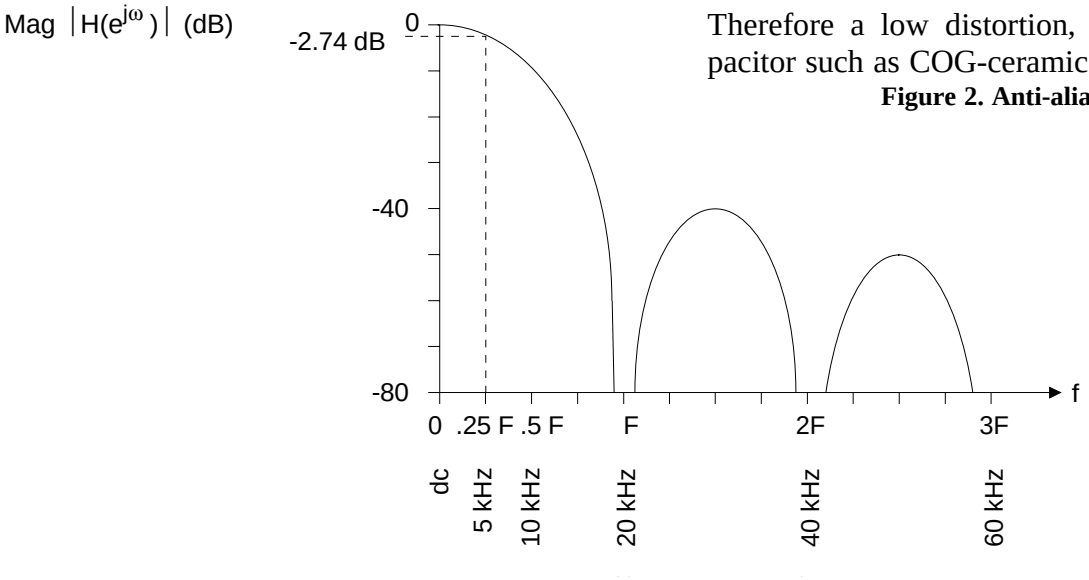
The CS5317 samples the analog input, AIN, at one-half the master clock frequency (~2.5 MHz max). The input sampling frequency, $f_{s_{in}}$, appears at CLKOUT regardless of whether the master clock is generated on-chip (CLKG1 and CLKG2 modes) or driven directly into the CS5317 (CLKOR mode). The digital filter then processes the input signal at the input sample rate.

Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate, $f_{s_{in}}$. That is, when the CS5317 is operating at its full-rated speed any noise within ± 5 kHz bands around 2.5 MHz, 5 MHz, 7.5 MHz, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled*. Since the signal is heavily oversampled (2.5 MHz : 5 kHz, or 500 : 1), a single-pole passive RC filter can be used as shown in Figure 2.



Note: Any nonlinearities contributed by this filter will be encoded as distortion by the CS5317. Therefore a low distortion, high frequency capacitor such as COG-ceramic is recommended.

Figure 2. Anti-alias Filter



$$\left|\left(\frac{\sin(128\pi f T)}{128\sin(\pi f T)}\right)^3\right| =$$ Magnitude where: $T = 1/f_{sin}$

f_{sin} = input sampling frequency = CLKOUT frequency for all modes
= CLKIN/2 in CLKOR mode
= CLKIN*128 in CLKG1 mode
= CLKIN*256 in CLKG2 mode

$F = f_{sin}/128$ for all modes

f = input frequency

$f_{sout} = f_{sin}/128$ = output data rate for CLKOR & CLKG1 = F

$f_{sout} = f_{sin}/256$ = output data rate for CLKG2 = F/2

Examples:
For f_{sin} = 2.56 MHz at f = 5 kHz: Magnitude is -2.74 dB
For f_{sin} = 2.56 MHz at f = 10 kHz: Magnitude is -11.8 dB

Figure 3. CS5317 Low-Pass Filter Response

Decimation

Aliasing effects due to decimation are identical in the CLKOR and CLKG1 modes. Aliasing is different in the CLKG2 mode due to the difference in output sample rates (10 kHz vs. 20 kHz) and thus will be discussed separately.

Aliasing in the CLKOR and CLKG1 Modes

The delta-sigma modulator output is fed into the digital low-pass filter at the input sampling rate, $f_{s_{in}}$. The filter's frequency response is shown in Figure 3. In the process of filtering the digitized signal the filter *decimates* the sampling rate by 128 (that is, $f_{s_{out}} = f_{s_{in}}/128$). In its most elementary form, decimation simply involves ignoring - or selectively reading - a fraction of the available samples.

In the process of decimation the output of the digital filter is effectively *resampled* at $f_{s_{out}}$, the output word rate, *which has aliasing implications*. Residual signals *after filtering* at multiples of $f_{s_{out}}$ will alias into the baseband. For example, an input tone at 28 kHz will be attenuated by 39.9 dB. If $f_{s_{out}}$ = 20 kHz, the residual tone will alias into the baseband and appear at 8 kHz in the output spectrum.

If the input signal contains a large amount of out-of-band energy, additional analog and/or digital antialias filtering may be required. If digital post-filtering is used to augment the CS5317's rejection above $f_{s_{out}}/4$ (that is, above 5 kHz), the filtering will also reject residual quantization noise from the modulator. This will typically increase the converter's dynamic range to 88 dB. Further bandlimiting the digital output to $f_{s_{out}}/8$ (2.5 kHz at full speed) will typically increase dynamic range to 90 dB.

Aliasing in the CLKG2 Mode

Aliasing effects in the CLKG2 mode can be modeled exactly as those in the CLKG1 mode with the output decimated by two (from 20 kHz to 10 kHz). This is most easily achieved by ignoring every other sample. In the CLKG2 mode the ratio of the output sampling rate to the filter's -3 dB point is two, with no oversampling beyond the demands of the Nyquist criterion. Without the ability to roll-off substantially before $f_{s_{out}}/2$, the on-chip digital filter's antialiasing value is diminished.

The CLKG2 mode should therefore be used only when the output data rate must be minimized due to communication and/or storage reasons. In addition, adequate analog filtering must be provided prior to the A/D converter.

Digital Design Considerations

The CS5317 presents its 16-bit serial output MSB-first in 2's complement format. The converter's serial interface was designed to easily interface to a wide variety of micro's and DSP's. Appendix A offers several hardware interfaces to industry-standard processors.

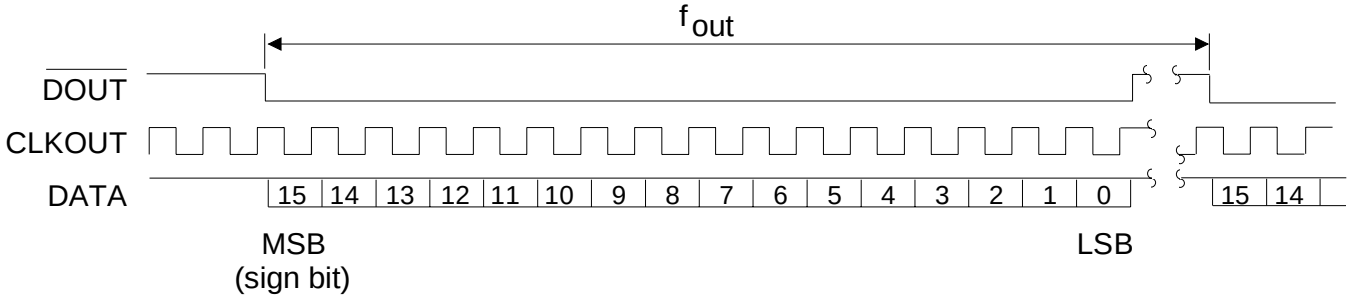


Figure 4. Data Output

Data Output Characteristics & Coding Format

As shown in Figure 4, the CS5317 outputs its 16-bit data word in a serial burst. The data appears at the DATA pin on the rising edge of the same CLKOUT cycle in which $\overline{DOUT}$ falls. Data changes on the rising edge of CLKOUT, and can be latched on the falling edge. The CLKOUT rate is set by the CLKIN input ($f_{clkin}/2$ in the CLKOR mode; f_{clkin}*128 in the CLKG1 mode; and f_{clkin}*256 in the CLKG2 mode). $\overline{DOUT}$ returns high after the last bit is transmitted. After transmitting the sixteen data bits, DATA will remain high until $\overline{DOUT}$ falls again, initiating the next data output cycle.

A 3-state capability is available for bus-oriented applications. The 3-state control input is termed Data Output Enable, $\overline{DOE}$, and is asynchronous with respect to the rest of the CS5317. If $\overline{DOE}$ is taken high at any time, even during a data burst, the DATA, $\overline{DOUT}$ and CLKOUT pins go to a high impedance state. Any data which would be output while $\overline{DOE}$ is high is lost.

Power Supplies

Since the A/D converter's output is digitally filtered in the CS5317, the device is more forgiving and requires less attention than conventional 16-bit A/D converters to grounding and layout arrangements. Still, care must be taken at the design and layout stages to apply the device properly. The CS5317 provides separate analog and digital power supply connections to isolate digital noise from its analog circuitry. Each supply pin should be decoupled to its respective ground, AGND or DGND. Decoupling should be accomplished with 0.1 µF ceramic capacitors. If significant low frequency noise is present in the supplies, 10 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5317 must never exceed the positive analog supply by more than a diode drop or the chip could be permanently damaged. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. Figure 1 shows a decoupling scheme which allows the CS5317 to be powered from a single set of ± 5V rails. The digital supplies are derived from the analog supplies through 10 Ω resistors to prevent the analog supply from dropping below the digital supply.

PLL Characteristics

A phase-locked loop is included on the CS5317 and is used to generate the requisite high frequency A/D sampling clock. A functional diagram of the PLL is shown in Figure 5. The PLL consists of a phase detector, a filter, a VCO (voltage-controlled oscillator), and a counter/divider. The phase detector inputs are CLKIN (θ_1) and a sub-multiple of the VCO output signal (θ_2). The inputs to the phase detector are positive-edge triggered and therefore the duty cycle of the CLKIN signal is not significant. With this type of phase detector, the lock range of the PLL is equal to the capture range and is independent of the low pass filter. The output of the phase detector is input to an external low pass filter. The filter characteristics are used to determine the transient response of the loop. The output voltage from the filter functions as the input control voltage to the VCO. The output of the VCO is then divided in frequency to provide an input to the phase detector. The clock divider ratio is a function of the PLL mode which has been selected.

Phase Detector Gain (Kd)

A properly designed and operating phase-locked loop can be described using steady state linear analysis. Once in frequency lock, any phase difference between the two inputs to the phase detector cause a current output from the detector during the phase error. While either the +50 µA or the -50 µA current source may be turned on, the average current flow is:

$$i_{out_{avg}} = Kd(\theta_1 - \theta_2) \approx (-50\mu A/2\pi)\ (\theta_1 - \theta_2)$$

where θ_1 is the phase of IN1, θ_2 is the phase of IN2 and Kd is the phase detector gain. The factor 2π comes from averaging the current over a full CLKIN cycle. Kd is in units of micro-amperes/radian.

VCO Gain (Ko)

The output frequency from the VCO ranges from 1.28 MHz to 5.12 MHz. The frequency is a function of the control voltage input to the VCO. The VCO has a negative gain factor, meaning that as the control voltage increases more positively the output frequency decreases. The gain factor units are Megaradians per Volt per Second. This is equivalent to 2π Megahertz per volt. Changes in output frequency are given by:

$$\Delta\omega_{vco} = Ko\ \Delta VCO_{in} \quad [Ko \text{ is typ. } -10Mrad/Vs.]$$

Counter/Divider Ratio

The CS5317 PLL multiplies the CLKIN rate by an integer value. To set the multiplication rate, a counter/divider chain is used to divide the VCO output frequency to develop a clock whose frequency is compared to the CLKIN frequency in the phase detector. The binary counter/divider ratio sets the ratio of the VCO frequency to the CLKIN frequency. As illustrated in Figure 5, the VCO output is always divided by two to yield the CLKOUT signal which is identical in frequency to the delta-sigma modulator sampling clock. The CLKOUT signal is then further divided by either 128 in the CLKG1 mode or by 256 in the CLKG2 mode. When the divide by two stage is included, the divider ratio (N) for the PLL in the CLKG1 mode is effectively 256. In the CLKG2 mode the divider ratio (N) is 512.

Loop Transfer Function

As the phase-locked loop is a closed loop system, an equation can be determined which describes its closed loop response. Using the gain factors for the phase detector and the VCO, the filter arrangement and the counter/divider constant N, analysis will yield the following equation which describes the transfer function of the PLL:

$$\frac{\theta_2}{\theta_1} = \frac{\frac{KoKdR}{N}s + \frac{KoKd}{NC}}{s^2 + \frac{KoKdR}{N}s + \frac{KoKd}{NC}}$$

This equation may be rewritten such that its elements correspond with the following

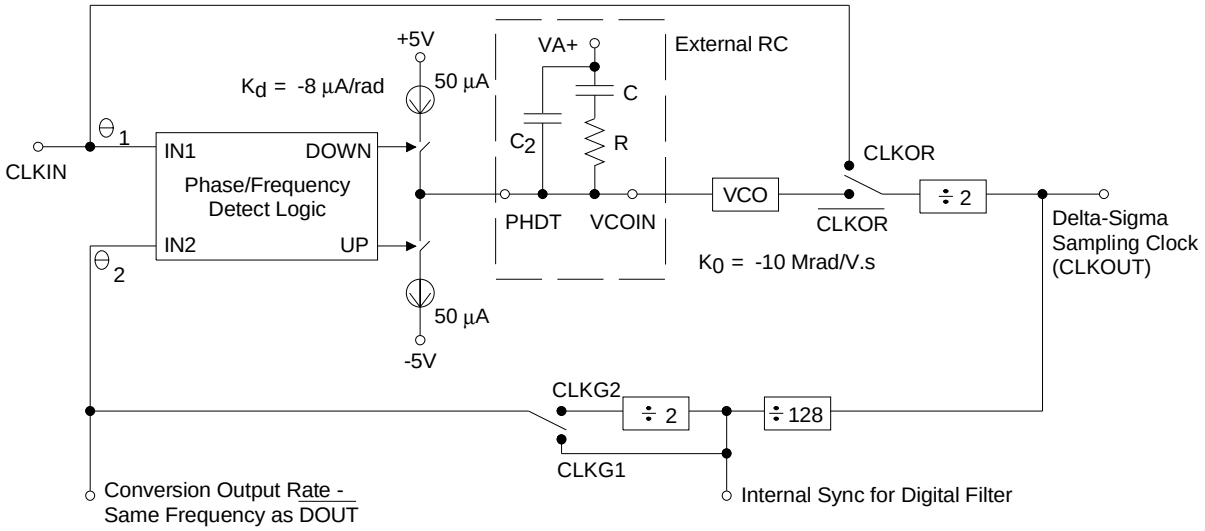


Figure 5. PLL Functional Diagram

characteristic form in which the damping factor, ζ, and the natural frequency, ω_n , are evident:

$$\frac{\theta_2}{\theta_1} = \frac{2\zeta\omega_n s + \omega_n{}^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}$$

Both the natural frequency and the damping factor are particularly important in determining the transient response of the phase-locked loop when subjected to a step input of phase or frequency. A family of curves are illustrated in Figure 6 that indicate the overshoot and stability of the loop as a function of the damping factor. Each response is plotted as a function of the normalized time, ω_n t. For a given ζ and lock time, t, the ω_n required can be determined. Alternatively, phase lock control loop bandwidth may be a specified parameter. In some systems it may be desirable to reduce the -3dB bandwidth of the PLL control loop to reduce the effects of jitter in the phase of the input clock. The 3 dB bandwidth of the PLL control loop is defined by the following equation:

$$\omega_{3dB} = \omega_n\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

The equations used to describe the PLL and the 3 dB bandwidth are valid only if the frequency of CLKIN is approximately 20 times greater than the 3 dB corner frequency of the control loop.

Filter Components

Using the equations which describe the transfer function of the PLL system, the following external filter component equations can be determined:

$$C = \frac{KoKd}{N\omega_n{}^2}$$

$$R = 2\zeta\omega_n \frac{N}{KoKd}$$

The gain factors (Ko, Kd) are specified in the Analog Characteristics table. In the event the system calls for very low bandwidth, hence a corresponding reduction in loop gain, the phase detector gain factor Kd can be reduced. A large series resistor (R1) can be inserted between the output of the detector and the filter. Then the 50 µA current sources will saturate to the supplies and yield the following gain factor:

$$Kd \approx \frac{-5V}{2\pi R_1}$$

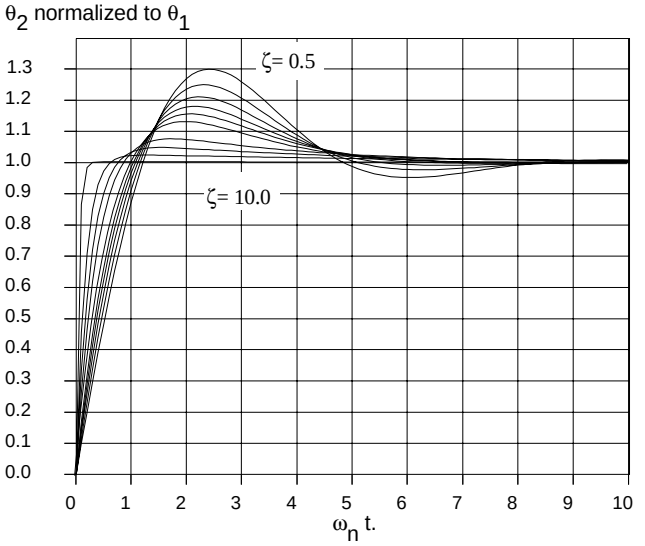


Figure 6a. θ_2 Unit Step Response

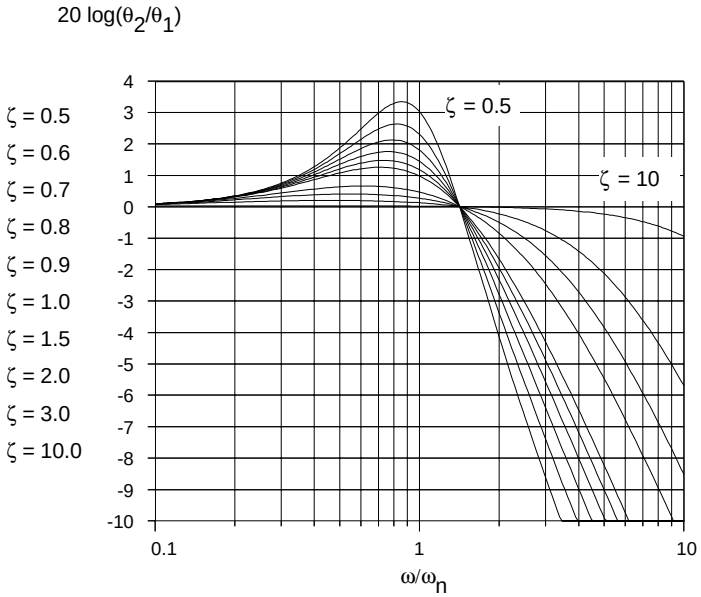


Figure 6b. Second Order PLL Frequency Response

In some applications additional filtering may be useful to eliminate any jitter associated with the discrete current pulses from the phase detector. In this case a capacitor whose value is no more than 0.1 C can be placed across the RC filter network (C_2 in Figure 5).

Filter Design Example

The following is a step by step example of how to derive the loop filter components. The CS5317 A/D sampling clock is to be derived from a 9600 Hz clock source. The application requires the signal passband of the CS5317 to be 4 kHz. The on-chip digital filter of the CS5317 has a 3 dB passband of CLKOUT/488.65 (see Note 4 in the data sheet specifications tables). The 4 kHz passband requirement dictates that the sample clock (CLKOUT) of the CS5317 be a minimum of 4000 X 488.65 = 1.954 MHz. This requires the VCO to run at 3.908 MHz. The 3.908 MHz rate is 407 times greater than the 9600 Hz PLL input clock. Therefore the CS5317 must be set up in mode CLKG2 with N = 512. If the CLKG1 mode were used (N = 256), too narrow of a signal bandwidth through the A/D would result.

Once the operating mode has been determined from the system requirements, a value for the damping factor must be chosen. Figure 6 illustrates the dynamic aspects of the system with a given damping factor. Damping factor is generally chosen to be between 0.5 and 2.0. The choice of 0.5 will result in an overshoot of 30 % to a step response whereas the choice of 2.0 will result in an overshoot of less than 5 %. For example purposes, let us use a damping factor of 1.0.

So, let us begin with the following variables :

Ko = - 10 Mradians/volt.sec
Kd = - 8 μA/radian
N = 512
$\zeta = 1.0$

To calculate values for the resistor R and capacitor C of the filter, we must first derive a value for ω_n. Using the general rule that the sample clock should be at least 20 times higher frequency than the 3dB bandwidth of the PLL control loop:

$CLKIN \geq 20\ \omega_{3dB}$

where CLKIN = 9600 Hz $= 2\pi\ 9600$ radians/sec.

So: $\omega_{3dB} = 2\pi\ 9600/20 = 3016$ radians/sec.

Knowing ω_{3dB} and the damping factor of 1.0, we can calculate the natural frequency, ω_n , of the control loop:

$$\omega_n = \omega_{3dB}\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

$$\omega_n = 3016\ \sqrt{2(1)^2 + 1 + \sqrt{(2(1)^2 + 1)^2 + 1}}$$

$$\omega_n = 1215 \quad 1/\text{sec}$$

Once the natural frequency, ω_n , is determined, values for R and C for the loop filter can be calculated:

$R = 2\zeta\omega_n N/KoKd$

$R = 2(1)(1215\ 1/s)\ 512/(-10\text{Mrad/v.s.})(-8\ \mu A/rad)$

$R = 15552\ v/A = 15.55\ k\Omega$. Use R = 15 kΩ.

$C = KoKd/N\omega_n^2$

$C = (-10\ \text{Mrad/v.s})(-8\ \mu A/rad)/512\ (1215\ 1/s)^2$

$C = 105.8 \times 10^{-9}\ A.s/v = 105\ nF$. Use 0.1 μF.

The above example assumed typical values for Ko and Kd. Your application may require a worst case analysis which includes the minimum or maximum values. Table 2 shows some other example situations and R and C values.

CLKIN (Hz)	Mode	N	CLKOUT (MHz)	ζ	ω3dB	ωn	R * (kΩ)	C * (nF)
7200	CLKG2	512	1.8432	1.0	2262	911	11.6	187
9600	CLKG2	512	2.4576	1.0	3016	1215	15.5	106
14400	CLKG1	256	1.8432	1.0	4524	1822	11.6	94
19200	CLKG1	256	2.4576	1.0	6032	2430	15.5	52

* The values for R and C are as calculated using the described method. Component tolerances have not been allowed for. Notice that Ko and Kd can vary over a wide range, so using tight tolerances for R and C is not justified. Use the nearest conveniently available value.

Table 2 Example PLL Loop Filter R and C values

CS5317 PERFORMANCE

The CS5317 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the CS5317.

FFT Tests and Windowing

The CS5317 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the CS5317 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5317.

If sampling is not synchronized to the input sinewave it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the CS5317 has a maximum side-lobe level of -92 dB.

Figure 7 shows an FFT plot of a typical CS5317 with a 1 kHz sinewave input generated by an "ultra-pure" sine wave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

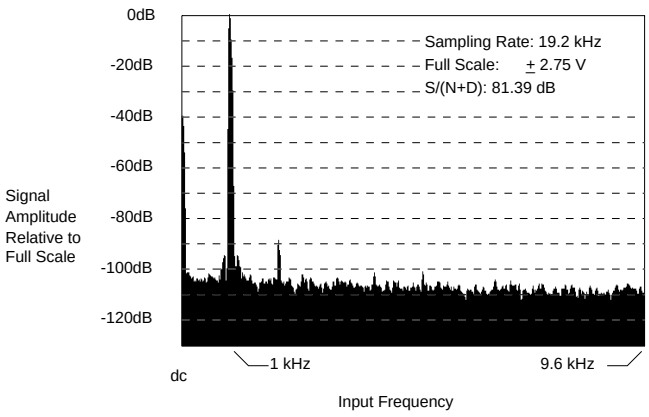


Figure 7. CS5317 Dynamic Performance

Full - scale signal - to - noise - plus - distortion [S/(N+D)] is calculated as the ratio of the rms power of the fundamental to the sum of the rms power of the FFT's other frequency bins, which include both noise and distortion. For the CS5317, signal-to-noise-plus-distortion is shown to be better than 81 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

Harmonic distortion characteristics of the CS5317 are excellent at 80 dB full scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation distortion of two or more input frequencies by a non-linear transfer function.

DNL Test

Figure 9 shows a plot of the typical differential non-linearity (DNL) of the CS5317. This test is done by taking a large number of conversion results, and counting the occurrences of each code. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the DNL test, a code with the average number of occurrences is considered ideal and plotted as DNL = 0 LSB. A code with more or less occurrences than average will appear as a DNL of greater than or less than zero. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

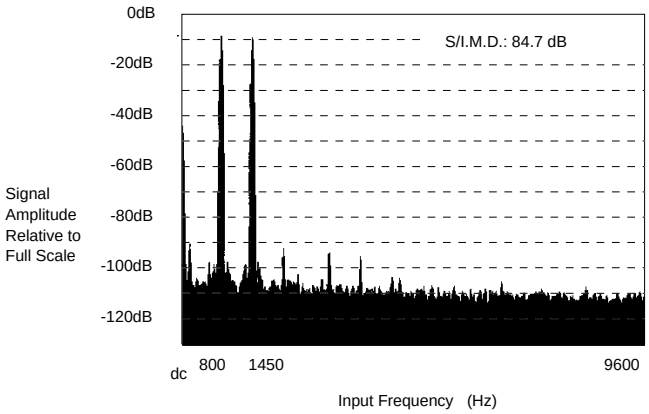


Figure 8. CS5317 Intermodulation Distortion

The plot below illustrates the typical DNL performance of the CS5317, and clearly shows the part easily achieves no missing codes.

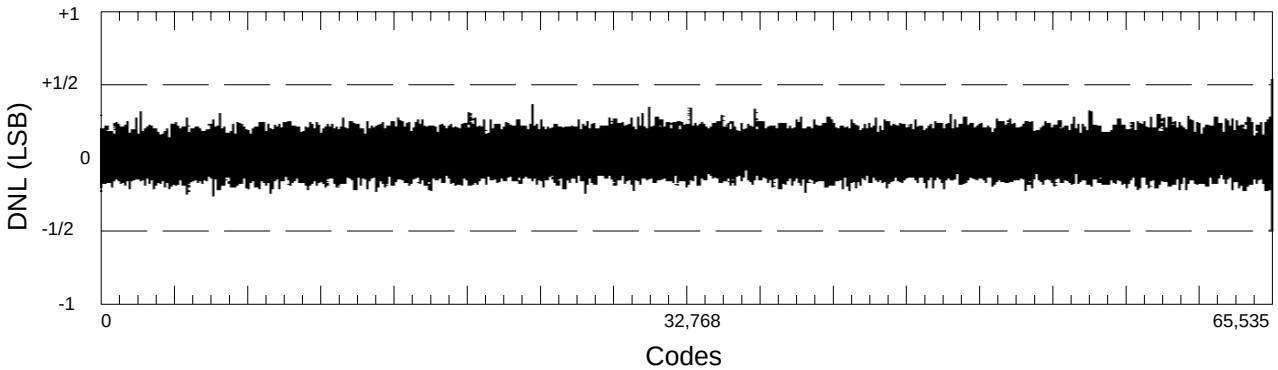
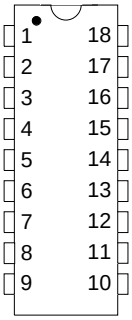


Figure 9. CS5317 DNL Plot

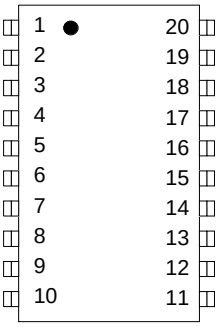
PIN DESCRIPTIONS (Pin numbers refer to the 18-pin DIP package)

18 pin DIP Pinout



POSITIVE ANALOG POWER	**VA+**	1	18	**VCOIN**	VCO INPUT
POSITIVE DIGITAL POWER	**VD+**	2	17	**PHDT**	PHASE DETECT
DATA OUTPUT ENABLE	**DOE**	3	16	**RST**	RESET
DIGITAL GROUND	**DGND**	4	15	**AGND**	ANALOG GROUND
SERIAL CLOCK OUTPUT	**CLKOUT**	5	14	**VA-**	NEGATIVE ANALOG POWER
SERIAL DATA OUTPUT	**DATA**	6	13	**NC**	NO CONNECT
CLOCKING MODE SELECT	**MODE**	7	12	**REFBUF**	POSITIVE REFERENCE BUFFER
DATA OUTPUT READY	**DOUT**	8	11	**AIN**	ANALOG INPUT
CLOCK INPUT	**CLKIN**	9	10	**VD-**	NEGATIVE DIGITAL POWER

20 pin SOIC pinout



POSITIVE ANALOG POWER	**VA+**	1	20	**VCOIN**	VCO INPUT
POSITIVE DIGITAL POWER	**VD+**	2	19	**PHDT**	PHASE DETECT
DATA OUTPUT ENABLE	**DOE**	3	18	**RST**	RESET
DIGITAL GROUND	**DGND**	4	17	**AGND**	ANALOG GROUND
NO CONNECT	**NC**	5	16	**NC**	NO CONNECT
SERIAL CLOCK OUTPUT	**CLKOUT**	6	15	**NC**	NO CONNECT
SERIAL DATA OUTPUT	**DATA**	7	14	**VA-**	NEGATIVE ANALOG POWER
CLOCKING MODE SELECT	**MODE**	8	13	**REFBUF**	POSITIVE REFERENCE BUFFER
DATA OUTPUT READY	**DOUT**	9	12	**AIN**	ANALOG INPUT
CLOCK INPUT	**CLKIN**	10	11	**VD-**	NEGATIVE DIGITAL POWER

Power Supplies

VD+ - Positive Digital Power, PIN 2.
Positive digital supply voltage. Nominally 5 volts.

VD- - Negative Digital Power, PIN 10.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 4.
Digital ground reference.

VA+ - Positive Analog Power, PIN 1.
Positive analog supply voltage. Nominally 5 volts.

VA- - Negative Analog Power, PIN 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 15.
Analog ground reference.

PLL/Clock Generator

CLKIN - Clock Input, PIN 9.
Clock input for both clock generation modes and the clock override mode (see MODE).

MODE - Mode Set, PIN 7.

Determines the internal clocking mode utilized by the CS5317. Connect to +5V to select CLKG1 mode. Connect to DGND to select CLKG2 mode. Connect to -5V to select CLKOR mode. This pin becomes equivalent to FSYNC in the CSZ5316 compatible mode.

VCOIN - VCO Input, PIN 18.

This pin is typically connected to PHDT. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

PHDT - Phase Detect, PIN 17.

This pin is typically connected to VCOIN. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

Inputs

AIN - Analog Input, PIN 11.

$\overline{\text{DOE}}$ - Data Output Enable, PIN 3.

Three-state control for serial output interface. When low, DATA, $\overline{\text{DOUT}}$, and CLKOUT are active. When high, they are in a high impedance state.

$\overline{\text{RST}}$ - Sample Clock Reset, PIN 16.

Sets phase of CLKOUT. Functions only in the clock override mode, CLKOR. Used to synchronize the output samples of multiple CS5317's. Must be kept high in CLKG1 or CLKG2 modes. Also, tying this pin low, with MODE not tied to - 5V, will place the CS5317 into CSZ5316 compatible mode.

Outputs

$\overline{\text{DOUT}}$ - Data Output Flag, PIN 8.

The falling edge indicates the start of serial data output on the DATA pin. The rising edge indicates the end of serial data output.

DATA - Data Output, PIN 6.

Serial data output pin. Converted data is clocked out on this pin by the rising edge of CLKOUT. Data is sent MSB first in two's complement format.

CLKOUT - Data Output Clock, PIN 5.

Serial data output clock. Data is clocked out on the rising edge of this pin. The falling edge should be used to latch data. Since CLKOUT is a free running clock, $\overline{\text{DOUT}}$ can be used to indicate valid data.

REFBUF - Positive Voltage Reference Noise Buffer, PIN 12.

Used to attenuate noise on the internal positive voltage reference. Must be connected to the analog ground through a 0.1µF ceramic capacitor.

PARAMETER DEFINITIONS

Resolution - The number of different output codes possible. Expressed as N, where 2^N is the number of available output codes.

Dynamic Range - The ratio of the largest allowable input signal to the noise floor.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

Signal to Intermodulation Distortion - The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Positive Full Scale Error - The deviation of the last code transition from the ideal, (VREF - 3/2 LSB). Units in mV.

Positive Full Scale Drift - The drift in effective, positive, full-scale input voltage with temperature.

Negative Full Scale Error - The deviation of the first code transition from the ideal, (-VREF + 1/2 LSB). Units in mV.

Negative Full Scale Drift - The drift in effective, negative, full-scale input voltage with temperature.

Bipolar Offset - The deviation of the mid-scale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

Bipolar Offset Drift - The drift in the bipolar offset error with temperature.

Absolute Group Delay - The delay through the filter section of the part.

Passband Frequency - The upper -3 dB frequency of the CS5317.

ORDERING GUIDE

Model Number	Temperature Range	Package
CS5317-KP	0 to 70°C	18 Pin Plastic DIP
CS5317-KS	0 to 70°C	20 Pin Plastic SOIC

APPENDIX A
APPLICATIONS

Figure A1 shows one method of converting the serial output of the CS5317 into 16-bit, parallel words. The associated timing is also shown.

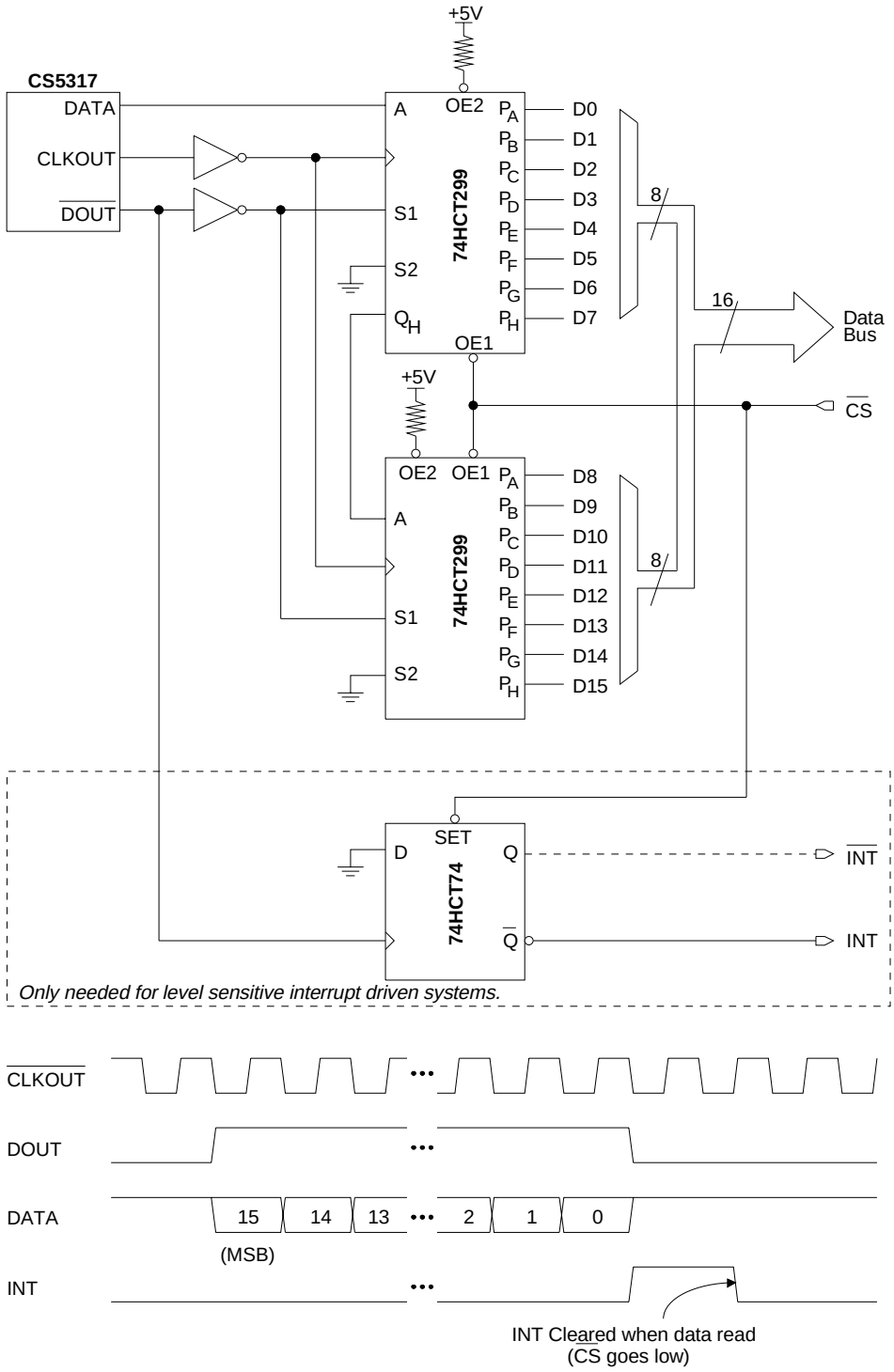


Figure A1. CS5317-to-Parallel Data Bus Interface

Figure A2 shows the interconnection and timing details for connecting a CS5317 to a NEC μPD7730 DSP chip.

Figure A3 shows the interconnection and timing details for connecting a CS5317 to a Motorola DSP 56000.

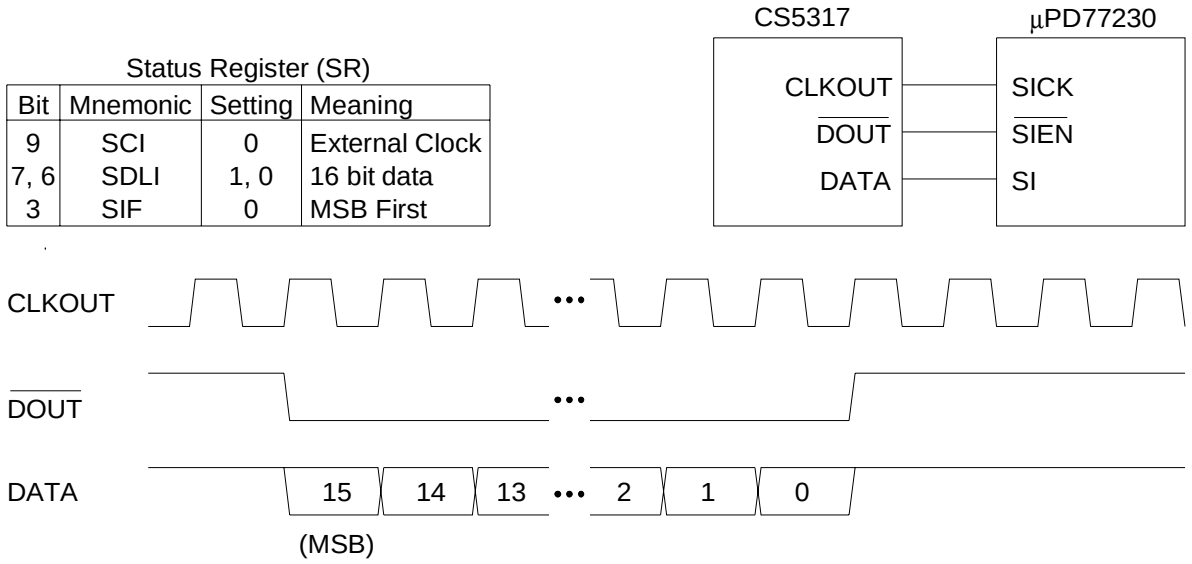


Figure A2. CS5317-to-NEC μPD77230 Serial Interface

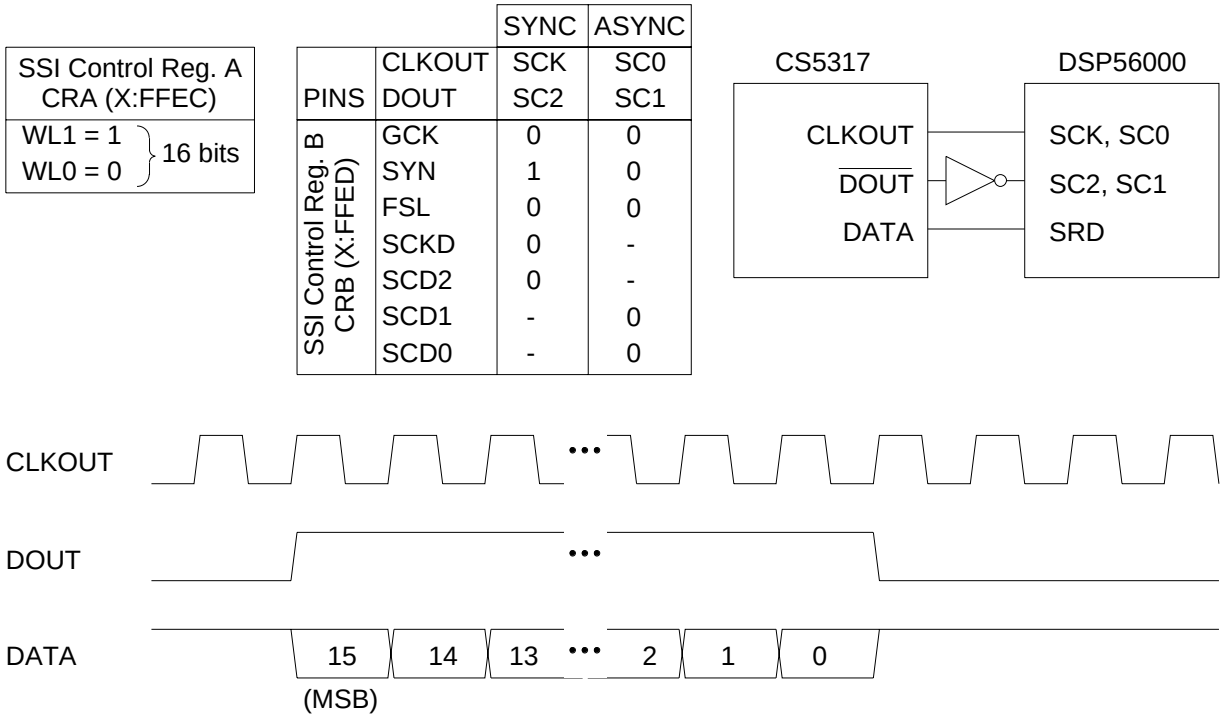


Figure A3. CS5317-to-Motorola DSP56000 Serial Interface

Figure A4 shows the interconnection and timing details for connecting a CS5317 to a WE DSP16 DSP chip.

Figure A5 shows the interconnection and timing details for connecting a CS5317 with TMS32020 and TMS320C25 DSP chips.

Serial I/O Control Register (SIOC)

Field	Value	Meaning
MSB	1	MSB input first
ILD	0	ILD is an input
ICK	0	ICK is an input
ILEN	0	16 bit input data

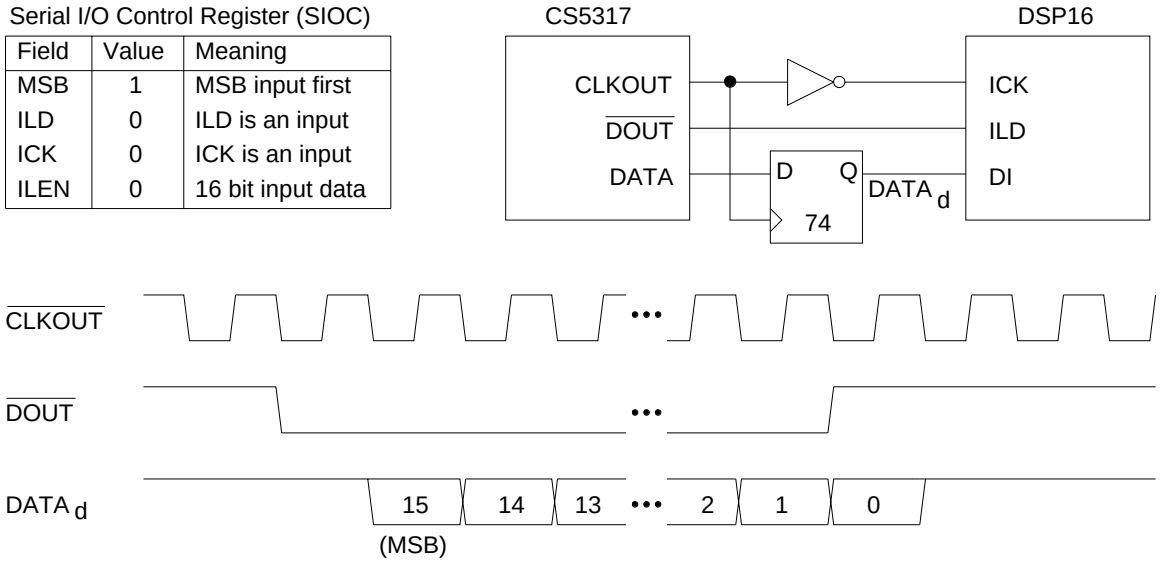


Figure A4. CS5317-to-WE DSP16 Serial Interface

TMS32020 Status Register (ST1):
F0 = 0 (16 bit data)
TMS320C25 Status Register (ST1):
F0 = 0 (16 bit data)
FSM = 1 (Frame Sync used)

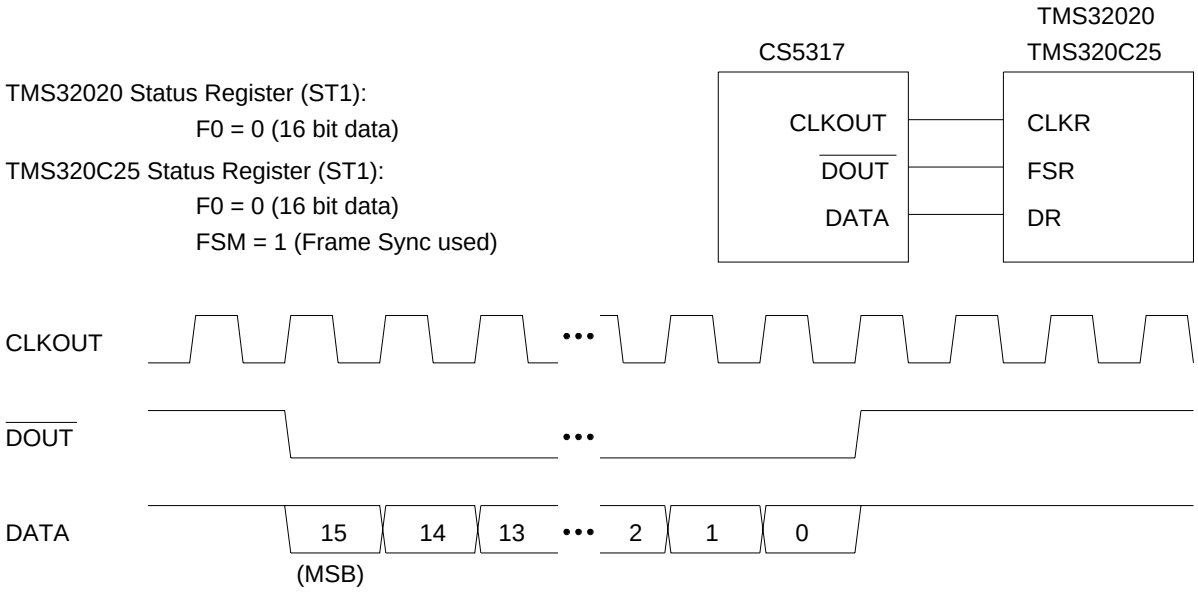


Figure A5. CS5317-to-TMS32020/TMS320C25 Serial Interface

• Notes •

A DIVISION OF CIRRUS LOGIC

CDB5317

Evaluation Board for CS5317

Features

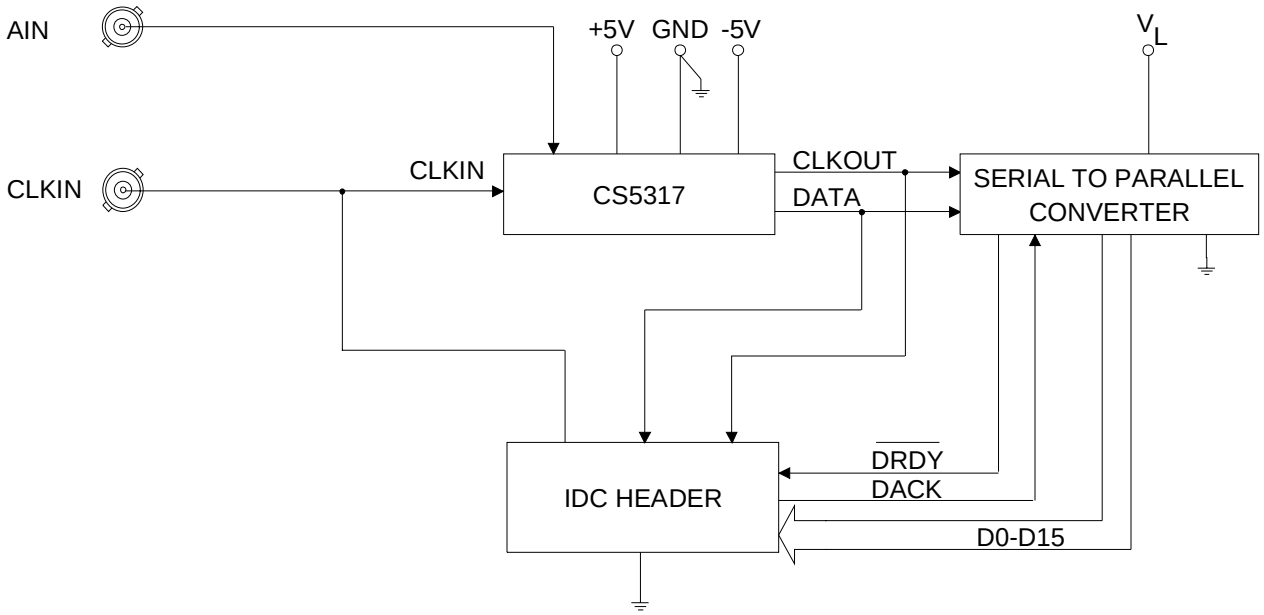
- Easy to Use Digital Interface
  Parallel 16 Bits With Clock
  Serial Output With Clock
- Multiple Operating Modes
  Including Two PLL Modes
- IDC Header used to access Parallel Data, Serial Data, and Clock Input and Output

Description

The CDB5317 Evaluation Board is designed to allow the user to quickly evaluate performance of the CS5317 Delta-Sigma Analog-to-Digital Converter. All that is required to use this board is an external power supply, a signal source, a clock source, and an ability to read either serial or parallel 16bitdata words.

ORDERING INFORMATION

CDB5317 Evaluation Board



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

GENERAL DESCRIPTION

The CDB5317 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5317 Delta-Sigma Analog-to-Digital Converter. Included on the board is a serial-to-parallel converter. The user can access output data in either parallel or serial form. When supplied with the necessary +5 V and -5 V power supplies, a CLKIN signal, and an analog signal source, the CDB5317 will provide converted data at the 40 pin header.

SUGGESTED EVALUATION METHOD

An efficient evaluation of the CS5317 using the CDB5317 may be accomplished as described below.

The following equipment will be required for the evaluation:

- The CDB5317 Evaluation Board.
- A power supply capable of supplying +5V and -5V.
- A clock source as the CLKIN signal of the CS5317.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator".
- A PC equipped with a digital data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface".
- A software routine to collect the data and perform a Fast Fourier Transform (FFT).

The evaluation board includes filter components for the on-chip phase locked loop. The components are adequate for testing if the CLKIN signal has little or no phase-jitter. If the CDB5317 board is being tested as part of a system which generates a CLKIN which contains jitter, the PLL filter components may need to be optimized for your system (see the CS5317 data sheet).

Set-up for evaluation is straightforward. First decide the operating mode and place the jumper on the board for the proper selection. Then decide whether the filter components for the phase locked loop are adequate or whether they should be changed for your evaluation. The PLL will lock on a steady clock input with the filter as it is. Connect the necessary 5 V (CMOS compatible) CLKIN signal for the application. Use the sine-wave generator to supply the analog signal to the CDB5317. Apply the analog input and CLKIN signals only when the evaluation board is powered up. Converted data will then appear at the header on the CDB5317. The header should be connected to the digital data acquisition board in the PC through an IDC 40 pin connector and cable. The software routine should collect the data from the CDB5317 and run a standard 1024 point Fast Fourier Transform (FFT). Such an analysis results in a plot similar to Figure 1. This plot resulted from using a 1kHz input signal and a Blackman-Harris window for the FFT.

The signal to noise and signal to total harmonic distortion characteristics of the CS5317 may be easily measured in this way. The signal to total harmonic distortion value for a particular input is the ratio of the RMS value of the input signal and the sum of the RMS values of the harmonics shown in the diagram. The dynamic range of the CS5317 can be measured by reducing the input

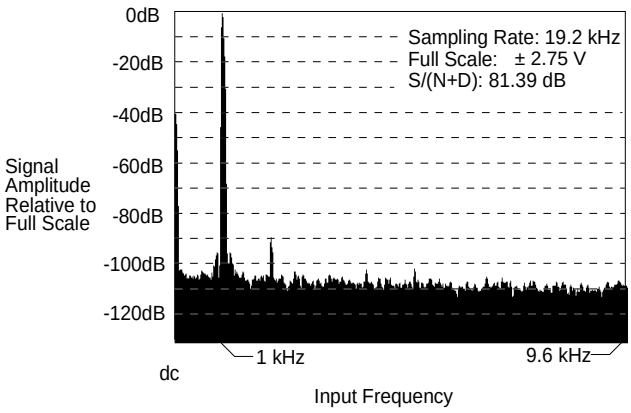


Figure 1. FFT Plot Example

amplitude so that distortion products become negligible. This allows an accurate measurement of the noise floor.

More complex analysis such as intermodulation distortion measurements can be accomplished with the addition of another sine-wave generator.

CIRCUIT DESCRIPTION

Figure 2 illustrates the CS5317 A/D converter IC circuit connections. The chip operates off of ±5V. These voltages are supplied from a power source external to the evaluation board. Binding posts are supplied on the board to connect the +5, -5, and ground power lines. A good quality low ripple, low noise supply will give the best performance. The +5 V supply can also be used for VL and should be connected between the VL board jack and the power supply, as opposed to connecting the VL jack straight to the +5V jack. The +5V jack is the positive power source for the CS5317 IC whereas the VL jack supplies power to all the digital ICs. Care should be taken that noise is not coupled between VL and +5V; however, supply noise is generally not a problem with the CS5317 since the on-chip decimation filter will remove any interference outside of its passband. The +5 and -5 V supply lines are filtered on

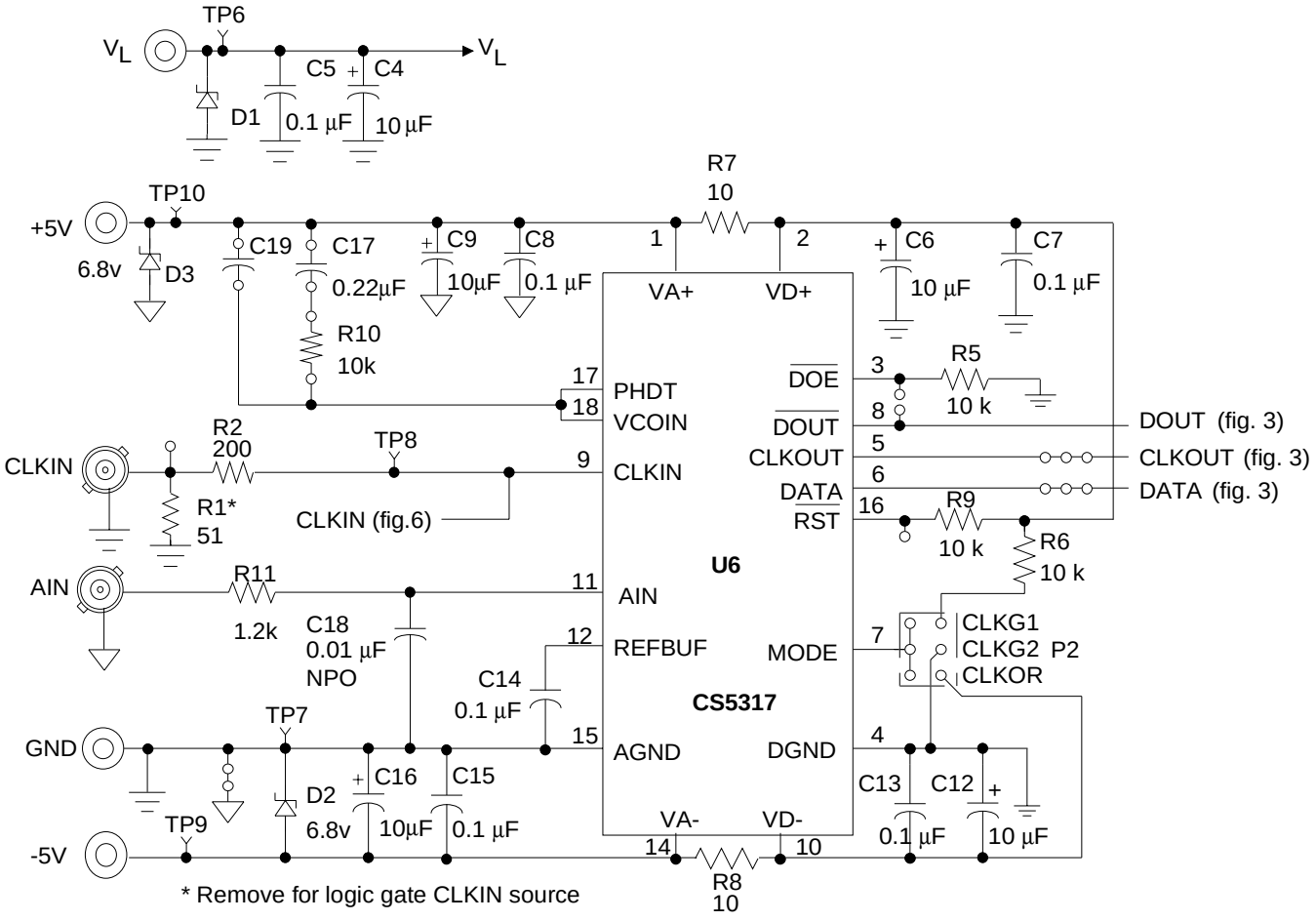


Figure 2. Analog-to-Digital Converter

the board and then connected to the V_A+ and V_A- supply pins of the chip. The +5 V and -5V are then connected by means of ten Ω resistors to the V_D+ and V_D- pins respectively. Capacitive filtering is provided on all supply pins of the chip. In addition there is a 0.1 µF filter capacitor connected from the REFBUF pin of the chip to the V_A- supply pin.

To properly operate, the CS5317 chip requires an external (5 V CMOS compatible) clock. A BNC connector labeled CLKIN is provided to connect the off-board clock signal to the board. The CLKIN signal is also available on the 40 pin header connector. The CLKIN signal is one input to the phase detector of the on-chip phase locked loop of the CS5317.

Header connector P2 (see Figure 2) is provided to allow mode selection for the CS5317 chip. The mode selection works together with the CLKIN signal to set the sample rate and the output word rate of the CS5317. See the CS5317 data sheet for details on mode selection. Two of the available modes (CLKG1 and CLKG2) utilize the on-chip phase locked loop to step up the CLKIN frequency to obtain the necessary sample rate clock for the A/D converter. Another mode (the CLKOR mode) does not use the on-chip PLL but instead drives the sample function directly. The

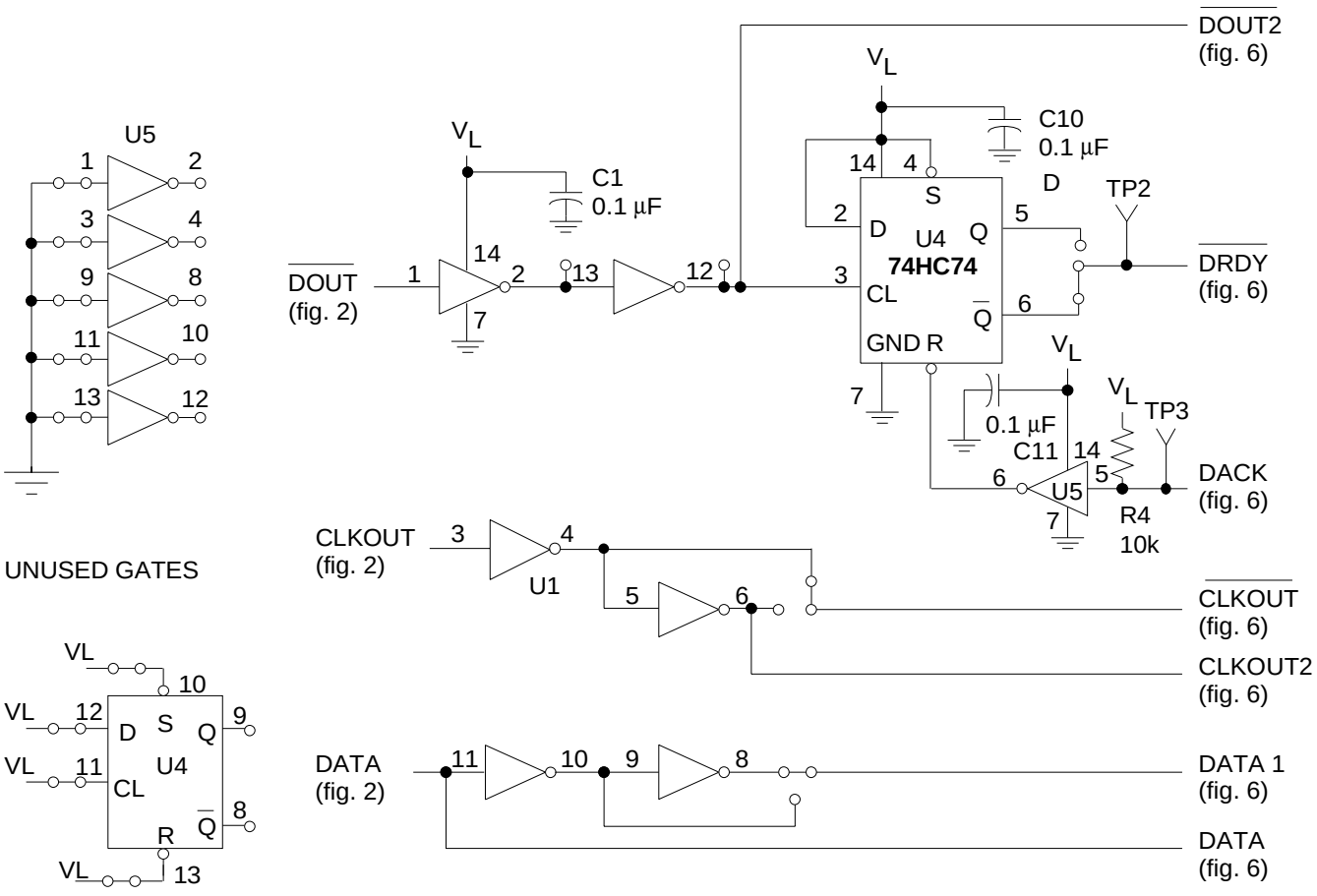
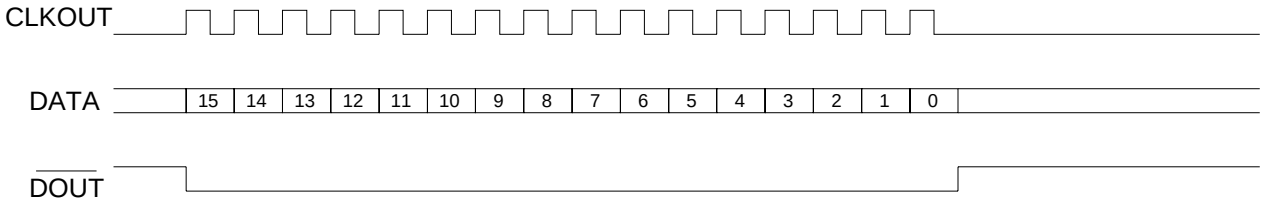


Figure 3. Buffers and Parallel Handshake Flip-Flop



Note: For a complete description of serial timing see the CS5317 Data Sheet

Figure 4 Serial Data Timing

two modes which use the phase locked loop will require appropriate low pass filter components on the Evaluation Board. The low pass filter components help determine the PLL control loop response, including its bandwidth and stability and therefore directly affect the transient response of the PLL control loop. Appropriate filter components should be installed if a particular dynamic response to changes of the CLKIN signal is desired.

The filter components which are installed on the board have been chosen for the following parameters: MODE: CLKG2; CLKIN: 7,200; N=512; damping factor: 1.0; Control loop -3 dB bandwidth: 2262 radians/second. These parameters yield R as 10 k Ω and C as 0.22 µF for the filter components.

The analog signal to be digitized is input to the AIN BNC connector. The digital output words from the CS5317 are buffered by HEX inverters as shown in Figure 3. The buffered versions of the CLKOUT and DATA signals are available on the header connector P1 in Figure 6. The serial data signals out of the CS5317 are illustrated in Figure 4. If remote control of the $\overline{\text{DOE}}$ line is desired, the trace on the PC Board can be opened and a wire connection can be soldered to the $\overline{\text{DOE}}$ input line. Remote control of the $\overline{\text{RST}}$ line of the CS5317 is also available if desired.

Figures 5 and 6 illustrate the serial to parallel shift registers including timing information. The DATA output signal from the CS5317 is input to the data input of the shift register. An inverted version of the CLKOUT signal is used to clock the DATA into the shift registers. The two 8-bit shift register ICs also include output latches. The rising edge

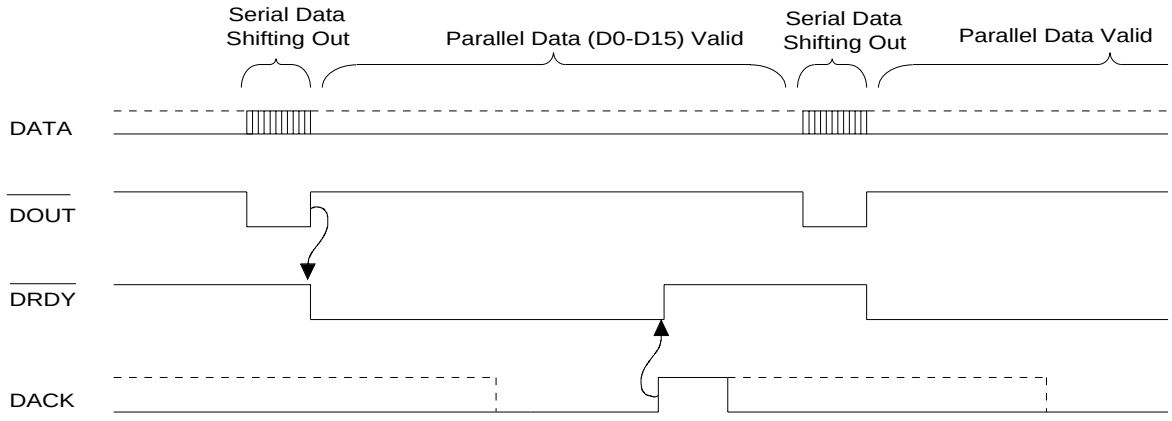


Figure 5. Parallel Data Timing

of the $\overline{\text{DOUT}}$ signal from the CS5317 is used to latch the data once it is input to the shift registers. The rising edge of $\overline{\text{DOUT}}$ is also used to toggle the $\overline{\text{DRDY}}$ flip flop (see Figure 3). The flip flop is used to signal a remote device whenever new data is latched into the output registers. The $\overline{\text{DRDY}}$ flip flop is reset whenever DACK occurs.

A component layout of the CDB5317 board is illustrated in Figure 7.

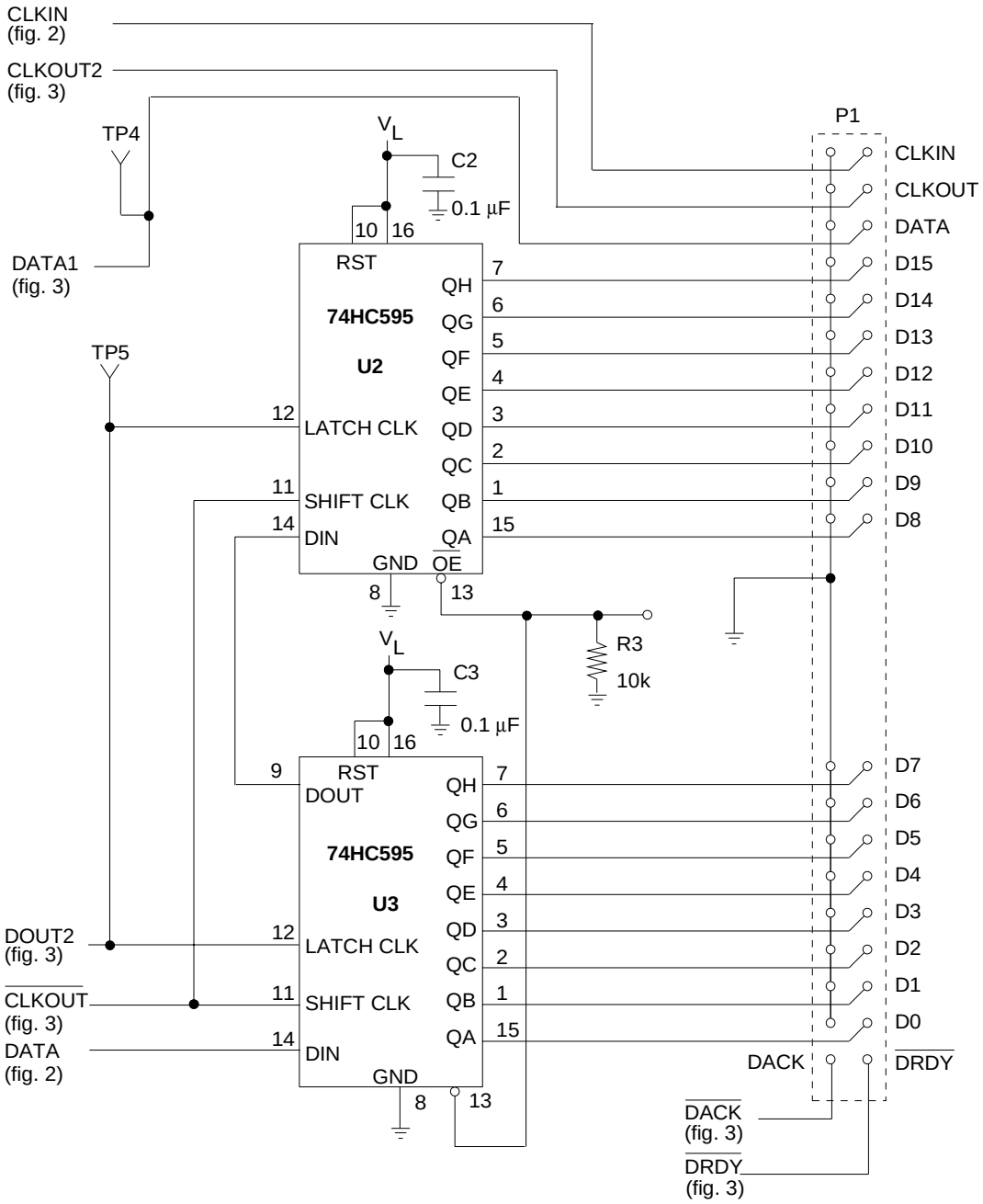


Figure 6.

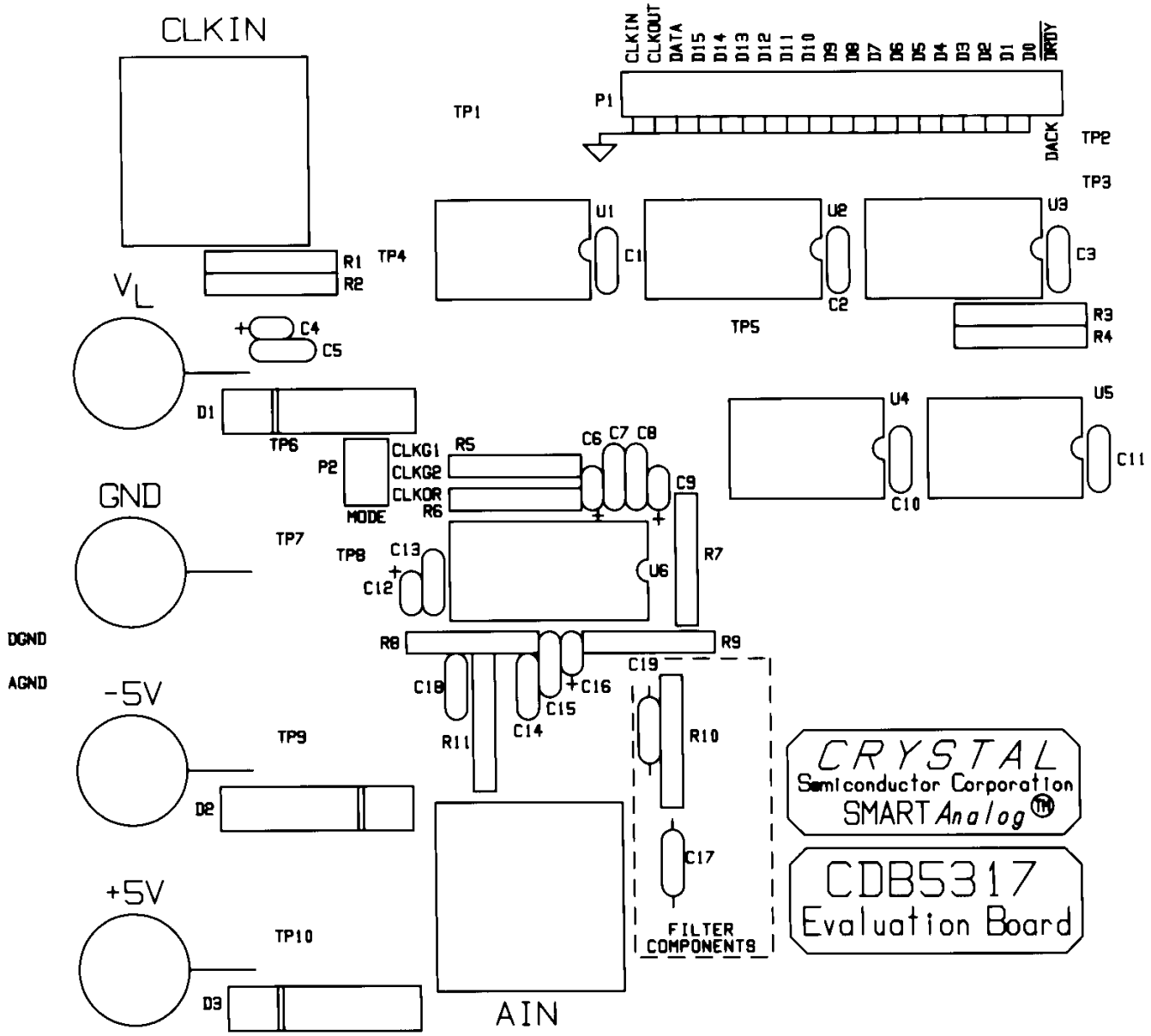


Figure 7. Bird's Eye View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