CS4811

Fixed Function Multi-Effects Audio Processor

Features

- Audio Processor for embedded reverb/effects applications
  - Proprietary 24-bit Audio Processing Engine
  - On-chip RAM (No external RAM required)
  - On-chip 24-bit ΔΣ ADC with 100 dB Dyn. Range
  - On-chip 24-bit ΔΣ DAC with 100 dB Dyn. Range
  - Automatically boots firmware from external serial EEPROM
- Firmware available for Guitar Effects or Mixer Effects applications
- Single +5 V Supply
- 100-pin Metric Quad Flat Pack (MQFP)

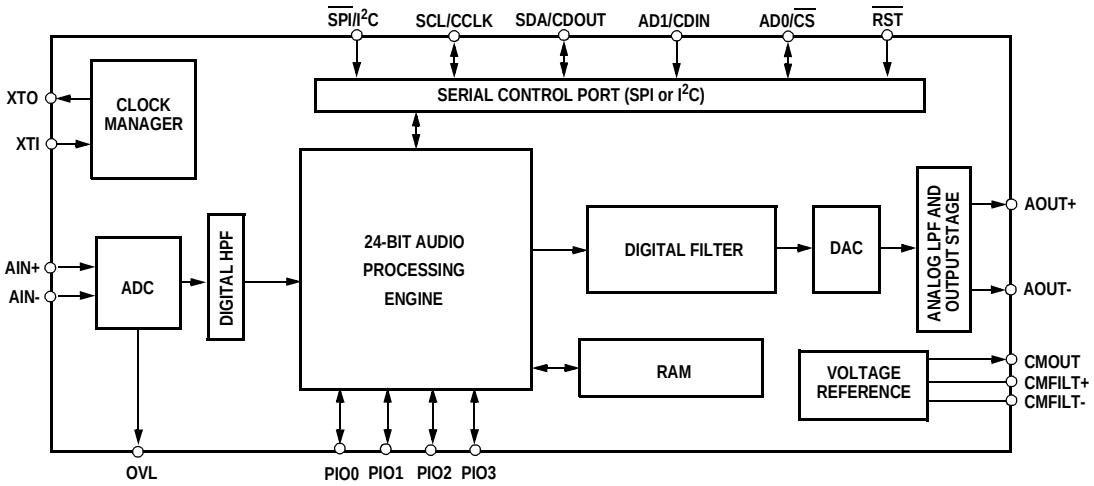
Description

The CS4811 is a complete audio effects processing system on a chip. This device integrates a proprietary 24-bit audio processing engine, large on-chip RAM memories, and a high performance 24-bit audio codec. A serial control port allows the device to boot firmware from a compact and low cost SPI or I^2C serial EEPROM. Other features such as single +5 V operation simplify system design.

Firmware for the CS4811 is provided by Cirrus Logic. There are two different firmware codes available; one for guitar effects and one for audio mixers. The guitar effects firmware provides a host of electric guitar effects including spring reverb, delay, chorus, flange and tremolo. The mixer effects firmware provides a suite of effects such as digital reverb, delay and chorus which are suitable for use in audio mixers, karaoke and acoustic instrument amplifiers. The CDB4811GTR and CDB4811MXR evaluation boards allow easy evaluation of the CS4811 device and the associated firmware.

ORDERING INFO

CS4811-KM	-10 to +70°C	100-pin MQFP
CDB4811GTR-01	Guitar Effects Evaluation Board	
CDB4811MXR-01	Mixer Effects Evaluation Board	



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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ADC CHARACTERISTICS (T_A = 25° C; VA, VD = + 5 V; -1 dB Full Scale Input Sine wave, 997 Hz; Fs = 48 kHz; XTI = 12.2880 MHz; Measurement Bandwidth is 20 Hz to 20 kHz)

Parameters		Symbol	Min	Typ	Max	Units
Analog Input Characteristics						
ADC Conversion	Stereo Audio channels		16	-	24	Bits
Dynamic Range	(A weighted, Note 4) (unweighted, Note 4)		93 90	100 97	- -	dB dB
Total Harmonic Distortion + Noise	(Note 1,4)	THD+N	-	-92	-87	dB
Offset Error (with internal high pass filter enabled)	(Note 5)		-	-	0	LSB
Full Scale Input Voltage (Differential)			1.9	2.0	2.1	V_{rms}
Gain Drift	(Note 2)		-	100	-	ppm/°C
Input Resistance			10	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage			-	2.3	-	V
Common Mode Rejection Ratio	(Note 2)	CMRR		60		dB
High Pass Filter Characteristics						
Frequency Response	-3dB (Note 3) -0.14dB (Note 3)		- -	3.7 20	- -	Hz Hz
Phase Deviation	@ 20 Hz (Note 3)		-	10	-	Degree
Passband Ripple			-	-	0	dB

Notes:
1. Referenced to typical full-scale differential input voltage (2 V_{rms}).
2. Bench tested only.
3. Filter characteristics scale with output sample rate.
4. Measured using differential analog input circuit, see Figure 6.
5. Filter response is not tested but is guaranteed by design.

DAC CHARACTERISTICS (T_A = 25° C; VA, VD = + 5 V; Full Scale Output Sine wave, 997 Hz; Fs = 48 kHz; XTI = 12.288 MHz; Measurement Bandwidth is 20 Hz to 20 kHz)

Parameters		Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.						
DAC Resolution			16	-	24	Bits
Dynamic Range	(DAC not muted, A weighted)		95	100	-	dB
Total Harmonic Distortion + Noise		THD+N	-	-90	-85	dB
Offset Voltage (differential)	(Note 6)		-	-20±5	-	mV
Offset Voltage (V+/V- relative to CMOUT)	(Note 6)		-	-45/-28	-	mV
Full Scale Output Voltage	(Differential)		1.9	2.0	2.1	V_{rms}
Gain Drift	(Note 2)		-	100	-	ppm/°C
Out of Band Energy	(Fs/2 to 2Fs, Note 2)		-	-60	-	dBFS
Analog Output Load	Resistance Capacitance		10 -	- -	- 100	kΩ pF
Analog Loopback Performance						
Signal-to-Noise Ratio (CCIR-2K weighted, -20 dB input)		CCIR-2K	-	74	-	dB
Power Supply						
Power Supply Current	Operating Power Down (Note 7)		- -	200 1	- -	mA mA
Power Supply Rejection	(1 kHz, 10 mV_{rms}, Note 2)		-	50	-	dB

Notes: 6. Measured with DAC calibration disabled.

7. Measured with XTI clock disabled.

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 25° C; VA, VD = +5 V, outputs loaded with 30 pF)

Parameters		Symbol	Min	Typ	Max	Units
ADC & DAC Sample Rate		Fs	30	-	50	kHz
XTI Frequency XTI = 256Fs			7.68	-	12.8	MHz
XTI Duty Cycle XTI =256Fs	(Note 8)		40	-	60	%
XTI Jitter Tolerance			-	500	-	ps
$\overline{\text{RST}}$ Low Time	(Note 9)		500	-	-	ns

Notes: 8. Guaranteed by characterization but not tested.

9. On power-up, the CS4811 $\overline{\text{RST}}$ pin should be asserted until the power supplies have reached steady state.

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MASTER (TA = 25° C, VA, VD = 5 V; Inputs: logic 0 = DGND, logic 1 = VD, C_L = 30 pF)

Parameter	Symbol	Min	Typ	Max	Units
SPI Master (Self-Boot) Mode (SPI/I2C = 0, SCPM/S = 1)					
CCLK Clock Frequency	f_{sck}	-	Fs	-	kHz
CCLK Low Time	t_{scl}	-	1/(2*Fs)	-	ns
CCLK High Time	t_{sch}	-	1/(2*Fs)	-	ns
CCLK Rise Time (Note 10)	t_{r2}	-	12	-	ns
CCLK Fall Time (Note 10)	t_{f2}	-	12	-	ns
$\overline{RST}$ rising to $\overline{CS}$ falling	t_{srs}	-	42	-	µs
$\overline{CS}$ High Time Between Transmissions	t_{csh}	37	-	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	5	-	-	µs
$\overline{CS}$ Falling to CDOUT valid	t_{dv}	-	-	50	ns
CCLK Falling to CDOUT valid	t_{pd}	-	-	100	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	80	-	-	ns
CCLK Rising to DATA Hold Time	t_{dh}	80	-	-	ns
CCLK Falling to $\overline{CS}$ rising	t_{clcs}	40	-	-	ns

Notes: 10. Measured with a 2.2 kΩ pullup resistor to VD.

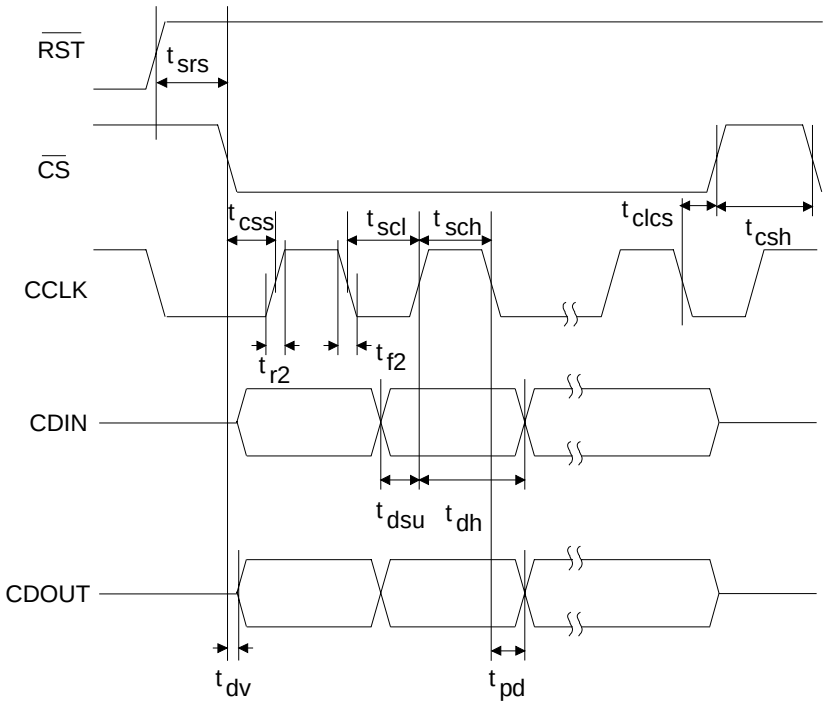


Figure 1. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MASTER (T_A = 25° C; VA, VD = 5 V; Inputs: logic 0 = DGND, logic 1 = VD, C_L = 30 pF)

Parameter		Symbol	Min	Typ	Max	Units
I²C® Master (Self-Boot) Mode ($\overline{SPI}$/I2C = 1, SCPM/$\overline{S}$ = 1) (Note 11)						
SCL Clock Frequency		f_{scl}	-	Fs	-	kHz
Clock Low Time		t_{low}	-	1/(2*Fs)	-	µs
Clock High Time		t_{high}	-	1/(2*Fs)	-	µs
Bus Free Time Between Transmissions		t_{buf}	4.7	-	-	µs
$\overline{RST}$ rising to start condition		t_{irs}	-	22	-	µs
Start Condition Hold Time		t_{hdst}	4.0	-	-	µs
Setup Time for Repeated Start Condition		t_{sust}	13.5	-	-	µs
SDA Setup Time to SCL Rising		t_{sud}	250	-	-	ns
SDA Hold Time from SCL Falling	(Note 12)	t_{hdd}	0	-	-	ns
SCL falling to SDA Output Valid		t_{cldv}	-	-	1.5	µs
SCL and SDA Rise Time	(Note 13)	t_r	-	-	1	µs
SCL and SDA Fall Time	(Note 13)	t_f	-	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	-	µs

Notes: 11. Use of the I²C bus interface requires a license from Philips. I²C is a registered trademark of Philips Semiconductors.
12. Data must be held for sufficient time to bridge the worst case fall time of 300 ns for CCLK/SCL.
13. For both SDA transmitting and receiving.

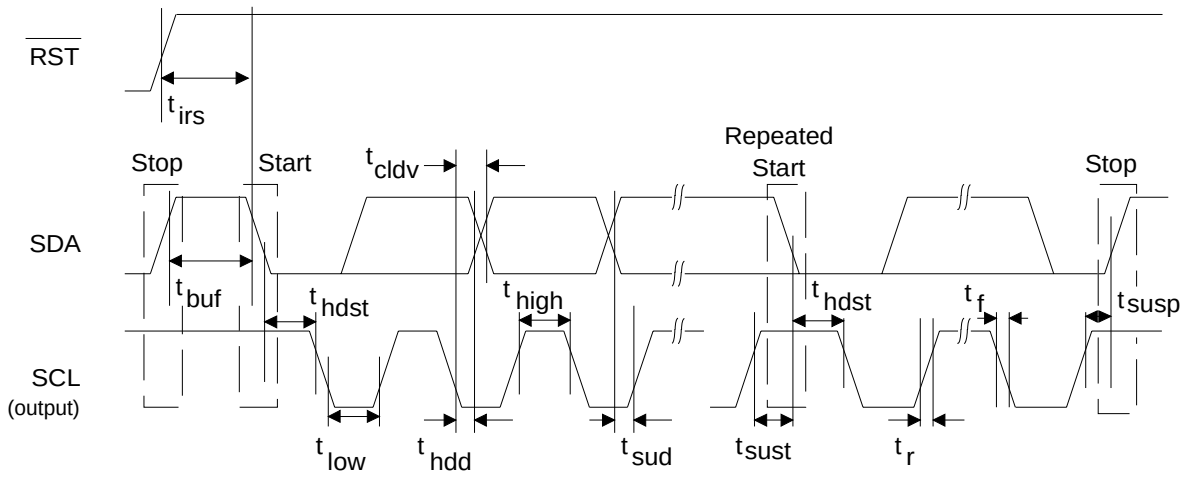


Figure 2. I²C Control Port Timing

ABSOLUTE MAXIMUM RATINGS (All voltages with respect to AGND = DGND = 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD	-0.3	-	6.0	V
	Analog	VA	-0.3	-	6.0	V
Input Current	(Note 14)		-	-	±10.0	mA
Analog Input Voltage	(Note 15)		-0.7	-	(VA)+0.7	V
Digital Input Voltage	(Note 15)		-0.7	-	(VD)+0.7	V
Ambient Temperature	(Power Applied)		-55	-	+125	°C
Storage Temperature			-65	-	+150	°C

Notes: 14. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

15. The maximum over or under voltage is limited by the input current.

Warning: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (All voltages with respect to AGND = DGND = 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies	Digital	VD	4.75	5.0	5.25	V
|VA - VD| < 0.4V	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature		T_A	-10	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 25° C; VA, VD = 5 V)

Parameters		Symbol	Min	Typ	Max	Units
High-level Input Voltage	(except XTI)	V_{IH}	2.8	-	(VD)+0.3	V
Low-level Input Voltage	(except XTI)	V_{IL}	-0.3	-	0.8	V
High-level Output Voltage at I_0 = -2.0 mA	(except XTO)	V_{OH}	(VD)-1.0	-	-	V
Low-level Output Voltage at I_0 = 2.0 mA	(except XTO)	V_{OL}	-	-	0.4	V
High-level Input Voltage	(XTI)	V_{IH}	2.8	-	-	V
Low-level Input Voltage	(XTI)	V_{IL}	-	-	2.3	V
Input Leakage Current	(Digital Inputs)		-	-	10	µA
Output Leakage Current	(High-Z Digital Outputs)		-	-	10	µA

SWITCHING CHARACTERISTICS - PROGRAMMABLE I/O (T_A = 25° C; VA, VD = 5 V ±5%; Inputs: logic 0 = DGND, logic 1 = VD, C_L = 30 pF)

Parameters	Symbol	Min	Typ	Max	Units
Output Rise Time	t_{rpo}	-	200	-	ns
Output Fall Time	t_{fpo}	-	200	-	ns

2. TYPICAL CONNECTION DIAGRAMS

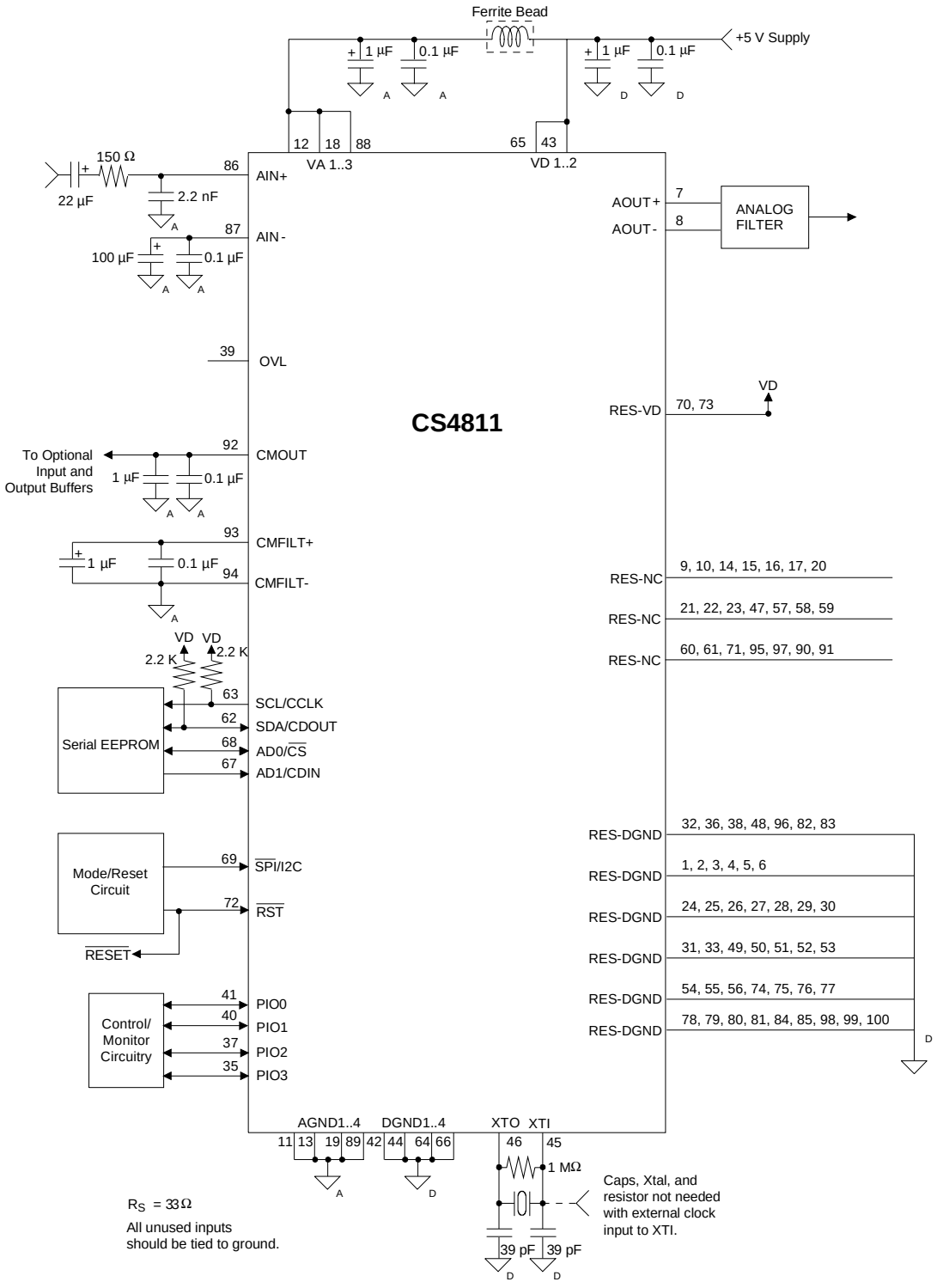


Figure 3. Typical Connection Diagram, Single-ended Input

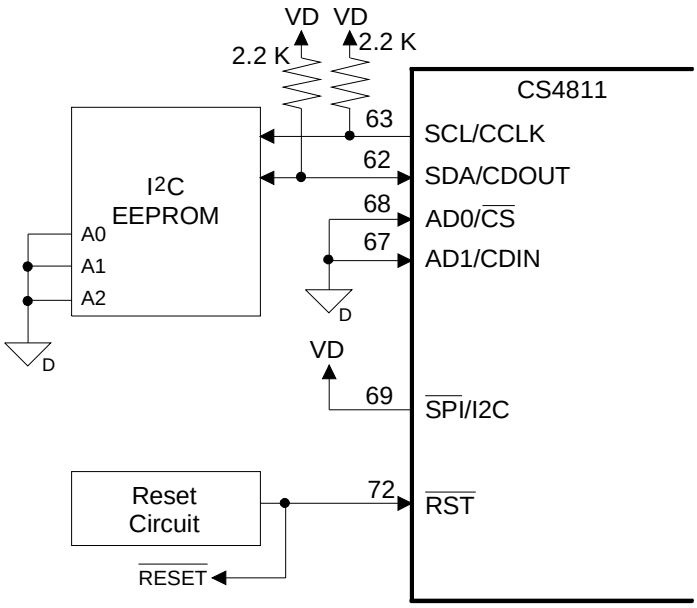


Figure 4. Typical Connection Diagram, I²C Mode

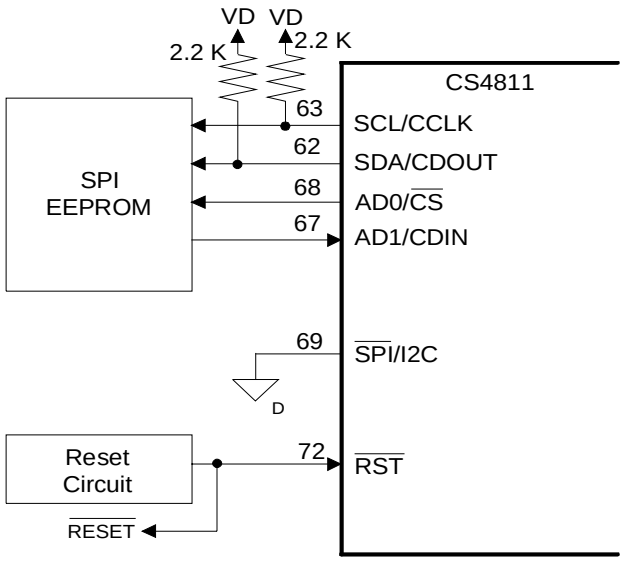


Figure 5. Typical Connection Diagram, SPI Mode

3. FUNCTIONAL DESCRIPTION

3.1 Overview

The CS4811 is a complete audio subsystem on a chip, integrating a proprietary 24-bit audio processing engine with large on chip RAM memories and a single channel 24-bit audio codec.

The delta-sigma ADC includes linear phase digital anti-aliasing filters and only requires a single-pole external passive filter.

The sigma-delta DAC includes a switched-capacitor anti-image filter and requires an external 2nd or 3rd order active filter that can be easily integrated into the output differential-to-single-ended converter circuit.

The serial control port is designed to accommodate I^2C® or SPI interfaces for stand-alone operation with an external non-volatile memory.

3.2 Analog Inputs

3.2.1 Line Level Inputs

AIN+ and AIN- are the differential line level analog inputs (See Figure 3). These pins are internally biased to the CMOUT voltage of 2.3 V. A DC blocking capacitor placed in series with the input pins allows signals centered around 0 V to be input to the CS4811. Figure 3 shows operation with a single-ended input source. This source may be supplied to either the positive or negative input as long as the unused input is connected to ground through capacitors as shown. When operated with single-ended inputs, distortion will increase at input levels higher than -1 dB Full Scale. If better performance is required, a single-ended-to-differential converter, shown in Figure 6, may be used. This circuit provides unity gain, DC blocking on the input and anti-alias filtering.

The OVL output pin asserts when the analog input is out-of-range.

3.2.2 Digital High Pass Filter

In DC coupled systems, a small DC offset may exist between the input circuitry and the A/D converters. The CS4811 includes a high pass filter after the decimator to remove these DC components. The high pass filter response, given in *High Pass Filter Characteristics*, scales linearly with sample rate. Thus, the -3 dB frequency at a 44.1 kHz sample rate will be equal to 44.1/48 times that at a sample rate of 48 kHz.

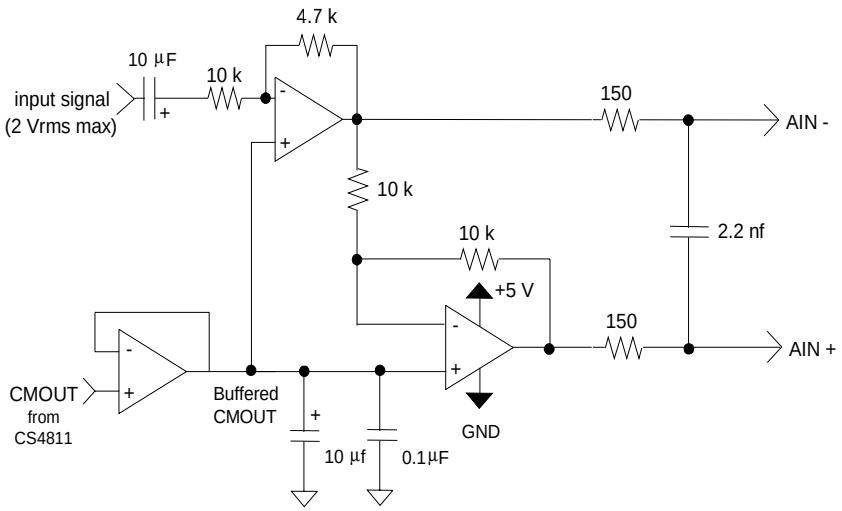


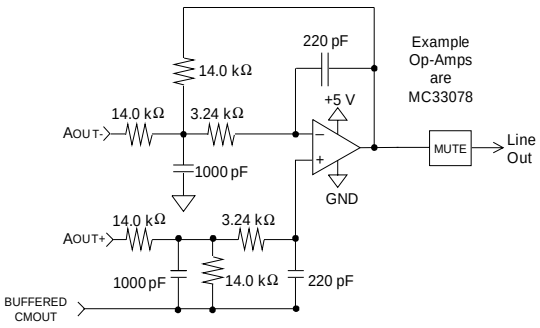
Figure 6. Optional Line Input Buffer

3.3 Analog Outputs

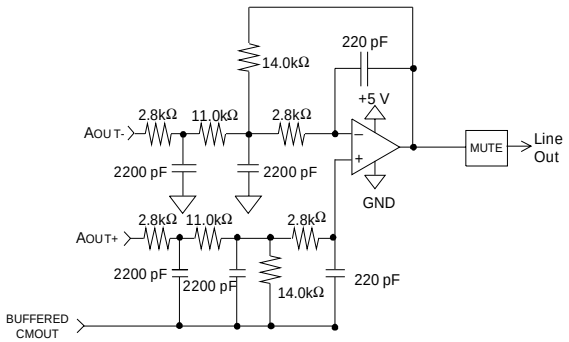
3.3.1 Line Level Outputs

The CS4811 contains on-chip differential buffer amplifiers that produce line level outputs AOUT+ and AOUT-, which are capable of driving 10 kΩ loads. These amplifiers are internally biased to the CMOUT voltage of 2.3 V.

The recommended off-chip analog filter is a 2nd order Butterworth with a -3 dB corner at Fs. A third order Butterworth filter with a -3 dB corner at 0.75 Fs can be used if greater out of band noise filtering is desired. These filters can be easily integrated into a differential-to-single-ended converter circuit as shown in the 2-pole and 3-pole Butterworth filters of Figure 7. Figure 8 shows the recommended mute circuit referenced in Figure 7. Activating the mute circuit is recommended on power-up and power-down to avoid the output of undesirable audio signals.



2-Pole Butterworth Filter



3-Pole Butterworth Filter

Figure 7. Butterworth Output Filters

3.4 Clock Generation

The master clock to operate the CS4811 may be generated by using the on-chip oscillator with an external crystal or may be input from an external clock source.

3.4.1 Clock Source

The CS4811 requires a 256 Fs master clock to run the internal logic. The two possible clock sources are the on-chip crystal oscillator or an external clock input to the XTI pin.

The master clock may be generated directly from the on-chip crystal oscillator circuit. When using the on-chip crystal oscillator, external loading capacitors are required. (see Figure 3) High frequency crystals (>8 MHz) should be parallel resonant, fundamental mode and designed for 20 pF loading. (equivalent to 40 pF to ground on each leg)

The master clock may also be generated directly from an external CMOS clock input to the XTI pin.

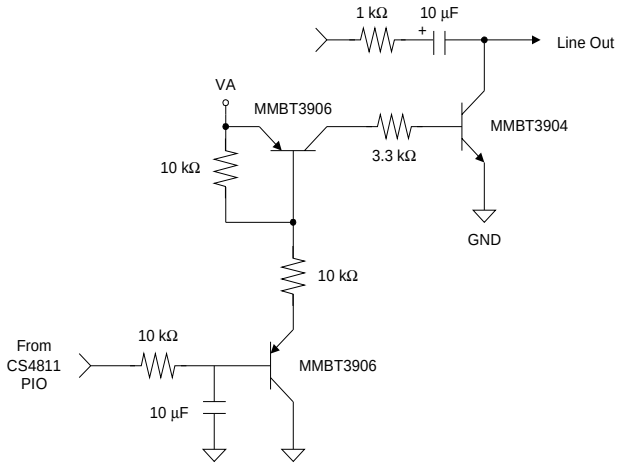


Figure 8. Output Mute Circuit

3.5 Serial Control Port

The serial control port is used for self-booting from an external EEPROM and supports both the SPI bus and the $I^2C^®$ bus interfaces. The desired interface is selected via the $\overline{SPI}/I^2C$ pin, which is sampled during de-assertion of the $\overline{RST}$ pin.

3.5.1 SPI Bus

The SPI bus interface consists of 4 digital signals, CCLK, CDIN, CDOUT and $\overline{CS}$. CCLK, the control port bit clock, is used to clock individual data bits. CDIN, the control data input, is the serial data input line to the CS4811. CDOUT, the control data output, is the output data line from the CS4811. $\overline{CS}$, the chip select signal, is asserted to enable an external SPI port. Data is clocked in on the rising edge of CCLK and clocked out on the falling edge.

3.5.1.1 SPI Mode

The SPI master mode is designed for read-only operation during self-booting from a serial EEPROM. A typical self-boot sequence with a Xicor X25650 serial EEPROM, or equivalent, is shown in Figure 9. On exit from reset, the CS4811 asserts $\overline{CS}$. The 8-bit read instruction (00000011) is sent to the EEPROM followed by a pre-defined 16-bit start address. The CS4811 then automatically clocks out sequential bytes from the EEPROM until the last byte has been received. These bytes include initialization and configuration data for the device along with the application firmware code. After the last byte is received, the CS4811 deasserts $\overline{CS}$ and begins program execution. At this point, the serial control port becomes inactive and cannot be accessed.

3.5.2 I^2C Bus

The I^2C bus interface implemented on the CS4811 consists of 2 digital signals, SCL and SDA. SCL or serial clock, is used to clock individual data bits. SDA or serial data, is a bidirectional data line. Two additional pins, AD1 and AD0, are inputs which determine the 2 lowest order bits of the 7-bit I^2C device address and should be tied to ground.

3.5.2.1 I^2C Mode

The I^2C master mode is designed for read-only operation during self-booting from a serial EEPROM. A typical self-boot sequence with a Microchip X24256 serial EEPROM, or equivalent, is shown in Figure 10. On exit from reset, the CS4811 sends an initial write preamble to the EEPROM which consists of a I^2C start condition and the slave ad-

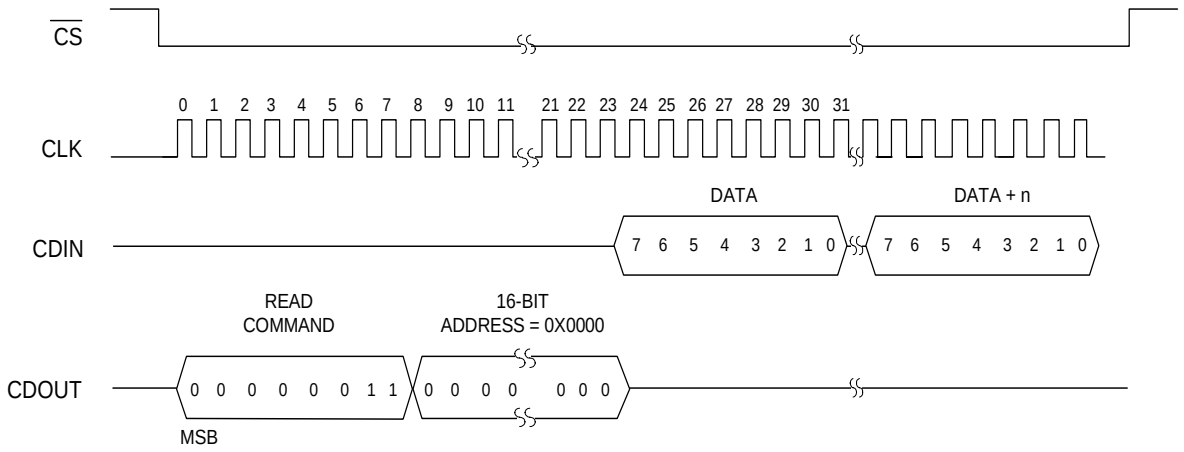


Figure 9. Control Port Timing, SPI Master Mode Self-Boot

dress byte. The slave address consists of the 4 most significant bits set to 1010, the following 3 bits corresponding to the device select bits, A2, A1 and A0 set to 000 and the last bit (R/$\overline{W}$) set to 0. Following this, a 2-byte EEPROM starting address of 0x0000 is sent to the EEPROM. The 2-byte EEPROM starting address uses only the lowest 13 bits and sets the highest 3 bits to zero. To begin reading from the EEPROM, the CS4811 sends another start condition followed by a read preamble. The read preamble is identical to the write preamble except for the state of the R/$\overline{W}$ bit. The CS4811 then automatically clocks out sequential bytes from the EEPROM until the last byte has been received. These bytes include initialization and configuration data for the device along with the application firmware code. After the last byte, the CS4811 initiates a stop condition and begins program execution. At this point, the serial control port becomes inactive and cannot be accessed.

3.6 Resets

Full chip reset can only be achieved by asserting the $\overline{RST}$ pin. With $\overline{RST}$ asserted, the chip enters low power mode during which the control port, CODEC and Audio Processor are reset, all registers are returned to their default values and the DAC outputs are muted. The $\overline{RST}$ pin should be asserted during power-up until the power supplies have reached steady state.

If the supply voltage drops below 4 Volts, the CODEC is reset, the DAC outputs are muted and the Audio Processor automatically executes a soft reset.

Upon exit from a CODEC reset, the Audio Processor restarts the application code and the CODEC performs the following procedure:

- The CODEC resynchronizes.
- The DAC outputs unmute.

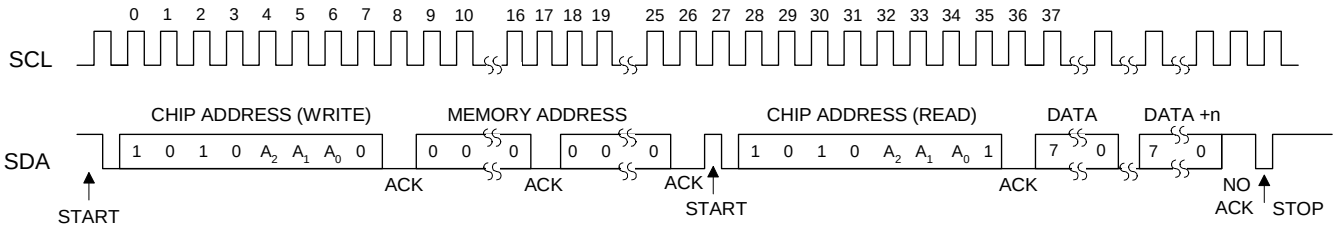


Figure 10. Control Port Timing, I²C Master Mode Self-Boot

4. POWER SUPPLY AND GROUNDING

Proper layout and grounding is critical to obtaining optimal audio performance in your system. The most important rule to remember is to not allow currents from digital circuitry to couple into sensitive analog circuitry. This is generally done by using a separate or filtered power supply for the analog circuitry, physically separating the analog and digital components and traces in the pcb layout and using wide traces or planes for ground and power. One misplaced component or trace can severely degrade overall system performance.

When using separate supplies, the analog and digital power should be connected via a ferrite bead, positioned closer than 1" to the device (see Figure 11). The CS4811 VA pin should be derived from the quietest power source available. If only one supply is available, use the suggested arrangement in Figure 3.

A single solid ground plane is the simplest grounding scheme that works well in many cases. In this case, all analog and digital grounds shown in Figure 3 are tied to the same ground plane. However, if separate analog and digital grounds are used, they should be tied together at one point with the location of this point determined by the circuit layout. By considering where the digital ground currents will return to their supply, the connection point can be chosen to keep those currents from flowing through sensitive analog circuit areas.

Decoupling capacitors should be placed as close as possible to the device with the lowest value capacitor closest to the chip. Any power and ground connection vias should be placed near their respective component pins and should be attached directly to the appropriate plane. If traces are used for the power supplies to the CS4811, they should be as wide as possible to maintain low impedance.

It is recommended to solder the CS4811 directly to the printed circuit board. Soldering improves performance and enhances reliability.

For an example layout, please refer to the CDB4811 data sheet.

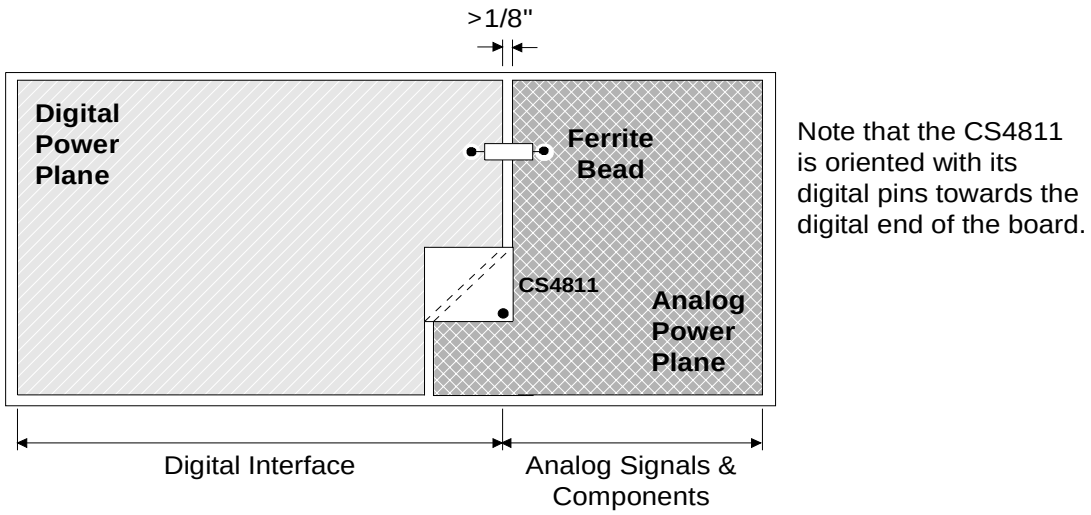


Figure 11. CS4811 Suggested Layout

5. PIN DESCRIPTIONS

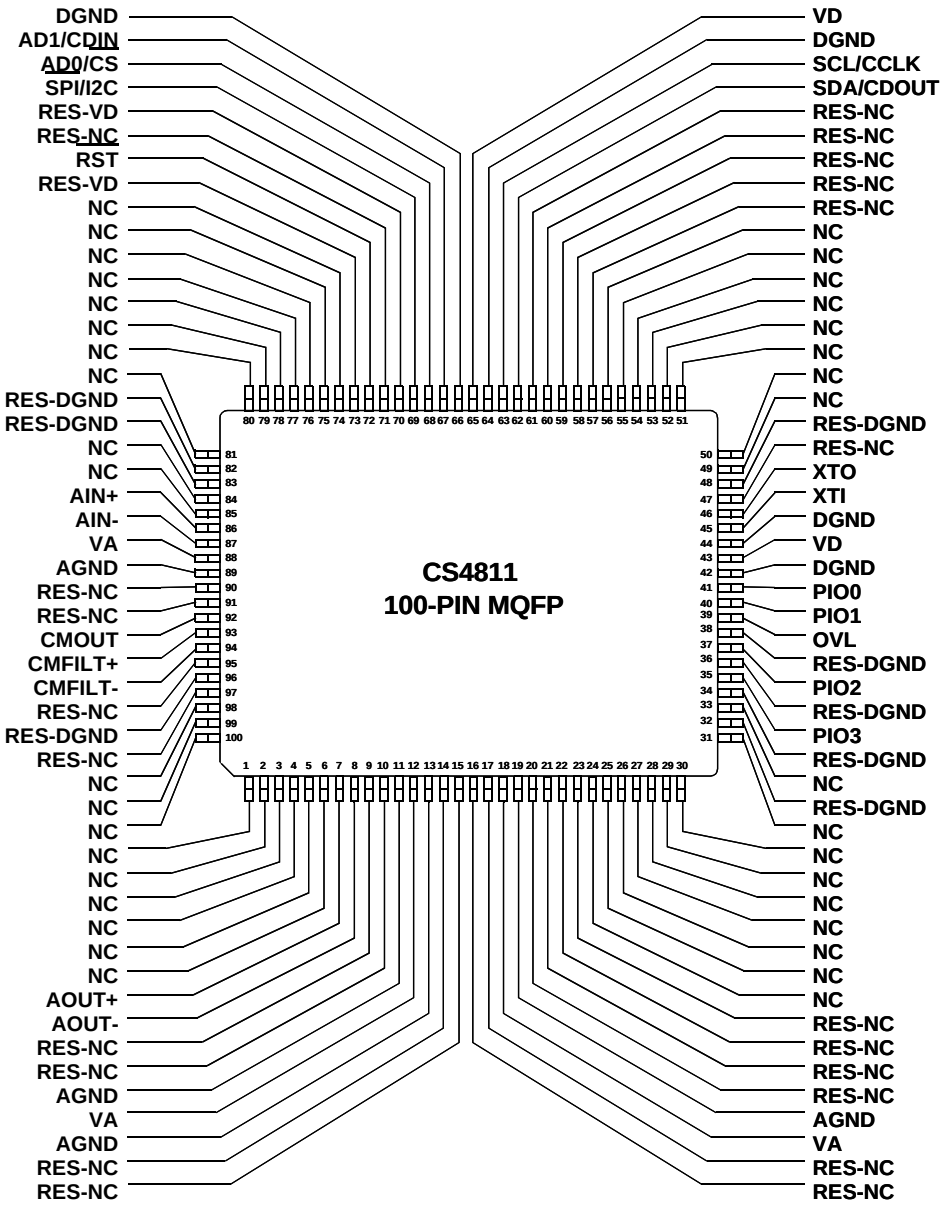


Figure 12. Pin Assignments

Power Supply

VA - Analog Power

Power: analog supply, +5 V.

AGND - Analog Ground

Ground: analog ground.

VD - Digital Power

Power: digital supply, +5 V.

DGND - Digital Ground

Ground: digital ground.

Analog Input

AIN+/- - Differential Audio Input

Inputs: These pins accept differential analog input signals and are biased to the internal reference voltage of approximately 2.3 V. The + and - input signals should be 180° out of phase resulting in a nominal differential input voltage of twice the input pin voltage. A single-ended signal may also be directly applied to either the + or - input with the other input AC coupled to ground through a capacitor. In general, differential input signals provide better performance. However, singled-ended inputs may result in reduced cost. Inputs may be AC or DC coupled. DC coupled input signals must be biased at 2.3 V. Any remaining DC offset is removed by an internal digital HPF. For best performance, a passive anti-aliasing filter is required. The typical connection diagram in Figure 3. shows the recommended single-ended input circuit. Figure 6 shows the recommended differential input circuit.

OVL - ADC Overload Indicator

Output: This pin is asserted when the ADC is clipping. The pin does not latch and de-asserts when clipping stops.

Analog Output

AOUT+/- - Differential Audio Output

Outputs: These pins output differential analog signals which are biased to the internal reference voltage of approximately 2.3 V. The + and - output signals are 180° out of phase resulting in a nominal differential output voltage of twice the output pin voltage. For best performance, an anti-imaging filter is required. Figure 7 shows the recommended second and third order Butterworth differential-to-single-ended output buffer circuits.

Voltage Reference

CMOUT - Common Mode Output

Output: This pin provides an internally generated reference of 2.3 V to be used for biasing external analog circuitry. The load on CMOUT must be DC only, with an impedance of not less than 50 kilohms.

CMFILT+,CMFILT- - Common Mode Filter Connections

Inputs: These pins are connections for external filter components required by the internal common mode reference circuit. See the typical connection diagram in Figure 3. for details.

Serial Control Port

$\overline{\text{SPI}}$/*I²C - Serial Control Port Format Select*

Input: This pin configures the control port for I²C format if tied to VD or SPI format if tied to DGND.

SCL/CCLK - Serial Control Port Clock

Output: This pin clocks serial control port data into and out of SDA in I²C mode. In SPI mode, it clocks control port data into CDIN and out of CDOUT.

AD0/$\overline{\text{CS}}$ *- I²C Address Bit 0 / SPI Chip Select*

Input/Output: In I²C® mode, AD0 is an input and must be tied to ground. In SPI mode, $\overline{\text{CS}}$ is an output and is used to select the boot EEPROM.

AD1/CDIN - I²C Address Bit 1 / SPI Data Input

Input: In I²C® mode, AD1 is an input and must be tied to ground. In SPI mode, CDIN is the serial control port data input and is clocked in on the rising edge of CCLK.

SDA/CDOUT - I²C Data / SPI Data Output

Bidirectional/Output: In I²C® mode, SDA is the bidirectional data I/O line. In SPI mode, CDOUT is the serial control port data output and is clocked out on the falling edge of CCLK.

Clock and Crystal

XTI, XTO - Crystal Oscillator Connections (Master Clock)

Input, Output: These pins provide connections for an external parallel resonant quartz crystal. Alternately, an external clock source may be applied to XTI. The clock frequency must be 256xFs.

Miscellaneous

PIO0:3 - General Purpose Inputs/Outputs

Bidirectional: These pins are general-purpose digital I/O pins. The Default state is input. The functionality of these pins after boot-up is determined by the application firmware.

$\overline{RST}$ - Reset

Input: This pin causes the device to enter a low power mode and forces all control port and I/O registers to be reset to their default values. The control port can not be accessed when reset is low.

NC - No Connect

Input: These pins are not internally connected and should be tied to ground for optimal performance.

RES-NC - Reserved, No Connect

These pins are reserved and must be left unconnected for normal operation.

RES-VD - Reserved, Connect to VD

These pins are reserved and must be tied to VD for normal operation.

RES-DGND - Reserved, Connect to DGND

These pins are reserved and must be tied to digital ground for normal operation.

RES-AGND - Reserved, Connect to AGND

These pins are reserved and must be tied to analog ground for normal operation.

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dbFs signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFs as suggested in AES 17-1991 Annex A.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the RMS analog output level with 1 kHz full scale digital input to the RMS analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the RMS sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

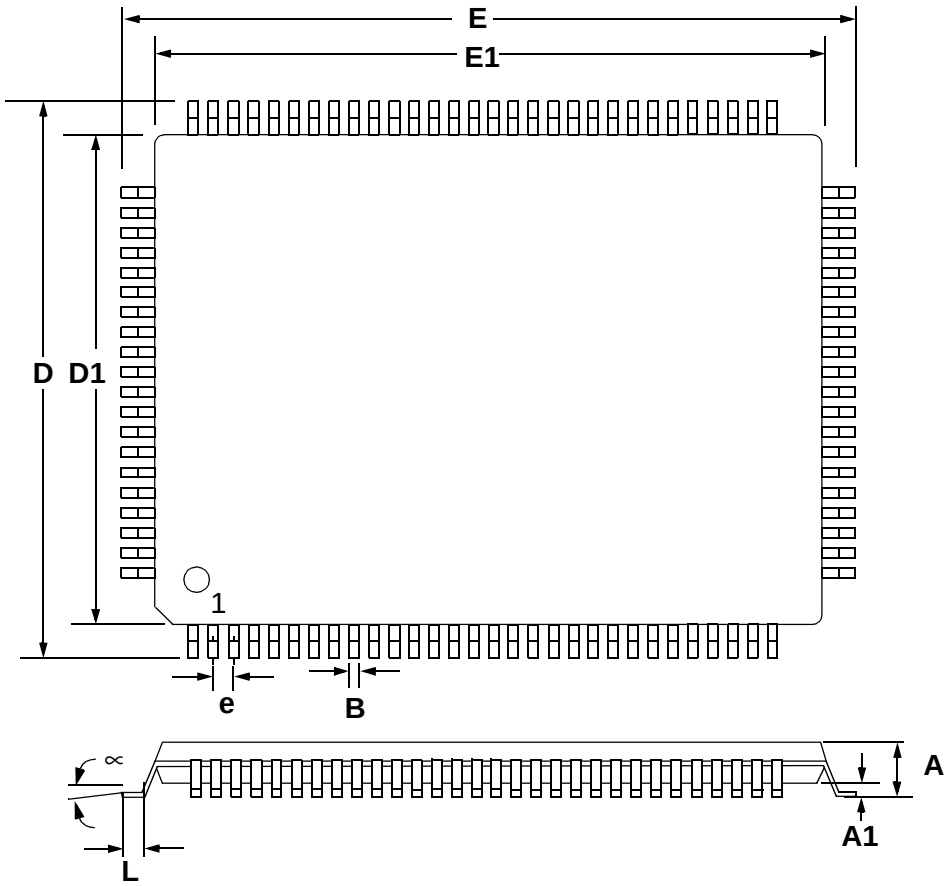
The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected input grounded. For the DAC's, the deviation of the output from zero (relative to CMOUT) with mid-scale input code. Units are in volts.

7. PACKAGE DIMENSIONS

100L MQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	0.134	--	--	3.400
A1	0.010	0.012	0.014	0.250	0.30	0.350
B	0.009	0.012	0.015	0.220	0.30	0.380
D	0.667	0.677	0.687	16.950	17.20	17.450
D1	0.547	0.551	0.555	13.900	14.00	14.100
E	0.904	0.91	0.923	22.950	23.20	23.450
E1	0.783	0.79	0.791	19.900	20.0	20.100
e*	0.022	0.026	0.030	0.550	0.65	0.750
∝	0.000°	4.00°	7.000°	0.00°	4.00°	7.00°
L	0.029	0.035	0.041	0.73	0.88	1.03

* Nominal pin pitch is 0.65 mm = 0.65 BSC

Controlling dimension is mm.
JEDEC Designation: MS022
ASE/SPIL

• Notes •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