CIRRUS LOGIC®

CS53L32A

Low Voltage, Stereo A/D Converter

Features

- 20-Pin TSSOP package
- 1.8 to 3.3 volt supply
- 24-bit conversion / 96 kHz sample rate
- 98 dB dynamic range at 3 V supply
- -88 dBFS THD+N
- Low power consumption
  - 9.7 mW at 1.8 V
- Up to 32 dB gain
  - 20 dB gain step
  - 12 dB variable input gain, 1 dB steps
  - Changes made at zero crossings
- Stereo inputs
- Digital volume control
  - 96 dB attenuation, 1 dB step size
  - Mute
  - Soft ramping
- 2:1 input mux

Description

The CS53L32A is a highly integrated, 24-bit, 96 kHz audio ADC providing stereo analog-to-digital converters using delta-sigma conversion techniques. This device includes volume control and line level inputs in a 20-pin TSSOP package.

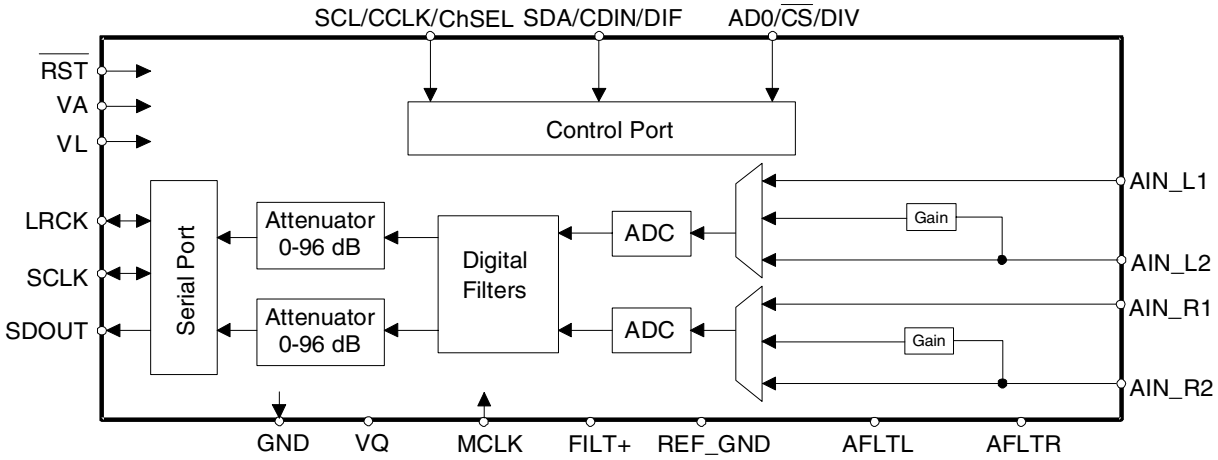
The CS53L32A is based on delta-sigma modulation allowing infinite adjustment of the sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS53L32A contains adjustable analog gain, a 2:1 input mux, and digital attenuation.

The CS53L32A operates from a +1.8 V to +3.3 V supply. These features are ideal for portable MP3 players, MD recorders/players, digital camcorders, PDAs, set-top boxes, and other portable systems that require extremely low power consumption in a minimum of space.

ORDERING INFORMATION

CS53L32A-KZ	20-pin TSSOP,	-10 to 70 °C
CDB53L32A	Evaluation Board	



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; GND = 0 V Logic "1" = VL = 1.8 V; Logic "0" = GND = 0 V; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter	Symbol	Base-rate Mode			High-rate Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics for VA = 1.8 V								
Dynamic Range A-weighted		TBD	93	-	TBD	94	-	dB
unweighted		TBD	90	-	TBD	91	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit -1 dB		-	-88	TBD	-	-88	TBD	dB
-20 dB		-	-70	-	-	-71	-	dB
-60 dB		-	-30	-	-	-31	-	dB
16-Bit -1 dB		-	-86	-	-	-86	-	dB
-20 dB		-	-68	-	-	-68	-	dB
-60 dB		-	-28	-	-	-28	-	dB
Dynamic Range (PGA on)*								
0 dB Gain								
A-weighted		-	90	-	-	89	-	dB
unweighted		-	87	-	-	86	-	dB
12 dB Gain								
A-weighted		-	85	-	-	86	-	dB
unweighted		-	82	-	-	83	-	dB
Total Harmonic Distortion + Noise (PGA on)* (Note 1)	THD+N							
0 dB Gain								
18 to 24-Bit -1 dB		-	85	-	-	84	-	dB
12 dB Gain								
18 to 24-Bit -1 dB		-	83	-	-	82	-	dB
Interchannel Isolation 1 kHz		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
HPF frozen with HPFREEZE		-	TBD	-	-	TBD	-	
Analog Input Characteristics for VA = 3.0 V								
Dynamic Range A-weighted		TBD	96	-	TBD	98	-	dB
unweighted		TBD	93	-	TBD	95	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit -1 dB		-	-88	TBD	-	-85	TBD	dB
-20 dB		-	-73	-	-	-75	-	dB
-60 dB		-	-33	-	-	-35	-	dB
16-Bit -1 dB		-	-86	-	-	-83	-	dB
-20 dB		-	-68	-	-	-65	-	dB
-60 dB		-	-28	-	-	-28	-	dB

*PGA : Programmable Gain Amplifier

Note: 1. Referenced to typical full-scale differential input voltage (0.5 Vrms).

ANALOG CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-rate Mode Min	High-rate Mode Typ	High-rate Mode Max	Unit
Total Harmonic Distortion + Noise (PGA on)* (Note 1)	THD+N							
0 dB Gain 18 to 24-Bit -1 dB		-	78	-	-	77	-	dB
12 dB Gain 18 to 24-Bit -1 dB		-	73	-	-	76	-	dB
Interchannel Isolation 1 kHz		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
HPF frozen with HPFREEZE		-	TBD	-	-	TBD	-	
Full Scale Input Voltage		TBD	VA/3.6	TBD	TBD	VA/3.6	TBD	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
Programmable Gain Characteristics								
Gain Step Size		-	1.0	-	-	1.0	-	dB
Absolute Gain Step Error		-	-	TBD	-	-	TBD	dB
A/D Decimation Filter Characteristics **(Note 2)**								
Passband (Note 3)		0	-	23.5	0	-	47.5	kHz
Passband Ripple		-0.08	-	+0.17	-0.09	-	0	dB
Stopband (Note 3)		27.5	-	-	64.1	-	-	kHz
Stopband Attenuation (Note 4)		-60.3	-	-	-48.4	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 5)	t_{gd}	-	10/Fs	-	-	2.7/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0.03	-	-	0.007	µs
High Pass Filter Characteristics								
Frequency Response -3 dB (Note 3)		-	3.7	-	-	3.7	-	Hz
-0.1 dB		-	24.2	-	-	24.2	-	Hz
Phase Deviation @ 20 Hz (Note 3)		-	10	-	-	10	-	Degree
Passband Ripple (Note 2)		-	-	0.17	-	-	0.09	dB

*PGA : Programmable Gain Amplifier

Notes:
2. Filter response is not tested but is guaranteed by design.
3. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.
4. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).
5. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Units
Power Supplies									
Power Supply Current-	VA=1.8 V	I_A	-	6.0	-	-	7.6	-	mA
Normal Operation	VL=1.8 V	I_{D_IO}	-	150	-	-	300	-	µA
Power Supply Current-	VA=1.8 V	I_A	-	100	-	-	250	-	µA
Power Down Mode (Note 6)	VL=1.8 V	I_{D_IO}	-	0	-	-	0	-	µA
Power Supply Current-	VA=3.0 V	I_A	-	9	-	-	11.5	-	mA
Normal Operation	VL=3.0 V	I_{D_IO}	-	260	-	-	520	-	µA
Power Supply Current-	VA=3.0 V	I_A	-	250	-	-	500	-	µA
Power Down Mode	VL=3.0 V	I_{D_IO}	-	0	-	-	0	-	µA
Total Power Dissipation-	All Supplies=1.8 V		-	11	TBD	-	14.5	TBD	mW
Normal Operation	All Supplies=3.0 V		-	28	TBD	-	36	TBD	mW
Package Thermal Resistance		θ_{JA}	-	75	-	-	75	-	°C/Watt
Power Supply Rejection Ratio	(1 kHz)	PSRR	-	60	-	-	60	-	dB
(Note 7)	(60 Hz)		-	40	-	-	40	-	dB
Chip Power									
Analog/Digital Converter			-	11	-	-	14.5	-	mA
A/D Converter & Programmable Gain Amplifier			-	13	-	-	16.5	-	mA

Notes: 6. Power Down Mode is defined as the chip being held in reset with MCLK being applied. To lower power consumption further, remove MCLK.

7. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 5.

DIGITAL CHARACTERISTICS (T_A = 25° C; VL = 1.7 V - 3.6 V; GND = 0 V)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7•VL	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3•VL	V
High-Level Output Voltage	V_{OH}	0.7•VL	-	-	V
Low-Level Output Voltage	V_{OL}	-	-	0.3•VL	V
Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

ABSOLUTE MAXIMUM RATINGS (GND = 0 V; all voltages with respect to ground.)

Parameters		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA	-0.3	4.0	V
	Digital I/O	VL	-0.3	4.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (GND = 0V; all voltages with respect to ground.)

Parameters		Symbol	Min	Typ	Max	Units
Ambient Temperature		T_A	-10	-	70	°C
DC Power Supplies:	Positive Analog	VA	1.7	-	3.6	V
	Digital I/O	VL	1.7	-	3.6	V

SWITCHING CHARACTERISTICS (T_A = -10 to 70° C; VA = 1.7 V - 3.6 V; Inputs: Logic 0 = GND, Logic 1 = VL, C_L = 20 pF)

Parameters		Symbol	Min	Typ	Max	Units
Input Sample Rate	Base Rate Mode High Rate Mode	Fs Fs	2 50	- -	50 100	kHz kHz
MCLK Pulse Width High	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 1024		8	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 768		10	-	-	ns
MCLK Pulse Width High	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width Low	MCLK/LRCK = 512		15	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 384 or 192		21	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 384 or 192		21	-	-	ns
MCLK Pulse Width High	MCLK / LRCK = 256 or 128		31	-	-	ns
MCLK Pulse Width Low	MCLK / LRCK = 256 or 128		31	-	-	ns
Master Mode						
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDATA Valid		t_{sdo}	0	-	20	ns
SCLK Duty Cycle			40	50	60	%
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	-	ns
SCLK Period	Base Rate Mode High Rate Mode	t_{sclkw} t_{sclkw}	$\frac{1}{(128)Fs}$ $\frac{1}{(64)Fs}$	- -	- -	ns ns
SCLK Falling to LRCK Edge		t_{slrd}	-20	-	20	ns
SCLK Falling to SDATA Valid	Base Rate Mode High Rate Mode	t_{dss} t_{dss}	- -	- -	$\frac{1}{(512)Fs}$ $\frac{1}{(256)Fs}$	ns ns

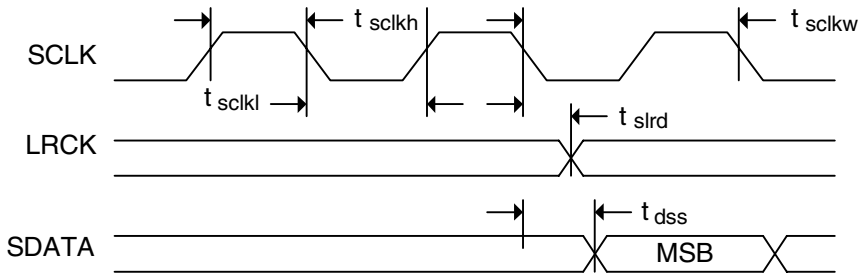


Figure 1. SCLK to LRCK and SDATA, Slave Mode

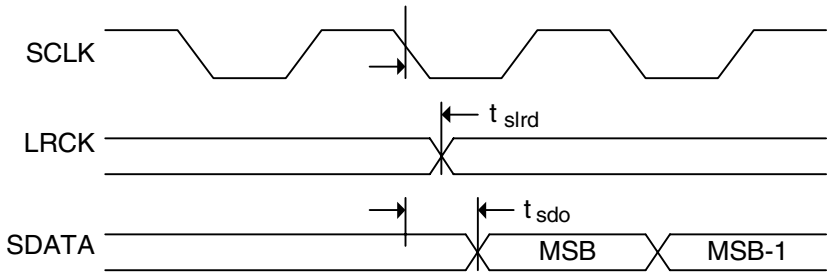


Figure 2. SCLK to LRCK and SDATA, Master Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - TWO WIRE MODE

(T_A = 25° C; VL = 1.7 V - 3.6 V; Inputs: logic 0 = GND, logic 1 = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
Two Wire Mode				
SCL Clock Frequency	f_{scl}	-	100	KHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 8)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	25	ns
Fall Time of Both SDA and SCL Lines	t_f	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Note: 8. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

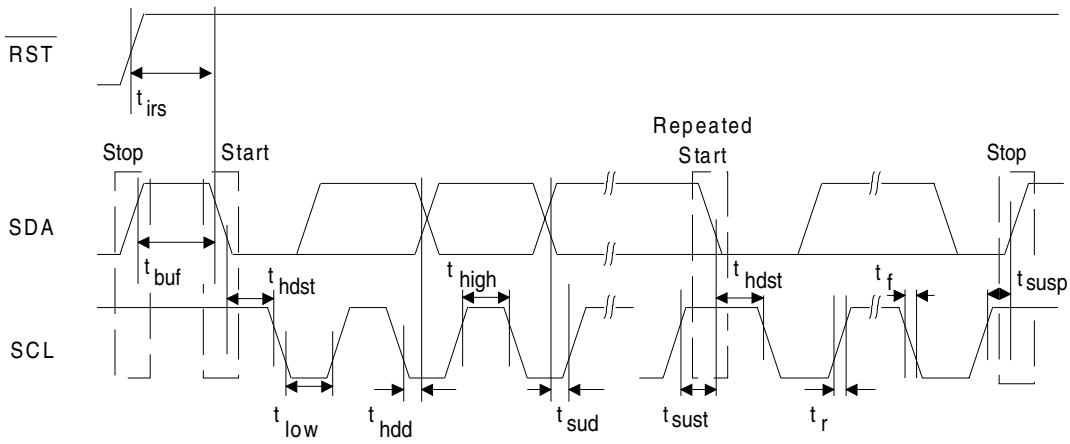


Figure 3. Control Port Timing - Two Wire Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(T_A = 25 °C; VL = 1.7V - 3.6V; Inputs: logic 0 = GND, logic 1 = VL, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling	(Note 9)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 10)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 11)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 11)	t_{f2}	-	100	ns

Notes: 9. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

10. Data must be held for sufficient time to bridge the transition time of CCLK.

11. For F_{SCLK} < 1 MHz.

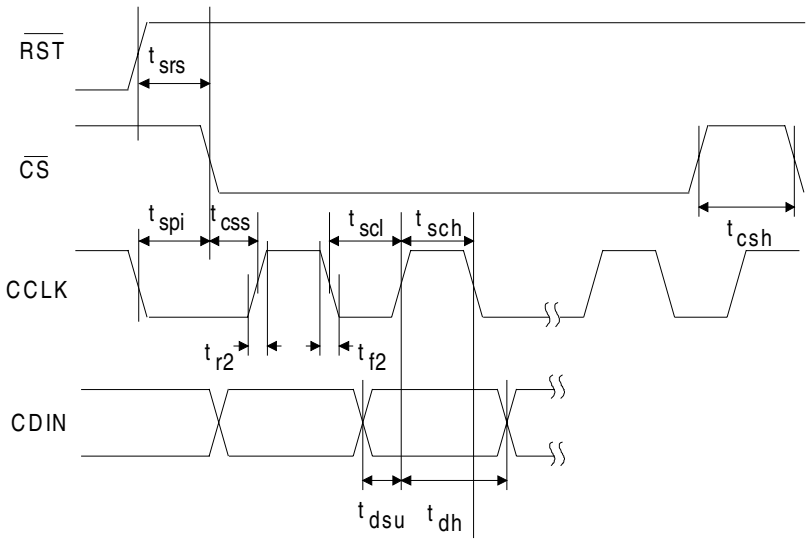


Figure 4. Control Port Timing - SPI Mode

2. TYPICAL CONNECTION DIAGRAM

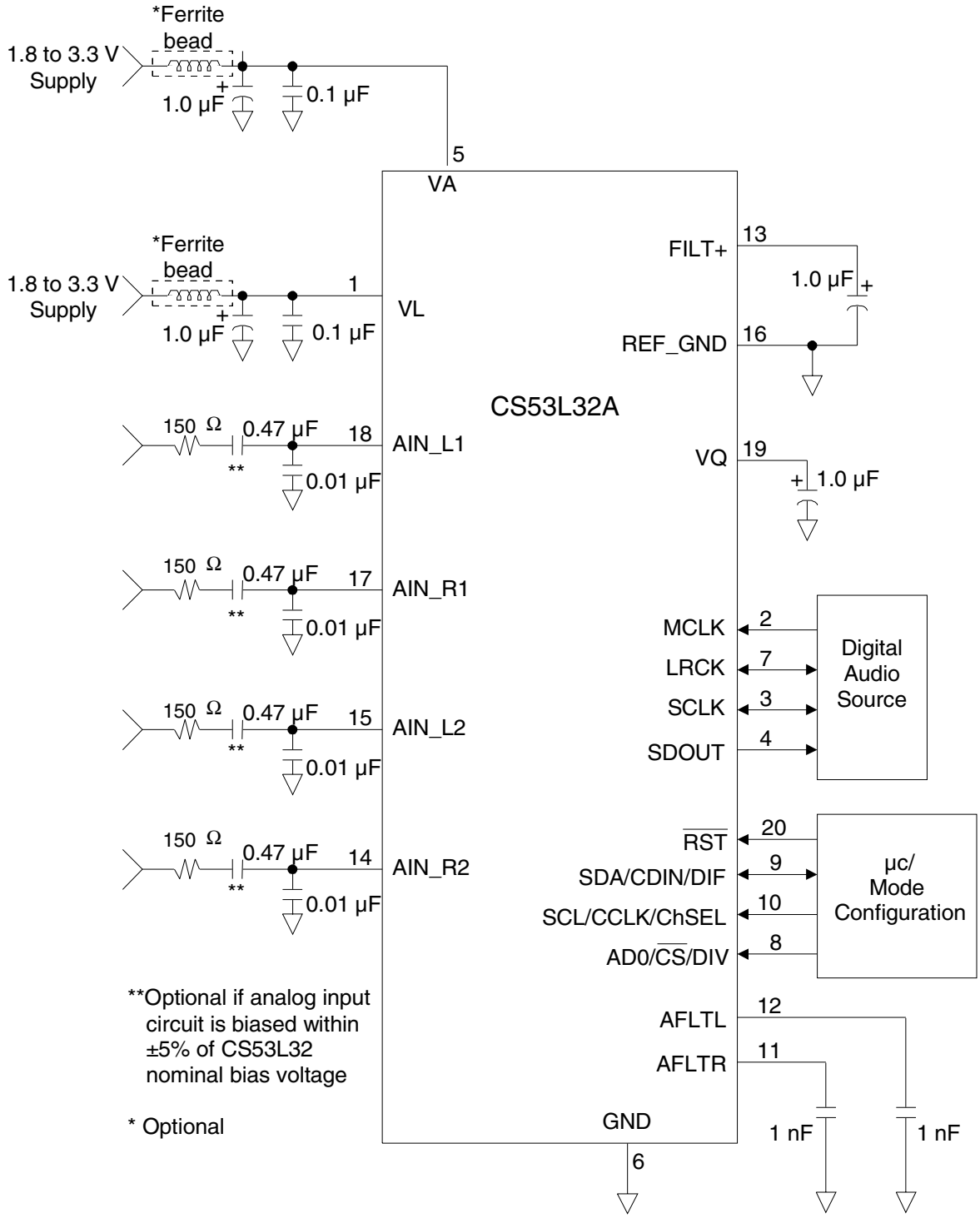


Figure 5. Typical Connection Diagram

3. REGISTER QUICK REFERENCE

** “default” ==> bit status after power-up-sequence or reset.

3.1 I/O and Power Control (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN
0	0	0	0	0	0	1	0

BOOST — 20 dB Digital Gain
Default = ‘0’
0 - Disabled
1 - Enabled

AINMUX — Analog Input Mulitplexer
Default =’0’.
0 - AIN_L1/AIN_R1 direct to A/D (default)
1 - AIN_L2/AIN_R2 direct to A/D
2 - AIN_L2/AIN_R2 through PGA to A/D
3 - Reserved

PDN — Power-Down
Default =’1’.
0 - Disabled
1 - Enabled

CP_EN — Control Port Enable
Default =’0’.
0 - Disabled
1 - Enabled

3.2 Interface Control (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0
0	0	0	0	0	0	0	0

MCLKDIV — Master Clock Divider
Default =’0’.
0 - Disabled
1 - Enabled

RATIO1-0 — Master Clock Ratio
Default =’0’.
0 - 128x (default)
1 - 192x
2 - 256x
3 - 384x

MASTER — Master Mode
Default =’0’.
0 - Slave Mode
1 - Master Mode

DIF2-0 Digital Interface Format
Default = '0'.
0 - I^2S, up to 24-bit Data, Data valid on positive edge of SLCK (default)
1 - Left Justified, up to 24-bit Data, Data valid on positive edge of SLCK
2 - Reserved
3 - Right Justified, 16-bit Data, Data valid on positive edge of SLCK
4 - Right Justified, 24-bit Data, Data valid on positive edge of SLCK
5 - Right Justified, 18-bit Data, Data valid on positive edge of SLCK
6 - Right Justified, 20-bit Data, Data valid on positive edge of SLCK
7 - Reserved

3.3 Analog I/O Control (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE
0	0	1	1	0	0	0	0

MUTEL Left Channel Mute
Default = '0'.
0 - Disabled
1 - Enabled

MUTER Right Channel Mute
Default = '0'.
0 - Disabled
1 - Enabled

SOFT Soft Digital/Analog Volume Control
Default = '1'.
0 - Disabled
1 - Enabled

ZC Analog Zero Cross Detection Control
Default = '1'.
0 - Disabled
1 - Enabled

INDVC Independent Volume Control Enable
Default = '0'.
0 - Disabled
1 - Enabled

L=R Left Channel Volume = Right Channel Volume
Default = '0'.
0 - Left channel volume is determined by the left channel volume control registers and right channel volume is determined by the right channel volume control registers.
1 - Left and right channel volumes are determined by the left channel volume control registers and the right channel volume control registers are ignored.

HPFREEZE High-pass filter freeze
Default = '0'.
0 - Disabled
1 - Enabled

3.4 Left Channel Digital Volume Control (address 04h)

3.5 Right Channel Digital Volume Control (address 05h)

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

VOL7-0 Volume
Default = '0'.
(Refer to Table 13)

3.6 Analog Gain Control (address 06h)

7	6	5	4	3	2	1	0
LVOL3	LVOL2	LVOL1	LVOL0	RVOL3	RVOL2	RVOL1	RVOL0
0	0	0	0	0	0	0	0

LVOL3-0 Left Analog Gain
Default = '0'.
(Refer to Table 14)

RVOL3-0 Right Analog Gain
Default = '0'.
(Refer to Table 14)

3.7 Clip Detection Status (address 07h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CLIP_L_FLAG	CLIP_R_FLAG
0	0	0	0	0	0	0	0

CLIP_L_FLAG Left Channel Clip Detection

CLIP_R_FLAG Right Channel Clip Detection
Default = '0'.
0 - No Clipping Detected
1 - Clipping Detected

4. REGISTER DESCRIPTION

4.1 GAIN ENABLE

I/O and Power Control Register (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

Applies a 20 dB digital gain to the input signal, regardless of the input path.

4.2 ANALOG INPUT MULTIPLEXER

I/O and Power Control Register (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - AIN_L1/AIN_R1 direct to A/D

Function:

The analog input multiplexer selects the input channel as well as the input path associated with various gain stages.

AINMUX	MODE
0	AIN_L1/AIN_R1 direct to A/D
1	AIN_L2/AIN_R2 direct to A/D
2	AIN_L2/AIN_R2 through PGA to A/D
3	Reserved

Table 1. Analog Input Options

4.3 POWER-DOWN

I/O and Power Control Register (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

1 - Enabled

Function:

The entire device will enter a low-power state whenever this function is activated. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained when this mode is enabled.

PDN	MODE
0	Disabled
1	Enabled

Table 2. Power-Down Enable

4.4 CONTROL PORT ENABLE

I/O and Power Control Register (address 01h)

7	6	5	4	3	2	1	0
RESERVED	BOOST	AINMUX1	AINMUX0	RESERVED	RESERVED	PDN	CP_EN

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

The CS53L32A will enter Control Port mode when this bit is enabled. Stand-Alone is the default power up mode. See Section 6.3, *Recommended Power-up Sequence,* for more details.

CP_EN	MODE
0	Disabled
1	Enabled

Table 3. Control Port Enable

4.5 MASTER CLOCK DIVIDE

Interface Control Register (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

Divides MCLK by two prior to all other chip circuitry.

MCLKDIV	MODE
0	Disabled
1	Enabled

Table 4. Master Clock Divide Select

4.6 MASTER CLOCK RATIO

Interface Control Register (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - 128x

Function:

Sets the ratio of MCLK to LRCK.

RATIO1,0	MCLK/LRCK RATIO (MCLKDIV=0)	MCLK/LRCK RATIO (MCLKDIV=1)
0	128x	256x
1	192x	384x
2	256x	512x
3	384x	768x

Table 5. MCLK/LRCK Ratios

4.7 MASTER MODE

Interface Control Register (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Slave Mode

Function:

Configures the device for master or slave operation when in Control Port mode.

MASTER	MODE
0	Slave Mode
1	Master Mode

Table 6. Master/Slave Mode Selection

4.8 DIGITAL INTERFACE FORMAT

Interface Control Register (address 02h)

7	6	5	4	3	2	1	0
RESERVED	MCLKDIV	RATIO1	RATIO0	MASTER	DIF2	DIF1	DIF0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Format 0 (I^2S, up to 24-bit data, Data valid on positive edge of SCLK)

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 17 through 20.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	I^2S, up to 24-bit Data, Data valid on positive edge of SCLK	0	17
0	0	1	Left Justified, up to 24-bit Data, Data valid on positive edge of SCLK	1	18
0	1	0	Reserved	2	-
0	1	1	Right Justified, 16-bit Data, Data valid on positive edge of SCLK	3	18
1	0	0	Right Justified, 24-bit Data, Data valid on positive edge of SCLK	4	19
1	0	1	Right Justified, 18-bit Data, Data valid on positive edge of SCLK	5	20
1	1	0	Right Justified, 20-bit Data, Data valid on positive edge of SCLK	6	21
1	1	1	Reserved	7	-

Table 7. Digital Interface Format

4.9 LEFT/RIGHT CHANNEL MUTE

Analog I/O Control (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

Digital mute of the left and right channels.

MUTEL/ MUTER	MODE
0	Disabled
1	Enabled

Table 8. Left/Right Channel Mute Enable

4.10 SOFT RAMP AND ZERO CROSS ENABLE

Analog I/O Control Register (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

11 - Soft Ramp and Zero Cross enabled

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented via an incremental ramp. Digital volume control is ramped from the current level to the new level at a rate of 1/8 dB per left/right clock period. Analog volume control is ramped in 1 dB steps every 8 left/right clock periods in Base Rate mode, and 1 dB every 16 left/right clock periods in High Rate mode.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 512 sample periods in BRM or 1024 sample periods in HRM (approximately 10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1 dB steps and be implemented on a signal zero crossing. The level change will occur after a timeout period of 512 sample periods in BRM or 1024 sample periods in HRM (approximately 10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

SOFT/ZC	ANALOG VOLUME CONTROL MODES
00	Change volume immediately
01	Change volume at next zero cross time
10	Change volume in 1 dB steps
11	Change volume in 1 dB steps at every zero cross time

Table 9. Analog Volume Control

.

SOFT	DIGITAL VOLUME CONTROL MODES
0	Change volume immediately
1	Change volume in1/8 dB steps

Table 10. Digital Volume Control

4.11 INDEPENDENT VOLUME CONTROL ENABLE

Analog I/O Control Register (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

When this function is disabled, the AIN_L and AIN_R volume levels are controlled by the Left and Right Volume Control registers and the Independent Analog Gain Control registers are ignored.

When this function is enabled, the volume levels are determined by both the Volume Control registers and the Independent Analog Gain Control registers.

INDVC	MODE
0	Disabled
1	Enabled

Table 11. Independent Volume Control Enable

4.12 LEFT CHANNEL VOLUME = RIGHT CHANNEL VOLUME

Analog I/O Control (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

When this function is disabled, the left channel volume is determined by the left channel volume control register and right channel volume is determined by the right channel volume control register.

When enabled, the left and right channel volumes are determined by the left channel volume control register and the right channel volume control register is ignored.

4.13 HIGH-PASS FILTER FREEZE

Analog I/O Control Register (address 03h)

7	6	5	4	3	2	1	0
MUTEL	MUTER	SOFT	ZC	RESERVED	INDVC	L=R	HPFREEZE

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - Disabled

Function:

The high-pass filter works by continuously subtracting a measure of the dc offset from the output of the decimation filter. If the HPFREEZE bit is taken low during normal operation, the current value of the dc offset is frozen and this dc offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system calibration by:

1) removing the signal source at the input to the subsystem containing the CS53L32A,

2) running the CS53L32A with the HPFREEZE bit high until the filter settles, approximately one second,

3) taking the HPFREEZE bit low, thus disabling the high-pass filter and freezing the stored dc offsett.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS53L32A.

HPFREEZE	MODE
0	Frozen
1	Enabled

Table 12. High-Pass Filter Enable

4.14 VOLUME CONTROL

Left Channel Volume Control Register (address 04h)

Right Channel Volume Control Register (address 05h)

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - 0 dB (No attenuation)

Function:

The Volume Control allows the user to alter the signal level in 1 dB increments from +12 to -96 dB, when the INDVC bit is disabled. When INDVC is enabled, the Volume Control can be altered in 1 dB increments from 0 to -96 dB. Volume settings are decoded as shown in Table 13, using a 2's complement code. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Analog I/O Control register. All volume settings less than -96 dB are equivalent to muting the channel.

Binary Code	Decimal Value	Volume Setting
00001010	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Table 13. Example Volume Settings

4.15 LEFT/RIGHT ANALOG GAIN

ADC Independent Analog Gain Control Register (address 06h)

7	6	5	4	3	2	1	0
LVOL3	LVOL2	LVOL1	LVOL0	RVOL3	RVOL2	RVOL1	RVOL0

Access:

R/W in Two Wire Mode and write only in SPI.

Default:

0 - 0 dB (No Gain)

Function:

The level of the left and right analog channels can be adjusted in 1 dB increments as dictated by the Soft Ramp and Zero Cross bits from 0 to +12 dB when routed throgh the PGA via the AINMUX bits in Control Port mode or the CH_SEL pins in Stand-Alone mode. Levels are decoded as shown in Table 14. Levels above +12 dB are interpreted as +12 dB.

Binary Code	Decimal Value	Volume Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 14. Example Gain Settings

4.16 CLIP DETECTION

Clip Detection Status Register (address 07h)

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CLIP_L_FLAG	CLIP_R_FLAG

Access:

Read only in Two Wire Mode and unavailable in SPI.

Default:

0 - No Clipping Detected

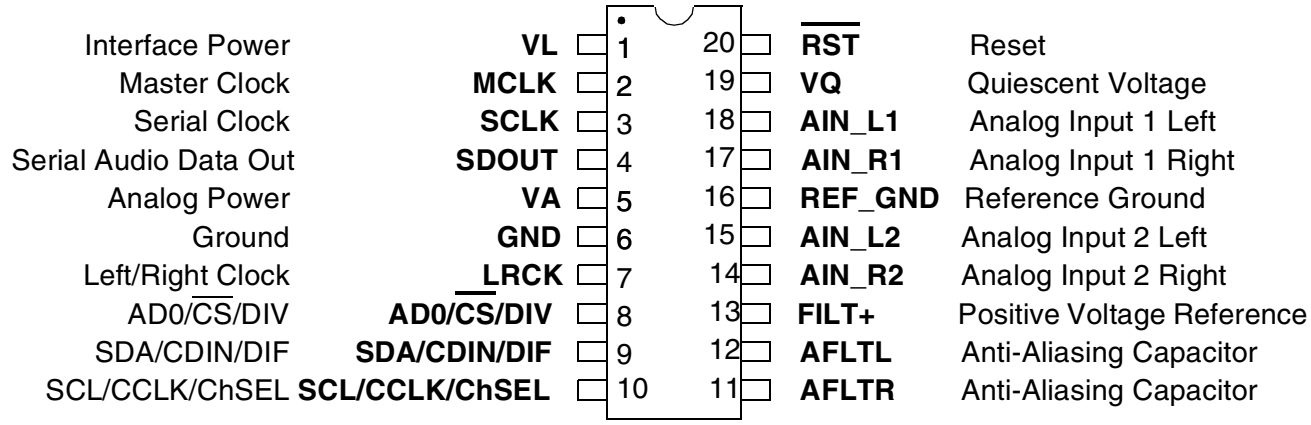
Function:

The Clip Flags indicate when there is an over-range condition anywhere in the CS53L32A internal signal path. These bits are “sticky”. They constantly monitor the ADC signal path and are set to 1 when an over-range condition occurs. They are reset to 0 when read.

CLIP_L_FLAG CLIP_R_FLAG	Condition
0	Signal within normal range
1	Signal is over-range

Table 15. Clip Detection Status Bits

5. PIN DESCRIPTION



Interface Power	1	**VL** (*Input*) - Digital interface power supply. Typically 1.8 to 3.3 VDC.
Master Clock	2	**MCLK** (*Input*) - The master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Base Rate Mode (BRM) and 128x, 192x, 256x, 384x the input sample rate in High Rate Mode (HRM). Table 18 illustrates several standard audio sample rates and the required master clock frequencies.
Serial Clock	3	**SCLK** (*Input/Output*) - Clocks the individual bits of the serial data out of the SDOUT pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF2-0 bytes when in Control Port mode or by the DIF1-0 pins when in Stand-Alone mode.
Serial Audio Data Out	4	**SDOUT** (*Output*) - Two's complement MSB-first serial data is output on this pin. The data is clocked out of SDOUT via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF2-0 bytes when in Control Port mode or by the DIF pin when in Stand-Alone mode.
Analog Power	5	**VA** (*Input*) - Analog power supply. Typically 1.8 to 3.3 VDC.
Ground	6	**GND** (*Input*) - Ground Reference.

Sample Rate (kHz)	MCLK (MHz)								
	HRM				BRM				
	128x	192x	256x*	384x*	256x	384x	512x	768x*	1024x*
32	4.0960	6.1440	8.1920	12.2880	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	5.6448	8.4672	11.2896	16.9344	11.2896	16.9344	22.5792	32.7680	45.1584
48	6.1440	9.2160	12.2880	18.4320	12.2880	18.4320	24.5760	36.8640	49.1520
64	8.1920	12.2880	16.3840	24.5760	-	-	-	-	-
88.2	11.2896	16.9344	22.5792	33.8688	-	-	-	-	-
96	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-

** MCLKDIV = 1 in Control Port mode or DIV= Hi when in Stand-Alone mode*

Table 18. Common Clock Frequencies

Left/Right Clock	7	**LRCK** (*Input*/*Output*) - The Left/Right clock determines which channel is currently being output on the serial audio data line SDOUT. The frequency of the Left/Right clock must be at the input sample rate. The required relationship between the Left/Right clock, serial clock and serial data is defined by the DIF2-0 bytes when in Control Port mode or by the DIF pin when in Stand-Alone mode.
Address Bit	8	**AD0/$\overline{CS}$ (Control Port Mode)** (*Input*) - In Two Wire mode, AD0 is a chip address bit. $\overline{CS}$ is used to enable the control port interface in SPI mode.
MCLK Divide Enable	8	**DIV (Stand-Alone Mode)** (*Input*) - When high, the chip will enter High Rate Mode. When this pin is low, the chip will enter Base Rate Mode.
Serial Control Data I/O	9	**SDA/CDIN (Control Port Mode)** (*Input*/*Output*) - In Two Wire mode,SDA is a data I/O line. CDIN is the input data line for the control port interface in SPI mode.
Digital Interface Format	9	**DIF (Stand-Alone Mode)** (*Input*) - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format.

DIF	DESCRIPTION
0	I^2S, up to 24-bit data
1	Left Justified, up to 24-bit data

Table 16. Digital Interface Format - DIF (Stand-Alone Mode)

Serial Control Interface Clock	10	**SCL/CCLK (Control Port Mode)** (*Input*) **-** Clocks the serial control data into or from SDA/CDIN/DIF.
Channel Select	10	**ChSEL (Stand-Alone Mode)** (*Input)* - The analog data path is determined by the Channel Select bit. These options are detailed in Table 17.

ChSEL	DESCRIPTION
0	Channel 1 directly to A/D
1	Channel 2 with 32dB of gain

Table 17. Channel Select Options

Anti-Aliasing Capacitors	11, 12	**AFLTR, AFLTL** (*Output*) - Anti-aliasing capacitors for the left and right channels. An external capacitor is required from AFLTR and AFLTL to ground, as shown in Figure 4. AFLTR and AFLTL are not intended to supply external current, and any current drawn from these pins will alter device performance.
Positive Voltage Reference	13	**FILT+** (*Output)* - Positive reference for internal sampling circuits. An external capacitor is required from FILT+ to ground, as shown in Figure 5. The recommended value will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedence of 250 kΩ and any current drawn from this pin will alter device performance.
Analog Inputs	14, 15, 17, and 18	**AIN_R1, AIN_L1, AIN_R2, AIN_L2** (*Input*) - Channel 1/Channel 2 analog inputs.
Reference Ground	16	**REF_GND** (*Input*) - Ground reference for the internal sampling circuits. Must be connected to ground.

Quiescent Voltage	19	**VQ** (*Output*) - Filter connection for internal A/D converter quiescent reference voltage. A capacitor must be connected from VQ to ground. VQ is not intended to supply external current. VQ has a typical source impedence of 250 kΩ and any current drawn from this pin will alter device performance.
Reset	20	**$\overline{\text{RST}}$** (*Input*) - The device enters a low power mode and all internal registers are reset to their default settings, including the control port, when low. When high, the control port becomes operational and the PDN bit must be cleared before normal operation will occur. The control port cannot be accessed when Reset is low.

6. APPLICATIONS

6.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS53L32A requires careful attention to power supply and grounding arrangements to optimize performance. Figure 5 shows the recommended power arrangement with VA and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible.

6.2 Oversampling Modes

The CS53L32A operates in one of two oversampling modes. Base Rate Mode supports input sample rates up to 50 kHz while High Rate Mode supports input sample rates up to 100 kHz. See Table 18 for more details.

6.3 Recommended Power-up Sequence

1) Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and VQ will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low and will initiate the Stand-Alone power-up sequence. The control port will be accesable at this time. If control port operation is desired, write the CP_EN bit prior to the completion of the Stand-Alone power-up sequence, approximately 1024 LRCK cycles. Writing this bit will halt the Stand-Alone power-up sequence and initialize the control port to its default settings. The desired register settings can be loaded while keeping the PDN bit set to 1.
3) If Control Port mode is selected via the CP_EN bit, set the PDN bit to 0 which will initiate the power-up sequence, which requires approximately 50 µS.

7. CONTROL PORT INTERFACE

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and Two Wire. If Two Wire operation is desired, AD0/$\overline{\text{CS}}$ should be tied to VL or GND. If the CS53L32A ever detects a high to low transition on AD0/$\overline{\text{CS}}$ after power-up, SPI mode will be selected.

7.1 SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS53L32A chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK. All CS53L32A registers are write-only in SPI mode.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP.

The CS53L32A has a MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers.

7.2 Two Wire Mode

In Two Wire mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VL or GND as required. The upper 6 bits of the 7 bit address field must be 001000. To communicate with the CS53L32A the LSB of the chip address field, which is the first byte sent to the CS53L32A, should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. See Section 7.3, *Memory Address Pointer (MAP)*. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

Note: The Two-Wire control port mode is compatible with the I^2C protocol.

7.3 MEMORY ADDRESS POINTER (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR (Auto MAP Increment Enable)
Default = '0'.
0 - Disabled
1 - Enabled

MAP0-2 (Memory Address Pointer)
Default = '000'.

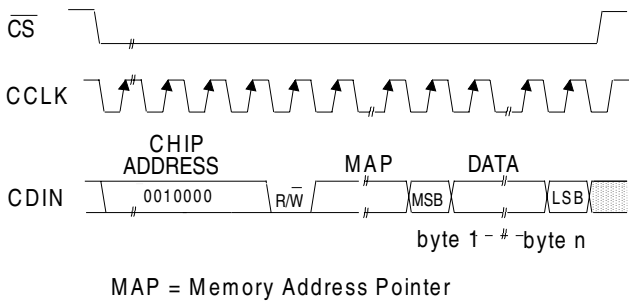
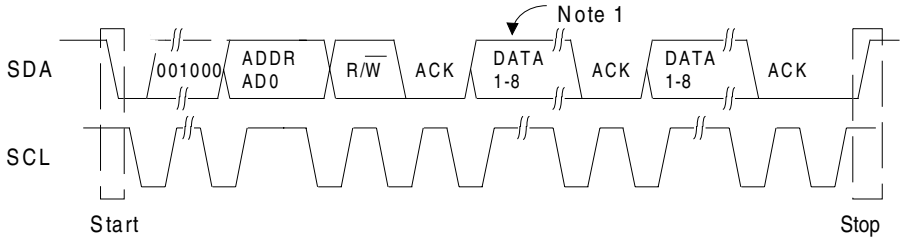


Figure 6. Control Port Timing, SPI Mode



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 7. Control Port Timing, Two Wire Mode

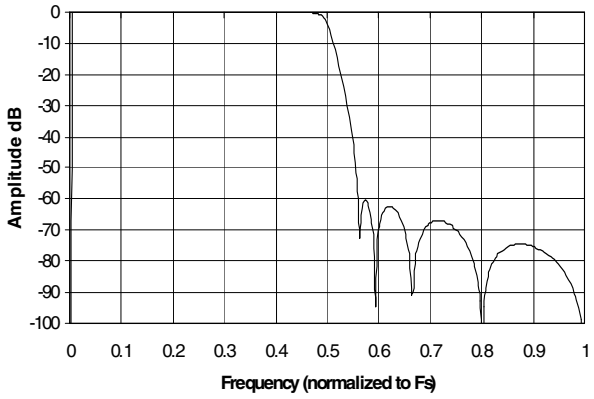


Figure 8. Base-Rate Stopband Rejection

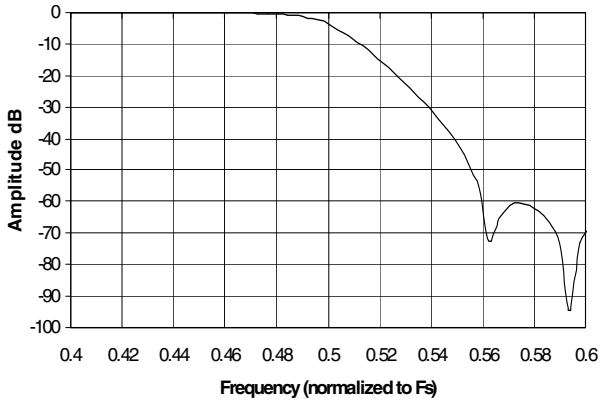


Figure 9. Base-Rate Transition Band

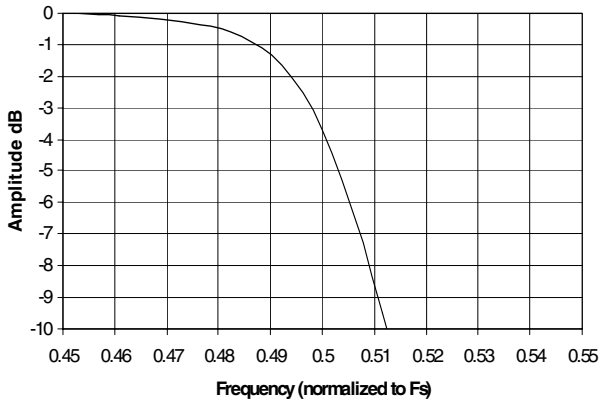


Figure 10. Base-Rate Transition Band (Detail)

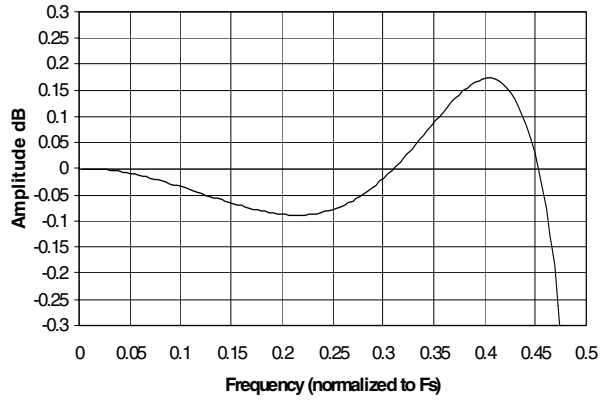


Figure 11. Base-Rate Passband Ripple

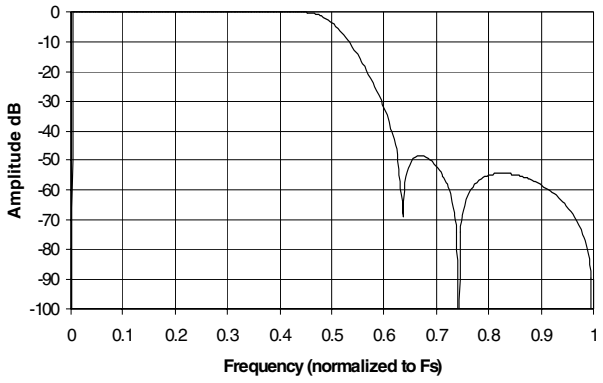


Figure 12. High-Rate Stopband Rejection

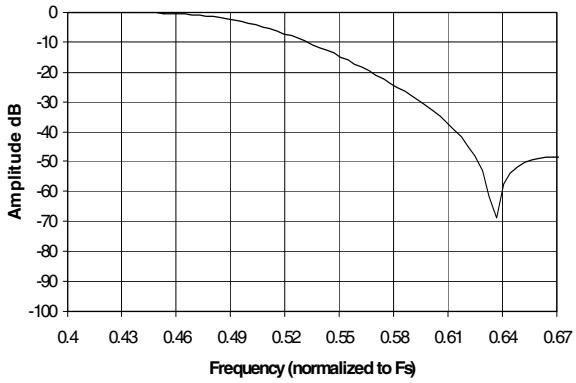


Figure 13. High-Rate Transition Band

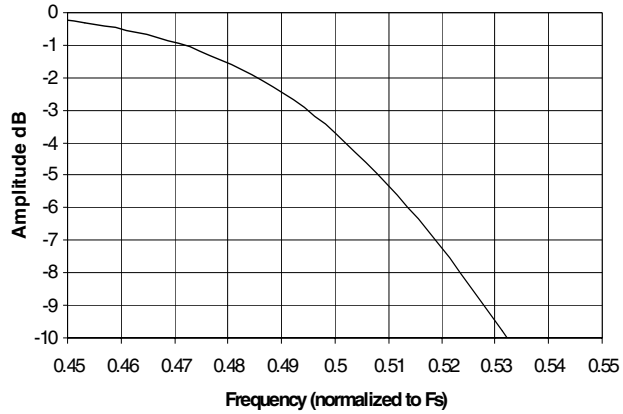


Figure 14. High-Rate Transition Band (Detail)

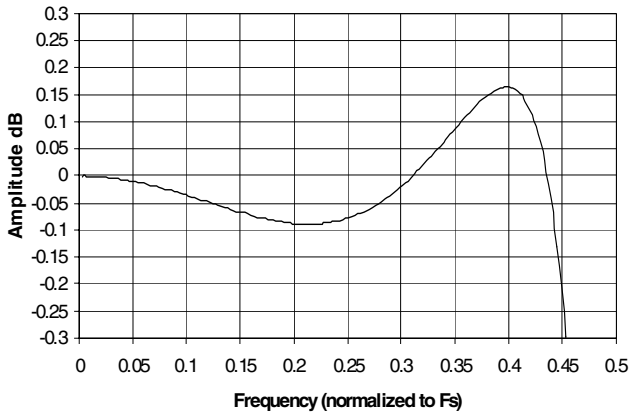


Figure 15. High-Rate Passband Ripple

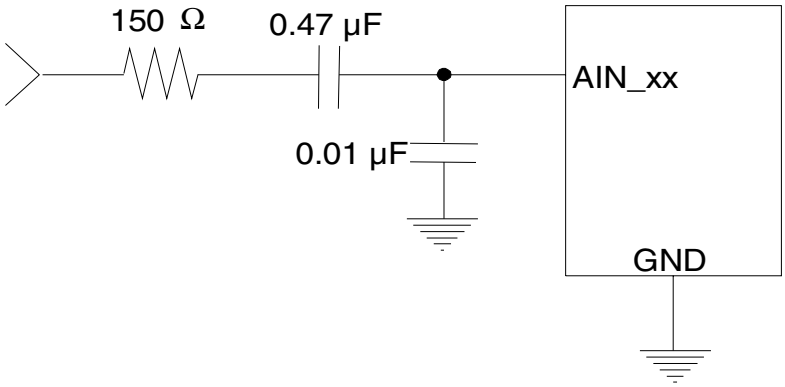
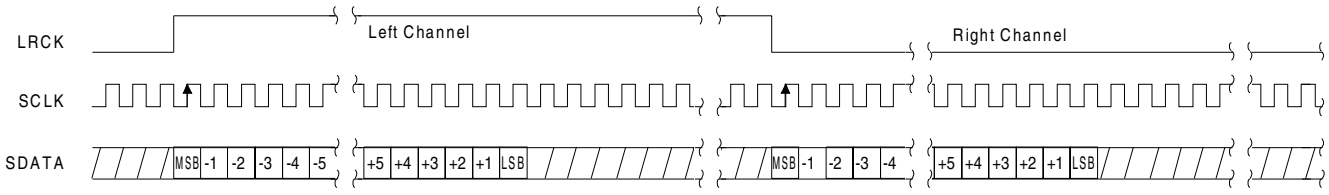
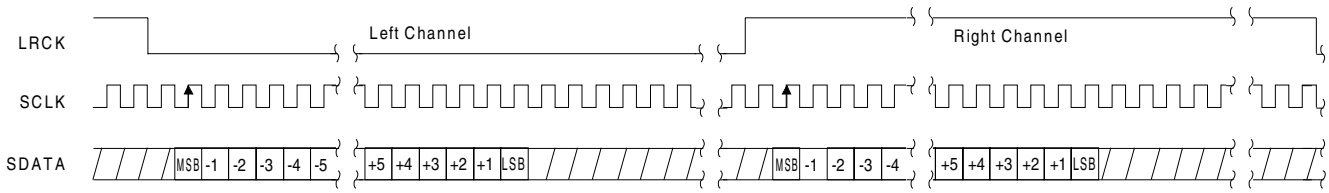


Figure 16. Line Input Test Circuit



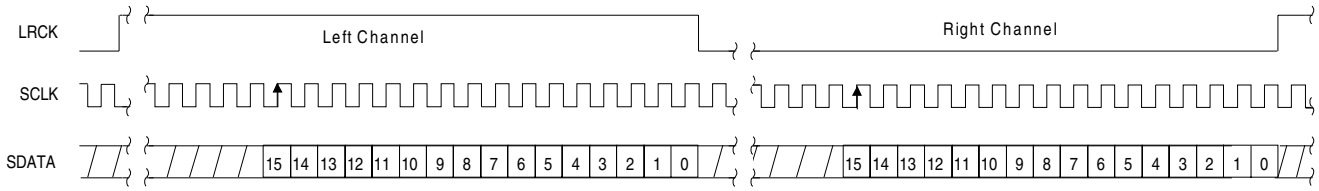
Left Justified, up to 24-Bit Data. Data Valid on Rising Edge of SCLK.

Figure 18. CS53L32A Control Port Mode - Serial Audio Format 1



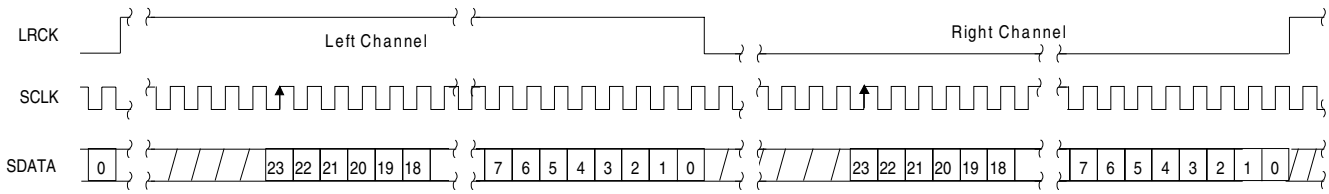
I²S, up to 24-Bit Data. Data Valid on Rising Edge of SCLK.

Figure 17. CS53L32A Control Port Mode - Serial Audio Format 0 (I^2S)



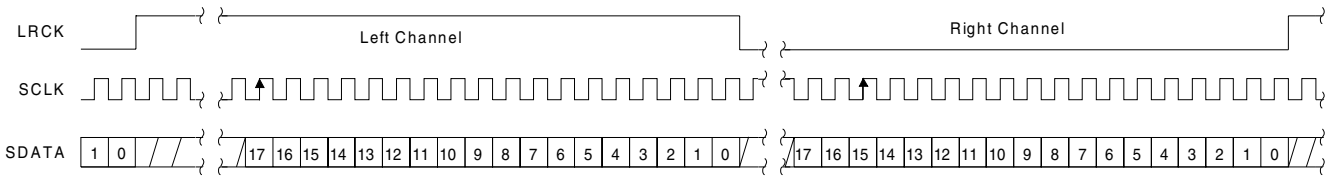
Right Justified, 16-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 32 Cycles per LRCK Period.

Figure 19. CS53L32A Control Port Mode - Serial Audio Format 3



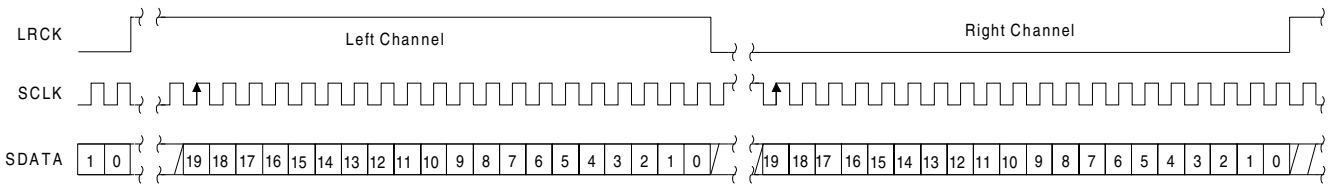
Right Justified, 24-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 48 Cycles per LRCK Period.

Figure 20. CS53L32A Control Port Mode - Serial Audio Format 4



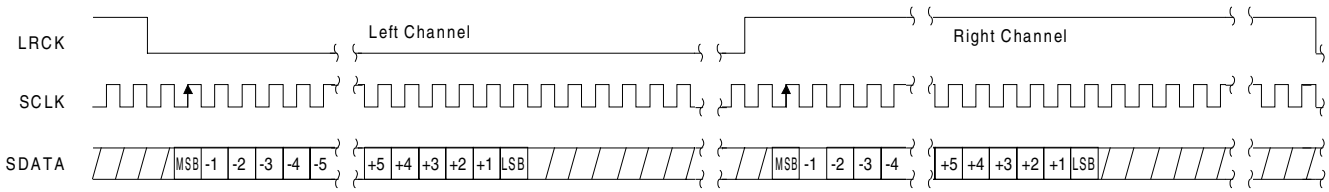
Right Justified, 18-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 36 Cycles per LRCK Period.

Figure 21. CS53L32A Control Port Mode - Serial Audio Format 5



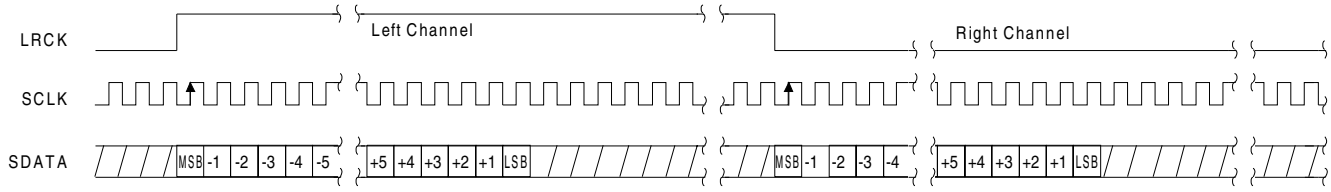
Right Justified, 20-Bit Data. Data Valid on Rising Edge of SCLK. SCLK Must Have at Least 40 Cycles per LRCK Period.

Figure 22. CS53L32A Control Port Mode - Serial Audio Format 6



I²S, up to 24-Bit Data. Data Valid on Rising Edge of SCLK

Figure 23. CS53L32A Stand-Alone Mode - Serial Audio Format 0 (I^2S)



Left Justified, up to 24-Bit Data. Data Valid on Rising Edge of SCLK.

Figure 24. CS53L32A Stand-Alone Mode - Serial Audio Format 1

8. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

9. REFERENCES

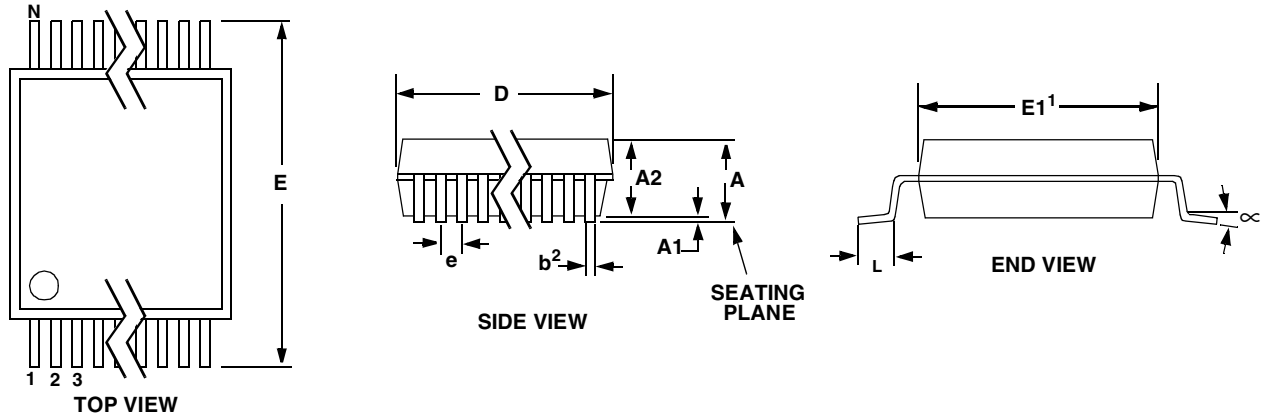
1. "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2. CDB53L32 Evaluation Board Datasheet.

3. “The I^2C-Bus Specification: Version 2.0” Phillips Semiconductors, December 1998. http://www.semiconductors.philips.com

10. PACKAGE DIMENSIONS

20L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.252	0.256	0.259	6.40	6.50	6.60	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	--	0.026	--	--	0.65	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

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Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.