CML Semiconductor Products

Application Information

AN/Data/469/2 November 1997

Using an FX469 FFSK Synchronous Modem with an Asynchronous Data I/O

Asynchronous Modem Circuitry

This application note, used with current FX469 product information, outlines the construction of a low-cost asynchronous modem for the transmission of RS-232 data in the form of Fast Frequency Shift Keying (FFSK, or Minimum Shift Keying (MSK), between terminals by a radio or line medium.

The modem circuitry shown in Figure 1 accepts asynchronous data while transmitting synchronous data using the FX469 series modem. The FX469 may be used to transmit data at either 1200 or 2400 bps, depending on the setting of Switch 1 shown in Figure 1. Details of the devices used in this application, are outlined below.

Function Requirement	**Device**
RS-232 Driver/Receiver Level Translator	Maxim MAX-232
Async to Sync conversion	MICRONAS MAS7838
Sync to Async Conversion	MICRONAS MAS7838
Data Carrier Detection	CML FX469
Controlled RTS/CTS Delay	74HC04 Delay Element
Generation of FFSK/MSK Signals	CML FX469
Reception of FFSK/MSK Signals	CML FX469
Interface into Radio System	CML FX469
RS-232 Handshake	Misc. Circuitry

The signals required for an RS-232 handshake for asynchronous data are as follows. A complete definition of each is given at the end of this application note.

DTR	Data Terminal Ready
DSR	Data Set Ready
RTS	Request to Send
CTS	Clear to Send
TXD	Transmit Data
RXD	Receive Data
DCD	Data Carrier Detect

The Maxim MAX-232 converts the TTL/CMOS input/output levels to the nominal ±10V RS-232 input/output levels. On power-up, the data set ready (DSR) signal is set by the MAX-232's DC to DC converter. The incoming data terminal ready (DTR) signal enables the transmitter keying signal.

The request to send (RTS) and clear to send (CTS) signals are level shifted from the RS-232 interface to TTL/CMOS signal levels. When the modem (DCE) receives an RTS, the RF transmitter and the MSK tone are keyed immediately and a 30 ms to 100 ms timer is started. At the completion of the timing, a CTS signal is generated for the data terminal (DTE) to allow serial data flow.

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The transmit data (TXD) signal is level shifted to the TTL/CMOS levels, and applied to the MICRONAS MAS7838 sync-to-async converter circuit. The random timed asynchronous input from the data terminal is synchronised with the transmit clock pulses of the FX469. If a timing error builds up due to the difference of the external asynchronous clock and the synchronous internal timing on the modem, the MICRONAS MAS7838 will skip a stop-pulse to allow an adjustment to occur. The receiving-end MICRONAS MAS7838 will generate a stop-pulse and add it into the data flow so that no information is lost.

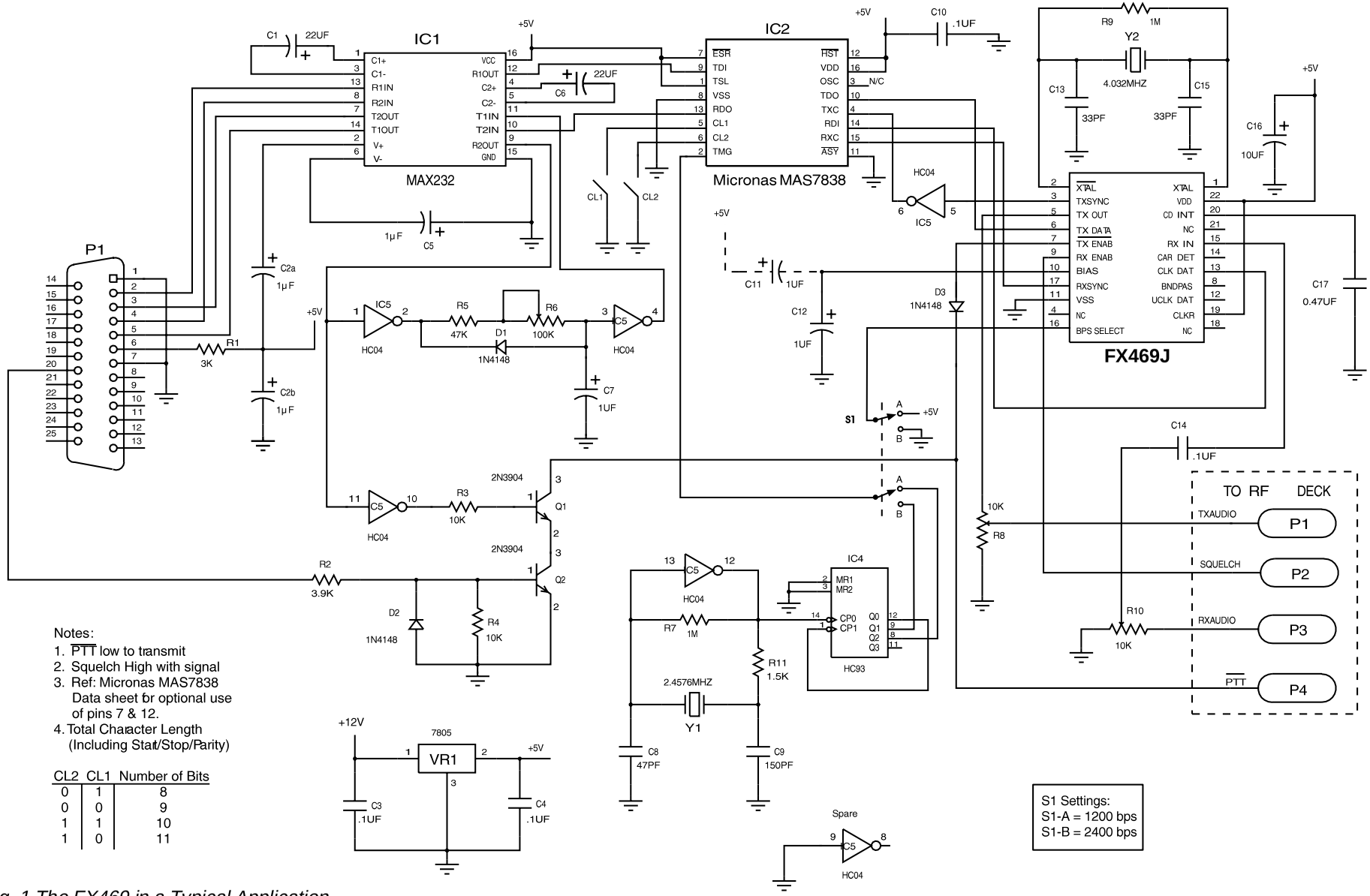
From the sync-to-async converter, synchronous information is then sent into the FX469, which converts the digital ‘1’ into one cycle of 1200 Hz sinewave and a digital ‘0’ into one and a half-cycles of 1800 Hz sinewave for 1200 bps and 1200 and 2400 Hz for 2400 bps. This sinewave is then sent on the transmitter through a level adjustment. The signal is sufficiently band limited and level controlled to pass FCC type acceptance testing without any additional in-band filtering.

The incoming receiver signal is fed into the FX469 which is held in a power down mode until an RF carrier is detected by the receiver squelch circuitry. This minimises power drain and also prohibits false information from being sent to the data terminal. If the receiver does not have a noise squelch signal, the chip’s carrier detect must be used. It will detect within 12 ms the presence of the data modulation tone. This event is output on the carrier detect pin which should be used to disable the data output to minimise random data at the terminal. The use of Schmitt trigger circuitry would minimise the ‘clatter’ at the beginning of the detection signal.

The FX469 FFSK tones are translated into logic levels and a digital phase lock loop is locked onto the incoming data steam within 16 bit reversals. The detected synchronous data and the recovered receive clock are sent into the MICRONAS MAS7838 for conversion back into asynchronous data. This information is then sent out to the data terminal through the Maxim, MAX-232.

Operation in either a synchronous or asynchronous mode is achieved by a logic level on pin 11 (XASY), of the MICRONAS MAS7838. If additional RS-232 level shifting is needed for transmit / receive clocks and the TX / RX enable (Note additional RS232 level shifting will require another MAX232), pin 11 (XASY) on the MICRONAS MAS7838 should be at logic ‘1’. Pulling this pin high bypasses the conversion process and allows synchronous data to pass directly through the device i.e. TDI = TDO and RDI = RDO.

The clock frequency for the FX469 device is provided by a 4.032MHz crystal. Clock frequency for the MICRONAS MAS7838 must be provided at 256 times the bit rate. This is accomplished by using a 2.4576MHz crystal and dividing down by eight to 301.2kHz (1200bps) or by four to 602.4kHz (2400bps). Power is derived from a single 7805 voltage regulator. Typical DC current measured on the first model is 12.75mA.



Notes:

1. $\overline{\text{PTT}}$ low to transmit
2. Squelch High with signal
3. Ref: Micronas MAS7838 Data sheet for optional use of pins 7 & 12.
4. Total Character Length (Including Start/Stop/Parity)

CL2	CL1	Number of Bits
0	1	8
0	0	9
1	1	10
1	0	11

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Fig. 1 The FX469 in a Typical Application

Software Considerations

As with many data systems, there are certain items that should be addressed within software for proper operation.

Bit Sync Pattern

The FX469 is a simple data pump that can be used with any protocol by adding the preamble to the start of the protocol. The ability of the FX469 to send and receive data, in a low signal to noise environment, lie in the ability of the receiving modem's phase lock loop to predictively determine the zero crossing of each successive data bit. A preamble must be sent prior to sending meaningful data (such as sync word or data) for the phase lock loop to acquire bit synchronisation. A minimum of 16 successive alternating ones and zeros must be transmitted as a preamble to train the receiving FX469's phase locked loop.

This preamble pattern may be accomplished by pre-pending two bytes of $55 or $AA onto the message. Make sure you take into account the stop, start, and parity bits to achieve a minimum of 16 one-to-zero transitions.

Stop, Start, and Length of Data

Once an RF signal ends, high level noise will be emitted from the receiver's discriminator. Even with data carrier detect or noise squelch circuits to gate the FX469's receiver off, there will be a period of noise (or false data out of the FX469) while muting circuits make a decision. This type of random data often creates problems down stream when applied to the logic controller or point of sale terminal. Having a message bracketed and only dealing with the information between start and stop characters is one method of prohibiting random data from entering the actual message. One should consider methods (or protocol) to distinguish start, stop, and length of data string to discern data burst from random noise.

Microprocessor Interface

Although this application note depicts using the FX469 without the need of a microprocessor, interface to a microprocessor may also be considered by the circuit designer. Additional flexibility can be added so the microprocessor adds or strips off any unnecessary start/stop and parity bits and adds the required preamble and bit timing to data sent to and from an asynchronous RS-232 port. The microprocessor interface is simple.

The FX469 internally generates an Rx and Rx SYNC clock for the microprocessor to use to synchronise each transmitted or received data bit. This allows the microprocessor to slave its timing to the zero crossings of the FFSK/MSK modulation method used to conserve bandwidth. Each successive data bit sent from the microprocessor to the TX data input pin must be present and stable while the TX SYNC clock is transitioning from a low to a high. The next bit to be transmitted is sent on the clock's falling edge. In a similar manner, data is read from the Rx CLOCKED DATA output pin on the falling edge of the Rx SYNC clock output pin. Data on the CLOCKED DATA output pin should be ignored on the rising edge of the Rx SYNC clock output.

The Carrier Detect output can be used as an additional logic-level to indicate that the presence of a carrier tone is or is not present at the Rx I/P during data reception.

Operation with CTCSS or DCS Sub-Carriers

Because the FX469 modems contain a bandpass filter on the Rx input and Tx output, CTCSS/DCS sub-carriers are filtered out without extra circuitry whilst the Tx filter bandlimits the data signal to reduce RF splatter during modulation..

It is important that no energy from the Tx sub-audio tone section appears within the transmitted data signal passband of 900 to 2100 Hz for 1200bps or 600 to 3000 Hz for 2400bps. It is equally important that the tone and data signals are not summed together and sent into the limiter section of the transmitter. The limiter represents a nonlinearity and would generate intermodulation products within the data pass-band which when received would generate errors in the decoding of the data.

The Tx sub-audio tone is normally summed into an FM transmitter after the limiting. Radios designed only for data do not require a speech limiter, allowing tone and data to be summed directly.

RS-232 Handshake

The RS-232 handshake for asynchronous data requires the following signals:

Data Terminal Ready (DTR) is a signal from the terminal or computer that indicates to the modem that the unit is powered and active.
An RF transmission **should not** be enabled if the Data Terminal is not active.

Data Set Ready (DSR) is a signal from the modem that indicates to the terminal that the unit is powered and active. Many terminals or computers will not allow data to flow without this condition being true.

Request to Send (RTS) emanates from the terminal or computer. The software or user has decided that transmission should begin and requests that the RF carrier be turned on.

Clear to Send (CTS) is a signal that originates from the modem. It is sent in response to a RTS, the request to send signal from the terminal or computer after certain criteria have been met. It is not sent until sufficient time has expired after the transmitter keyed to allow adequate settling time for both the RF transmitter and receiver.

Transmit Data and Receive Data (TXD0 (RXD) is the actual asynchronous data flow. Transmit data is data coming from the terminal and Receive data is data flowing into the terminal. Another term often heard is DTE and DCE ends of RS-232. This refers to what part of the handshake is expected and what the functions of the RS-232 connectors would be.
Most often a computer would be programmed to be a DTE or data terminal end of the information flow whilst the modem would be the DCE or data connection equipment end.

Data Carrier Detect (DCD) (Pin 8) is often connected to DSR (pin 6) in a modem, if it is required to function as a Carrier Detect pin. However in this application DSR is permanently wired high.

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