CML Semiconductor Products

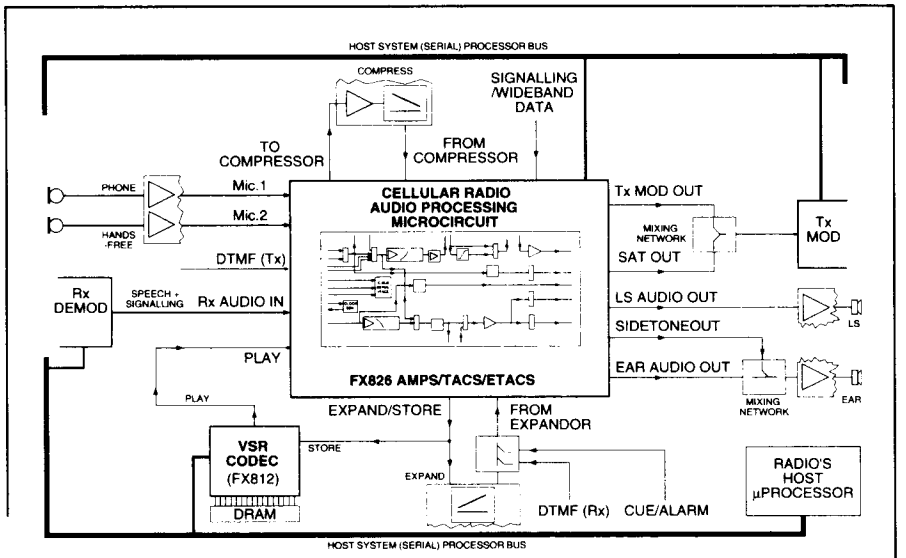
PRODUCT INFORMATION

FX826 AMPS/TACS System Audio Processor

Publication D/826/3 July 1994
Provisional Issue

Features

- **Full-Duplex Audio Processing for AMPS & TACS Cellular Systems**
- **On-Chip Speech and SAT Facilities**
  – Tx/Rx Filtering & Gain – SAT Channel Pre-/De-Emphasis – Deviation Limiter –
- **Serial µProcessor Interface**
  Separate SAT Channel
- **"Sidetone" Output Available**
- **HandsFree Compatibility**
- **Access to External Processes**
  – Compression – Expansion – Signalling – VSR Codec (Store/Play) –
- **Powersave (Low-Current) Settings**



FX826

Fig.1 The FX826 AMPS/TACS Audio Processor Installed within a Cellular System

Brief Description

The FX826 is a µProcessor controlled full-duplex audio processor on a single-chip with separate Tx and Rx paths to provide all the filter/gain/limiting functions necessary to pre-process audio, wideband-data and signalling in cellular communications systems using the AMPS or TACS/ETACS/JTACS specifications.

Selectable inputs available to the transmit path are: a choice of two microphones and DTMF/signalling, with access, in this path, to external compression circuitry. Operationally the Tx path provides input gain/filtering, a deviation limiter and Tx Modulation Drive controls.

In the Rx path the SAT signal is separated from the incoming audio via a filter block and made available at a separate pin for mixing externally with the Tx Modulation Drive.

The Rx path consists of an input gain/filter block for voice, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the FX816/826/836 cellular audio processors is the ability to route audio (Tx or Rx) to an external Voice Store and Retrieve (VSR) device such as the FX802 or FX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

The FX826, a low-power CMOS device, which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin plastic small outline (S.O.I.C.) surface mount and cerdip DIL packages.

Pin Number Function

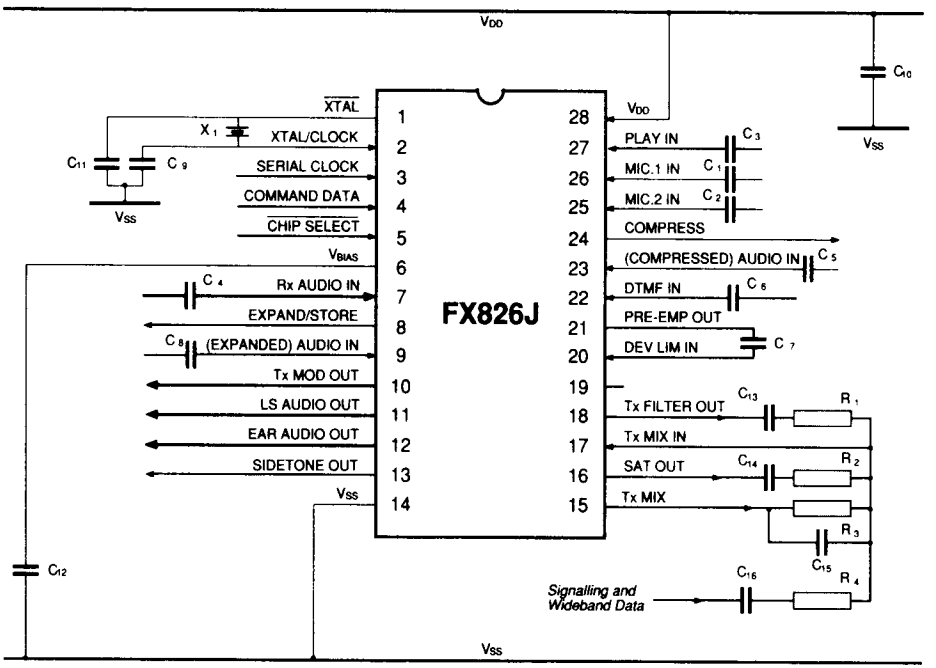
FX826DW	FX826J	Function
1	1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the FX826 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the FX826. See Timing Diagrams.
4	4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the FX826 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
6	6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	7	**Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	8	**Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the FX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 3.
10	10	**Tx Mod Out:** The composite Tx audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	11	**LS Audio Out:** An audio output of the Rx path (or selected audios, see Figure 3) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command (10_H)). A driver amplifier may be required.
12	12	**Ear Audio Out:** An audio output of the Rx path (or selected audios), available as an output for a handset earpiece. This output, in parallel with the LS Audio Out function, can be connected to V_{BIAS} when not required, by SW7 (Configuration Command (10_H)). A driver amplifier may be required.
13	13	**Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3.
14	14	**V_{SS}:** Negative supply rail. Signal ground.
		Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

Pin Number Function

FX826DW	FX826J	
15	15	**Tx Mix:** The output of the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment.
16	16	**SAT Out:** The output of the SAT Bandpass filter. This level is recovered from the input Rx audio and is available for mixing externally with the transmitter modulation. See Figure 3.
17	17	**Tx Mix In:** The input to the Tx Mix Amplifier. Used with external components, it allows the Tx Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. The recovered SAT signal may be introduced at this point. See Figures 2 and 3.
18	18	**Tx Filter Out:** The output of the Deviation Limiter/Lowpass Filter stage. This stage can be by-passed using SW3 (Configuration Command). See Figure 3.
19	19	No internal connection – Leave open circuit.
20	20	**Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve maximum possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	21	**Pre-Emphasis Out:** Audio output from the Tx Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 & 3.
22	22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the Tx Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	23	**Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	24	**Compression:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2.
25	25	**Mic.2 In:** Tx voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any Tx audio input. Pre-amplification may be required at these inputs. These inputs each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
26	26	**Mic.1 In:**
27	27	**Play In:** The input via SW2 from a voice storage device such as the FX812. This "replayed" audio can be sent to Rx or Tx paths allowing a Messaging/Voice Notepad/Answering facility. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	28	V_{DD}: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

"C-BUS" *is CML's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController. For further details refer to CML Publication No. DµINT/1 June 1991.*

Application Information



R_1 =	100kΩ	C_3 =	100nF	C_8 =	100nF	C_{13} =	100nF
R_2	as required	C_4	100nF	C_9	33pF	C_{14}	100nF
R_3	100kΩ	C_5	100nF	C_{10}	100nF	C_{15}	100pF
R_4	as required	C_6	100nF	C_{11}	33pF	C_{16}	100nF
C_1	100nF	C_7	100nF	C_{12}	1.0µF	X_1	4.000MHz
C_2	100nF						

Tolerances – Capacitors ±20%

Fig.2 Recommended External Components

Notes

1. **Xtal/clock operation**
Operation of any CML microcircuit without a Xtal or clock input may cause device damage. To minimise damage in the event of a Xtal/drive failure, it is recommended that the power rail (V_{DD}) is fitted with a current limiting device (resistor or fast-reaction fuse).

2. **SAT Output**
It is possible, due to the impedance of this output, that an external buffer amplifier is required when interfacing or mixing with other cellular system sections.

3. **Tx Mix Gain**
The value of R_4 should be chosen with R_3/C_{15} so as to provide the required gain.

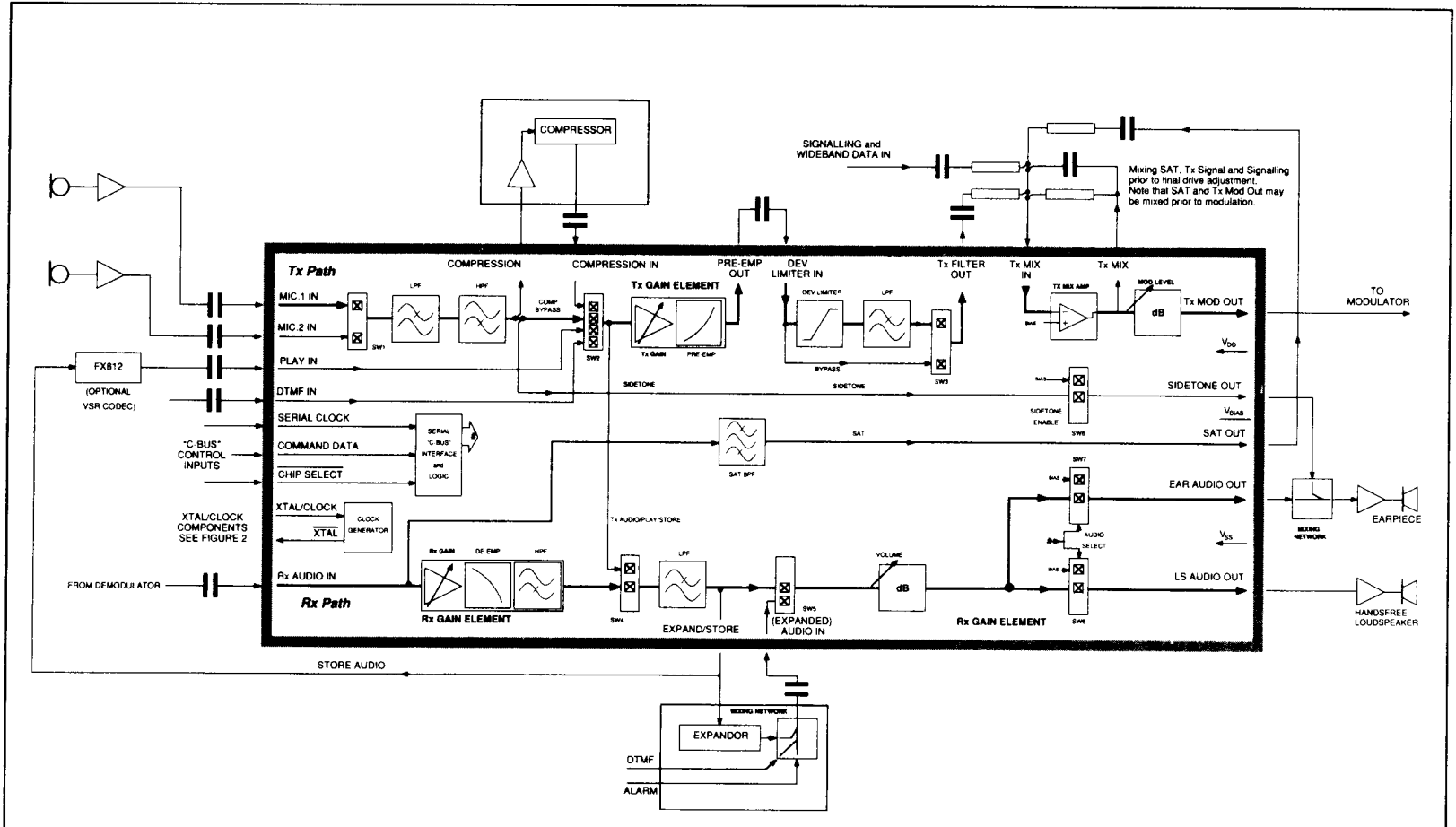


Fig.3 The FX826 Internal and External Signal Paths within a TACS Cellular Radio System

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX826 AMPS and TACS Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB ... LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Tx Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Rx Gain & Vol. Command	12	0 0 0 1 0 0 1 0	+	1 byte	4
Powersave Command	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, Tx/Rx Gains and Powersave assignments and data requirements are given in Table 1.
Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command (01_H)** will be required to set all FX826 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		Control Bits
MSB		***Transmitted First***
Bit 7		**Sw8 Sidetone**
0		Sidetone Bias
1		Sidetone Enabled
6		**Sw6/7 Rx Audio**
0		Ear Enabled, LS Bias
1		LS Enabled, Ear Bias
5		**Sw5 Expandor**
0		Expandor By-Pass
1		Expandor Route
4		**Sw4 Tx/Rx Audio**
0		Tx Store/Audio
1		Rx Store/Audio
3		**Sw3 Dev. Limiter**
0		Dev. Limiter By-Pass
1		Dev. Limiter Route
2		**Sw1 Mic. Inputs**
0		Mic. 1 Input
1		Mic.2 Input
1	***0***	**Sw2 Tx Function**
0	0	DTMF In
0	1	Compressor By-Pass
1	0	Compressor In
1	1	Play In

Table 2 Configuration Commands

Tx Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dBs)
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**Tx Input Gain**
0	0	0	0	2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 Tx Gain & Mod. Commands

The Controlling System .....

Rx Gain & Vol. Command *(Preceded by A/C 12_H)*

Setting				Gain (dBs)
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Rx Volume**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	***2***	***1***	***0***	**Rx Input Gain**
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.55
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 Rx Gain and Vol. Commands

Powersave Command *(Preceded by A/C 13_H)*

Setting							Control Bits
MSB							
Bit 7							***Transmitted First***
7	*6*	*5*	*4*	*3*	*2*	*1*	
0	0	0	0	0	0	0	All must be a logic "0"
			0				**Powersave Setting**
			0				Powersave FX826
			1				Enable FX826

Table 5 Powersave Command

Reference Signal Levels

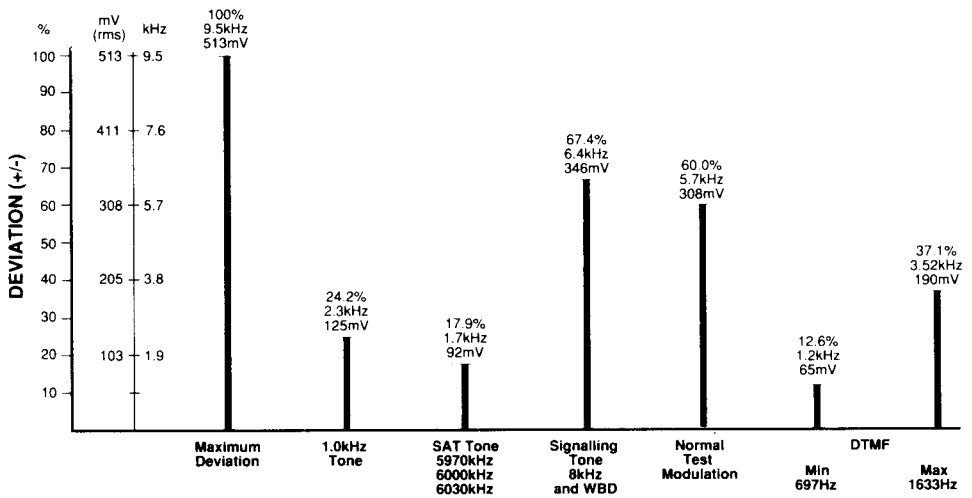


*Fig.4 TACS Signal Deviation Levels and corresponding **Tx Mod Outputs** with the Mod Level set to 0dB*

Control Timing Information

Timing Specification – Figures 5 and 6.

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the FX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

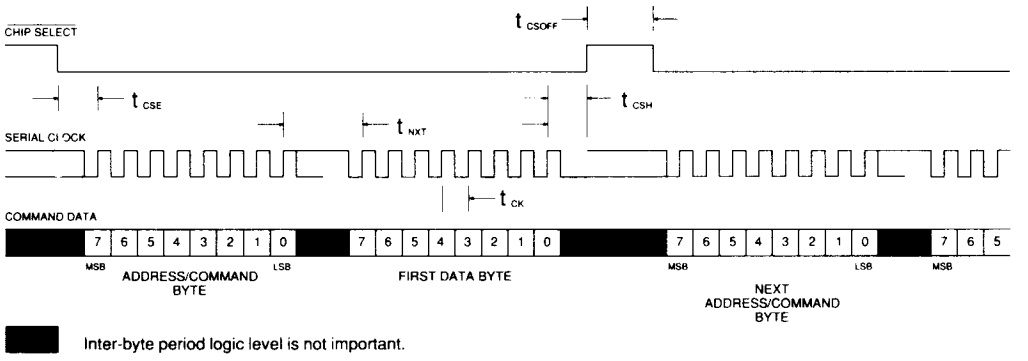


Fig.5 Control Timing Information

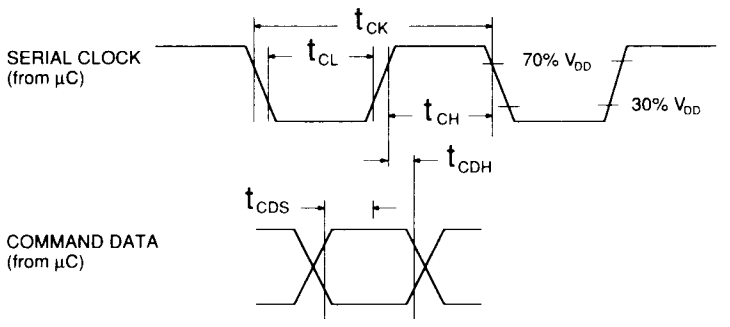
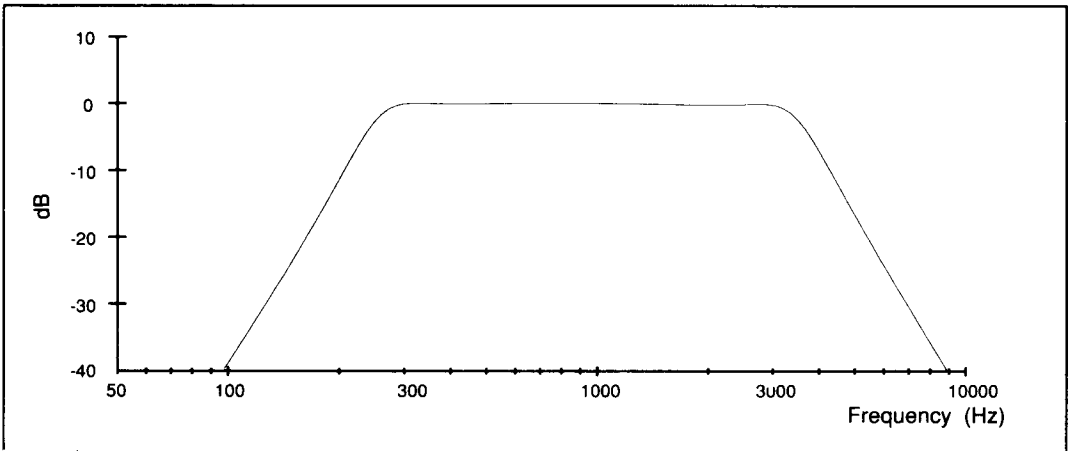


Fig.6 Control Timing Relationships

Frequency Responses



g.7 Microphone Input Stages -Combined Low and Highpass Filter Frequency Response

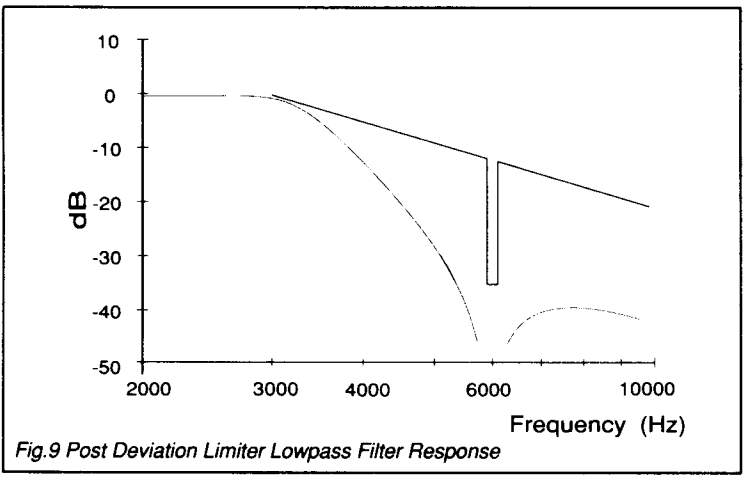


Fig.9 Post Deviation Limiter Lowpass Filter Response

Figure 7
Mic.1/2 In to Compression Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 8
Dev Limiter In to Tx Filter Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

ure 9

Rx Audio In to SAT out

V_{DD} = 5.0V

Signal Input Level = 100mVrms

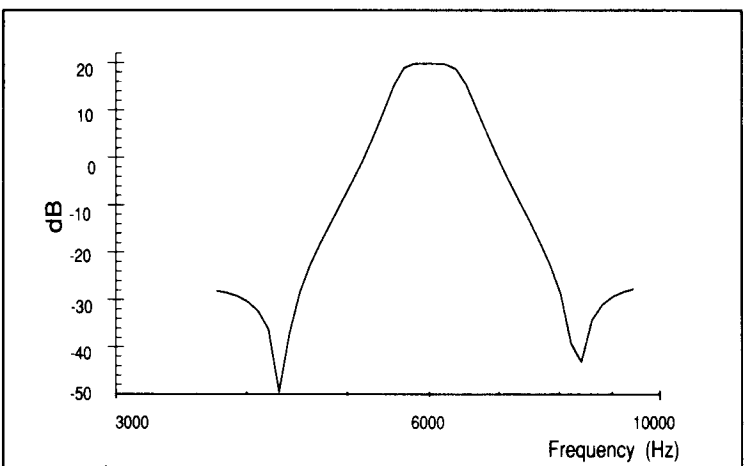


Fig.9 Rx SAT Path Bandpass Filter Response

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX826DW**	-40°C to +85°C (plastic)
	FX826J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX826DW**	-40°C to +85°C (plastic)
	FX826J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.000MHz. Audio level 0dB ref. = 308mV rms @ 1.0kHz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Operating		–	6.5	–	mA
Powersave		–	0.5	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
Tx Mix Amp (Open Loop Gain)		–	50.0	–	dB
(Bandwidth)		20.0	–	–	kHz
Analogue Input Impedances					
Mic.1 & 2		–	500	–	kΩ
Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
Tx Mix In		10.0	–	–	MΩ
Rx Audio In		–	100	–	kΩ
Analogue Output Impedances					
Pre-Emp Out		–	600	–	Ω
Tx Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
SAT Out	3	–	1.0	–	kΩ
Tx Filter Out		–	600	–	Ω
Comp Out		–	600	–	Ω
Sidetone Out		–	2.0	–	kΩ
Tx Mix (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ
Control Interface Parameters					
Input Logic Levels					
Logic "1"	1	3.5	–	–	V
Logic "0"	1	–	–	1.5	V
I_{IN} (logic "1" or "0")	1	-1.0	–	1.0	µA
Input Capacitance	1	–	–	7.5	pF
Channel Performances					
Tx Path					
Filter Specifications					
Pre-Compression L/HPF Combination					
Passband		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-24.0	–	–	dB/oct.
Tx Gain Pre-Emphasis					
Gain at 1.0kHz		–	0	–	dB
Slope (300Hz - 3000Hz)		–	6.0	–	dB/oct.

Specification .....

Characteristics		See Note	Min.	Typ.	Max.	Unit
Post Deviation Limiter LPF						
Attenuation Relative to 1.0kHz	3.0kHz - 5.9kHz			40 log(f/3000)		dB
	5.9kHz - 6.1kHz			35.0		dB
	6.1kHz - 15kHz			40 log(f/3000)		dB
	>15kHz			28.0		dB
Analogue Signal Input Levels						
Mic. 1 and 2		2	–	0	–	dB
Play		2	–	0	–	dB
DTMF		2	–	0	–	dB
Comp. In		2	–	0	–	dB
Tx Mix In		2	–	0	–	dB
Analogue Signal Output Levels						
Pre-Emp Out		2	–	0	–	dB
Tx Filter Out		2	–	0	–	dB
Tx Mod Out		2	–	0	–	dB
Sidetone Out		2	–	0	–	dB
Path Gains/Levels						
Tx Gain – 11_H						
Nominal Adjustment Range			-2.65	–	3.65	dB
Error of any Setting			-0.2	–	0.2	dB
Dev Limiter						
Threshold			–	1086	–	mVp-p
Symmetry			–	7.0	–	%
Mod Level Attenuation – 11_H						
Nominal Adjustment Range			-5.6		0	dB
Step Size			0.2	0.4	0.6	dB
Error of any Setting			-1.0	–	1.0	dB
Overall						
Tx Distortion			–	-40.0	-32.0	dBp
Tx Hum and Noise			–	-40.0	-20.0	dB
Rx Signal Path						
Filter Specifications						
Rx Gain De-Emphasis						
Gain at 1.0kHz			–	3.75	–	dB
Slope (300Hz - 3000Hz)			–	-6.0	–	dB/oct.
Rx Channel Bandpass			300		3000	Hz
Slope - below 300Hz			+24.0	–	–	dB/oct.
above 3000Hz			-36.0	–	–	dB/oct.
Analogue Signal Levels						
Rx Audio Input Level		2	–	-7.0	–	dB
LS/Ear Audio Output Level		2	–	0	–	dB
Path Gains/Levels						
Rx Gain – 12_H						
Nominal Adjustment Range			3.75		9.70	dB
Error of any Setting			-0.2	–	0.2	dB
Volume – 12_H						
Nominal Adjustment Range			-28.0		0	dB
Step Size			1.5	2.0	2.5	dB
Error of any Setting			-1.0	–	1.0	dB
Overall						
Rx Distortion			–	-40.0	-32.0	dBp
Rx Hum and Noise			–	-40.0	-34.0	dB
SAT Signal Path						
Bandpass Filter						
Frequency Range			5970		6030	Hz
Gain			19.0	20.0	21.0	dB

Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Levels equivalent to ±3.0kHz deviation with the settings below:

   Tx Gain = 0dB *Mod Level = 0dB*

   Rx Gain = 7.05dB *Volume = 0dB*

   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
3. Recommended load >10.0kΩ.

Package Outlines

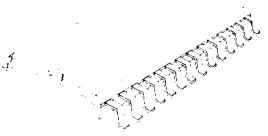
The FX826 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX826 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX826DW 28-pin plastic S.O.I.C. (D1)

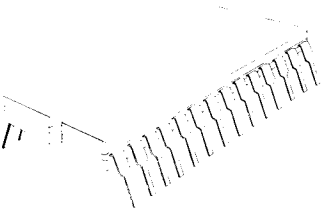
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX826J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX826DW	28-pin plastic S.O.I.C.	(D1)
FX826J	28-pin cerdip DIL	(J5)