FX809
FFSK Modem

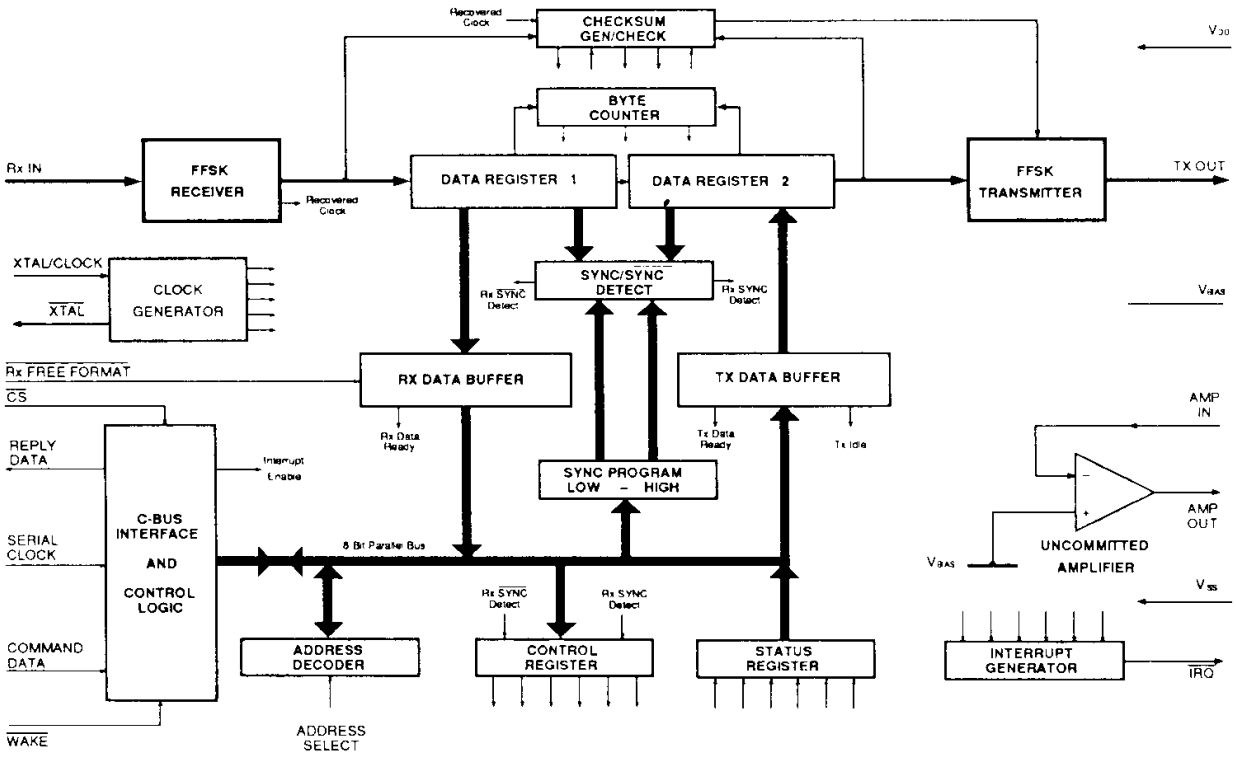

Fig 1. FX809 FFSK Modem

Brief Description

An intelligent, half-duplex, FFSK/MSK modem which operates under "C-BUS" control. In addition this modem provides software selectable checksum generation and error checking, in accordance with MPT1327.
The FX809, using Interrupt and Status Register procedures, performs the functions described below:

In Tx mode the FX809 will:

1. (a) Accept from the host and transmit, 8-bit bytes of data as instructed (Preamble, Sync, Address and data).
   (b) internally calculate and insert a 2 byte checksum based upon the preceeding 6 bytes of data, or
   (c) disable the internal checksum generator and continuously transmit the data supplied.
2. Transmit 1 hang-bit and go to Tx Idle when all loaded data bytes have been transmitted.

In Rx mode the FX809 will:

1. Detect and achieve bit synchronization within 16 bits.
2. (a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and achieve frame sychronization. Data will then be output in 8-bit bytes via the Rx Data Buffer.
   (b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.
3. Make the incoming data directly available, via the Rx Data Buffer (Rx Freeformat), overriding synchronization requirements.

The FX809 achieves Rx input timing by recovering an Rx clock from the incoming data stream. Output tones are timed to the internally generated transmit clock. Filter, register clocks and transmit FFSK tone frequencies are derived internally from the external Xtal or clock pulse input.
For compliance with the MPT 1327 Signalling Specification a 4.032MHz Xtal or clock input will be required.

NOTE: All information contained in this data sheet is specified using a 4.032 MHz Xtal, 1200 bps baud rate, Mark and Space frequencies 1200 Hz and 1800 Hz.

The FX809 is a low-power 5-volt integrated circuit, incorporating "Powersave" modes to further reduce power requirements.

An uncommitted amplifier is provided on chip for general purpose applications within DBS 800.
The FX809 is available in 24-pin cerdip DIL and 24-pin/lead plastic SMD packages.

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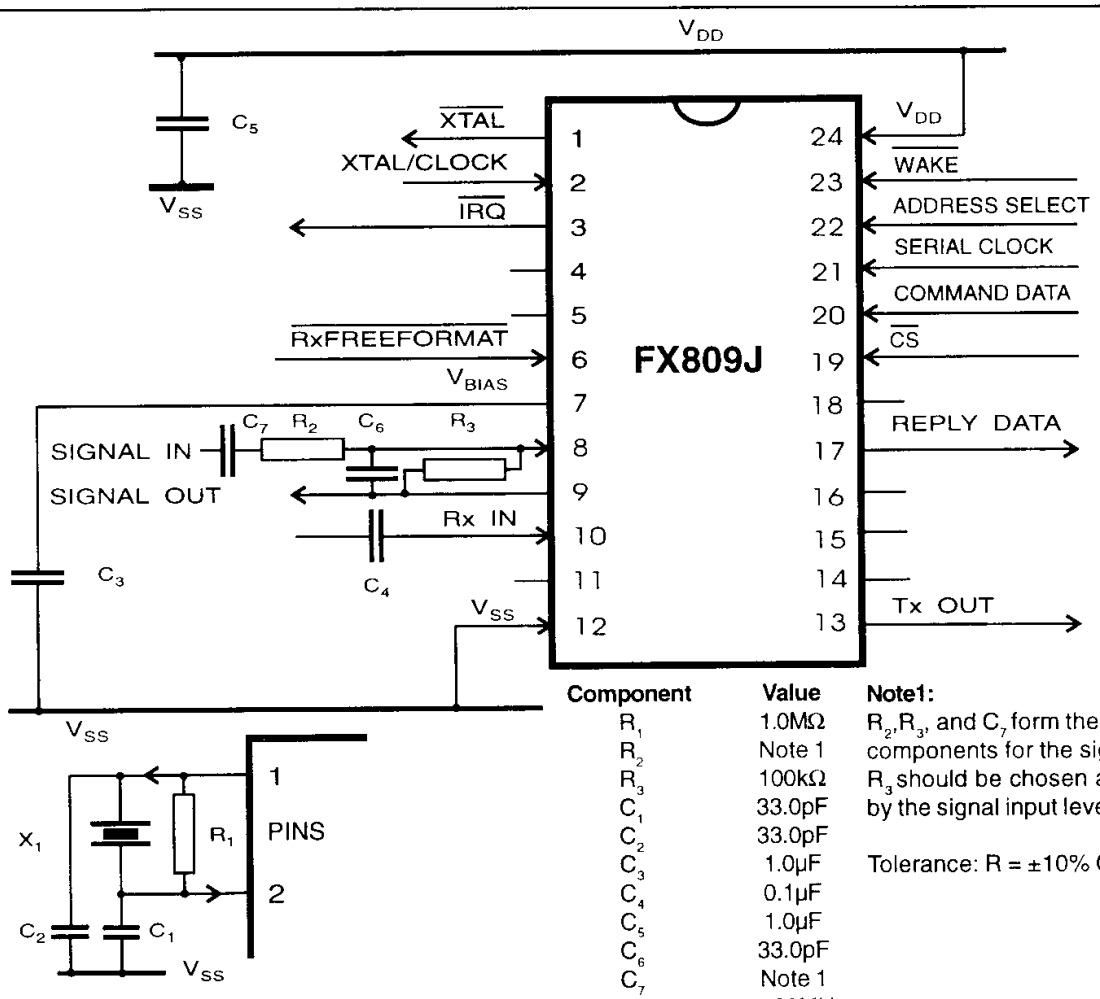
Pin Number FX809 J/LG/LS	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2, INSET.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET.
3	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low-impedance pulldown to logic "0" when active and a high-impedance when inactive. The conditions that cause interrupts are indicated in the Status Register and are shown below: Tx Idle — Rx Data Ready — Tx Data Ready Rx SYNC Detect — Rx $\overline{\text{SYNC}}$ Detect Interrupt outputs can be disabled by bit 3 of the Control Register.
4	No Internal connection.
5	No Internal connection.
6	**$\overline{\text{Rx Freeformat}}$:** Used in the Rx mode, this input, when a logic "0," allows received data to be read from the Rx Data Buffer via the Reply Data line without having to acheive byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime bit is set or the modem set to Tx mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pullup resistor. NOTE: If this input is held at a logic "0" in the Tx mode, the Rx Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the Rx mode, an Rx Data Ready interrupt may be generated immediately, in this case the first byte of Rx data should be ignored.
7	V_{BIAS} : The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_3, see Figure 2.
8	**Amp In:** The inverting input to the on-chip uncommitted amplifier .
9	**Amp Out:** The output of the on-chip uncommitted amplifier.
10	**Rx In:** The 1200 baud, 1200Hz/1800Hz, received FFSK signal input. The input signal to this pin must be a.c. coupled via capacitor C_4, see Figure 2.
11	No Internal connection.
12	V_{SS}: Negative Supply (GND).

Pin Number FX809 J/LG/LS	Function
13	**Tx Out:** The 1200 baud, 1200Hz/1800Hz FFSK Tx output. When not transmitting data the output impedance of this pin is high. On power-up, this output can be any level, a General Reset command is required to ensure that this output attains V_{BIAS} initially.
14	No Internal connection.
15	No Internal connection.
16	No Internal connection.
17	**Reply Data:** The "C-BUS", serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams and System Support Document, Document 2.
18	No Internal connection.
19	**Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function, this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams and System Support Document, Document 2.
20	**Command Data:** The "C-BUS," serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams and System Support Document, Document 2.
21	**Serial Clock:** The "C-BUS," serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the FFSK Modem. See Timing Diagrams and System Support Document, Document 2.
22	**Address Select:** This pin enables two FX809 devices to be used on the same "C-BUS," providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Tables 1 and 2.
23	**$\overline{Wake}$:** This input can be used to reactivate the FX809 from the 'Powersave' condition. The device will be in a 'Powersave' condition when both this pin and bit 2 of the Control Register are set to a logic "1." Recovery from Powersave is achieved by putting either the $\overline{Wake}$ pin or the Powersave bit in the Control Register to a logic "0." This allows FX809 activation by the µController or an external signal, such as R.S.S.I. or Carrier Detect.
24	V_{DD}: Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the FFSK Modem are dependant upon this supply.

Powersave (CR bit 2)	$\overline{Wake}$	FX809 Condition
1	1	Powersave
0	1	Enabled
1	0	Enabled
0	0	Enabled

NOTE: Pins 4, 5, 11, 14, 15, 16 and 18 may be connected to V_{SS} to improve screening.

External Components



Component	Value
R_1	1.0MΩ
R_2	Note 1
R_3	100kΩ
C_1	33.0pF
C_2	33.0pF
C_3	1.0µF
C_4	0.1µF
C_5	1.0µF
C_6	33.0pF
C_7	Note 1
X_1	4.032MHz

Note1:
R_2, R_3, and C_7 form the gain components for the signal; R_3 should be chosen as required by the signal input level.

Tolerance: R = ±10% C = ± 20%

Fig.2 External Components

Modem Performance

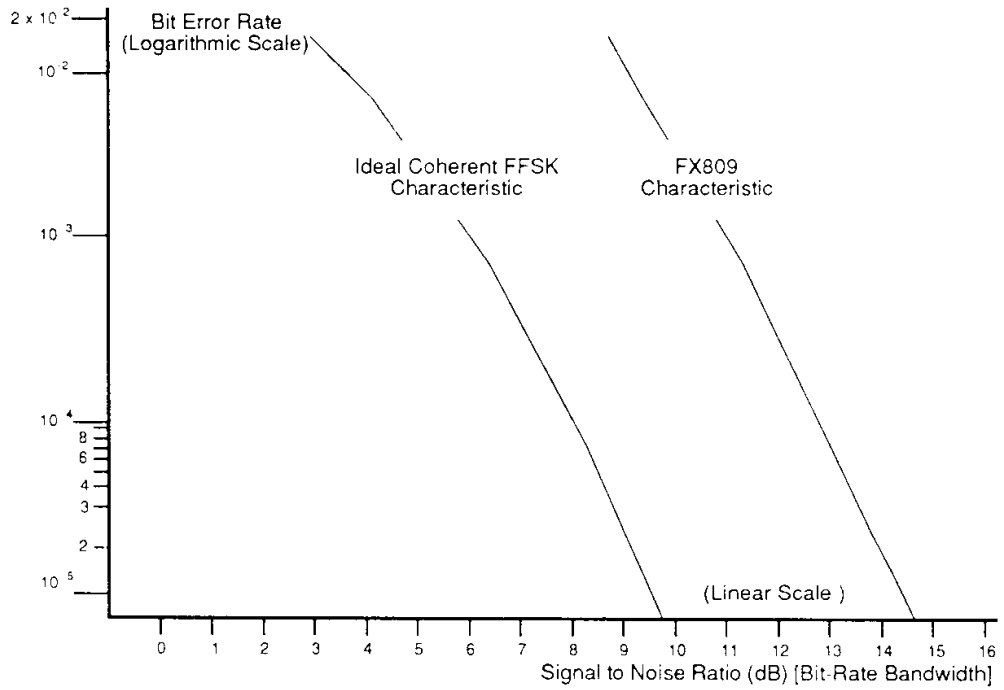


Fig.3 Bit Error Rate vs Signal-to-Noise Ratio

Controlling Protocol

Control of the functions within the FX809 FFSK Modem is by a group of Address/Commands (A/Cs) and appended data to and from the system μController via "C-BUS." Provision is made to address 2 separate FFSK Modems. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB							LSB		Notes
General Reset	01	0	0	0	0	0	0	0	1		Control Register bits set to logic "0"
Write to Control Register	40	0	1	0	0	0	0	0	0	+	1 byte instruction to Control Reg.
Read Status Register	41	0	1	0	0	0	0	0	1	+	1 byte reply from Status Reg.
Read Rx Data Buffer	42	0	1	0	0	0	0	1	0	+	1 byte of data from Rx Data Buffer
Write to Tx Data Buffer	43	0	1	0	0	0	0	1	1	+	1 byte of data to Tx Data Buffer
Write to SYNC Program	44	0	1	0	0	0	1	0	0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 1 Modem No.1 "C-Bus" Address/Commands – (Address Select input at a logic "0")

Address/Commands

Instruction and data transactions to and from the FX809 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data, or
(ii) a Status or Rx data Reply.

Control and configuration is by writing instructions from the μController to the Control Register [40_H, (48_H)].

Reporting of FX809 configurations is by reading the Status Register [(41_H, (49_H)]. Instructions and data are transferred, via "C-BUS," in accordance with the timing information given in Figure 4.

Data for transmission as FFSK is sent to the Tx Data Buffer via the Command Data line. Received data is read from the Rx Data Buffer via the Reply Data line.

Instruction and data transactions to and from this device are preceded by the relevant Address/ Command (A/C).

"C-BUS" allocations for the FX809 are shown in Tables 1 and 2.

A complete list of DBS 800 "C-BUS" Address/ Command allocations is published in the System Support Document, Document 2.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB							LSB		Notes
General Reset	01	0	0	0	0	0	0	0	1		Control Register bits set to logic "0"
Write to Control Register	48	0	1	0	0	1	0	0	0	+	1 byte instruction to Control Reg.
Read Status Register	49	0	1	0	0	1	0	0	1	+	1 byte reply from Status Reg.
Read Rx Data Buffer	4A	0	1	0	0	1	0	1	0	+	1 byte of data from Rx Data Buffer
Write to Tx Data Buffer	4B	0	1	0	0	1	0	1	1	+	1 byte of data to Tx Data Buffer
Write to SYNC Program	4C	0	1	0	0	1	1	0	0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 2 Modem No.2 "C-Bus" Address/Commands – (Address Select input at a logic "1")

Address Select

This input allows, using the correct addressing, 2 FFSK Modems on the same BUS.

When operating in a system employing 2 FFSK Modems, 1 FFSK Modem is designated No.1 and requires its Address Select input to be held at a logic "0", and the second FFSK Modem (No. 2) requires its Address Select input to be held at logic "1."

All "C-BUS" transactions with Modem 1 will use Address/Command allocations 40_H to 44_H (Table 1) and transactions with Modem 2 will use 48_H to $4C_H$ (Table 2).

For explanation purposes further descriptions in this publication of FX809 FFSK Modem internal register functions will deal primarily with FFSK Modem No. 1 (Address Select at logic "0").

Controlling Protocol...

"Write to Control Register" This 'Write Only' register directs the modem's operation.

Setting	*Control Bits*
MSB Bit 7	***Transmitted First*** Not used Set to "0"
6	Not used Set to "0"
5	**SYNC Prime**
0	
1	Primed
4	**SYNC Prime**
0	
1	Primed
3	**Interrupt Enable**
0	Disable
1	Enable
2	**Powersave**
0	Normal Operation
1	Powersave
1	**Checksum Enable**
0	Disable
1	Enable
0	**Rx/Tx Mode**
0	Rx
1	Tx

Table 3 Control Register

SYNC Prime When set, this bit enables SYNC Word detection.
Cleared on a successful SYNC Word detection.

SYNC Prime When set, this bit enables SYNC Word detection.
Cleared on a successful SYNC Word detection.

Interrupt Enable When set, this bit allows interrupts to be output by the FX809 on the IRQ line.

Powersave Used in conjunction with the Wake input (see Pin Functions) to control the Powersave state of the FX809.

Checksum Enable When set:
In Tx: a 2-byte checksum is generated and transmitted after every 6 bytes transmitted.
In Rx: After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the Rx Checksum True bit in the Status Register is set to a logic "1."
When this bit is a logic "0" no checksums are generated or checked.
NOTE: Checksum operation is inhibited during the SYNC/SYNC search period.

"Read Rx Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
Rx Data Buffer							

Rx Data Buffer

This "Read Only' register contains the last byte of data received from the Data Register. Received Bit 7 (MSB) first.

"Write to Tx Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
Tx Data Buffer							

Tx Data Buffer

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) will be transmitted first.

"Write to Sync Program"

MSB Byte 1											Byte 0				LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC High								**SYNC Low**							

SYNC Program

This "Write Only" register is loaded with the required Sync Word. This word (or its opposite logic sense, SYNC) is compared with the received synchronization word. If the required SYNC Word is less than 16 bits, the remaining bits must be programmed as preamble (10101010..etc.) bit 15 (MSB) is loaded first.

Controlling Protocol...

"Read Status Register" This 'Read Only' register will indicate the source of FX809 interrupts ($\overline{IRQ}$'s).

Reading	*Status Bits*
MSB	*Received First*
Bit 7	Undefined
0	"0" or,
1	"1"
6	Undefined
0	"0" or,
1	"1"
5	**Rx $\overline{SYNC}$ Detect**
0	
1	SYNC
4	**Rx SYNC Detect**
0	
1	SYNC
3	**Tx Idle**
0	
1	Idle
2	**Tx Data Ready**
0	
1	Tx Data Ready
1	**Rx ChecksumTrue**
0	
1	True
0	**Rx Data Ready**
0	
1	Rx Data Ready

Table 4 Status Register

Rx $\overline{SYNC}$ Detect
Set and an Interrupt generated when the correct $\overline{SYNC}$ Word is detected (if $\overline{SYNC}$ Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Rx SYNC Detect
Set and an Interrupt generated when the correct SYNC Word is detected (if SYNC Prime is set).

Cleared by (i) reading the Status Register,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Tx Idle
Set and an Interrupt generated when all loaded Tx data and 1 'hang-bit' have been transmitted.

Cleared by (i) writing to the Tx Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "0."

Tx Data Ready
Set and an Interrupt generated indicating that a byte of data should be written to the Tx Data Buffer.

Cleared by (i) reading the Status Register and writing a byte of data to the TX Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "0."

Rx Checksum True
Set and an Interrupt generated by successful comparison of the received and self generated checksums.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) $\overline{Rx}$/Tx being taken to logic "1."

Rx Data Ready
Set and an Interrupt generated, indicating that the Rx Data Buffer is full, a byte of data is to be read from the Rx Data Buffer, this must be read within 8 bit periods.

Cleared by (i) reading the Status Register and the Rx Data Buffer,
(ii) Setting $\overline{Rx}$/Tx to logic "1."

Interrupt Requests ($\overline{IRQ}$)

The conditions that cause interrupts to be output (if enabled by the Control Register) from the FX809 are:

Tx Idle
Tx Data Ready
Rx $\overline{SYNC}$ Detect
Rx Data Ready
Rx SYNC Detect

To ascertain the cause of the interrupt the Status Register should be read.

Interrupts are cleared:

(i) by a read of the Status Register, or

(ii) by changing the state of the $\overline{Rx}$/Tx bit.

General Reset

Upon Power-Up, the bits in the FX809 Modem registers and buffers will be random (either "0" or "1"). The General Reset command (01_H) will "reset" all microcircuits on the "C-BUS" and has the following effect on the FX809:

All bits in the Control Register will be set to logic "0." The Tx Out output will be set to V_{BIAS}.

NOTE: That the Status Register, Rx Data Buffer, Tx Data Buffer and Sync Program register are not affected by the General Reset command.

"C-BUS" Timing Information

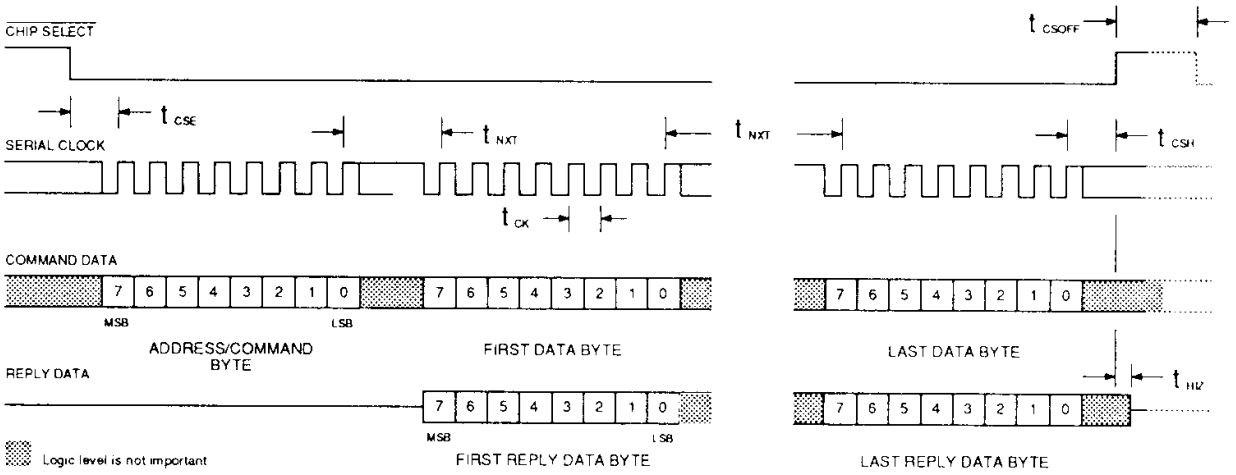


Fig.4 "C-BUS" Timing

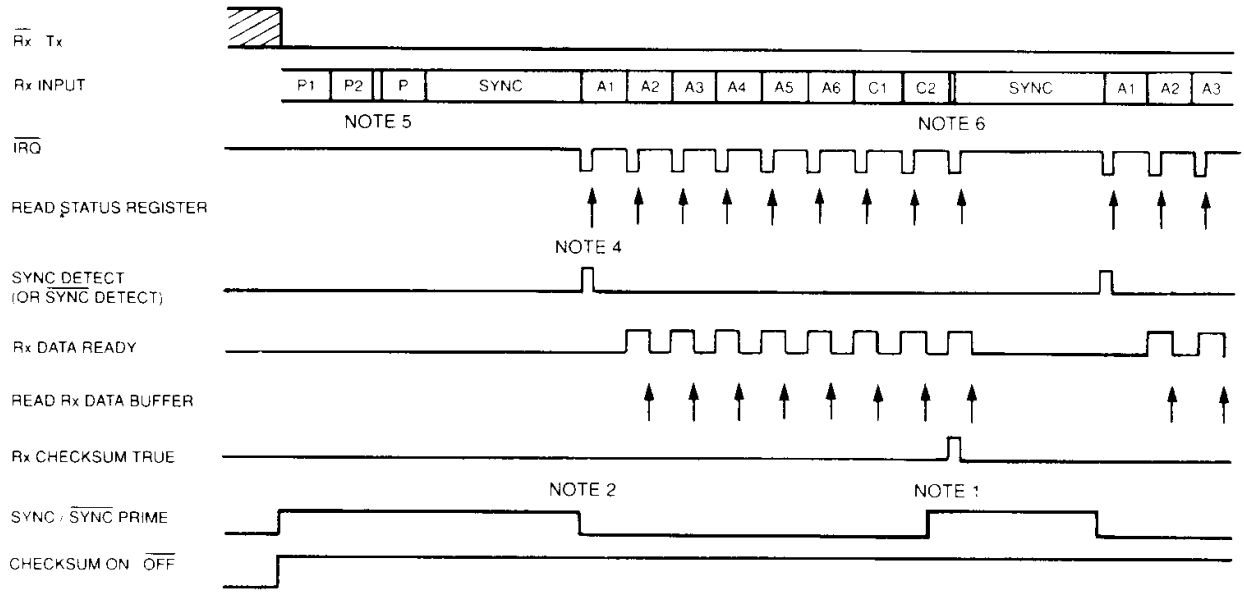
"C-BUS" Timing – Figure 4

Parameter	Min.	Max.	Unit
t_{CSE}	2.0	–	µs
t_{CSH}	4.0	–	µs
t_{HIZ}	–	2.0	µs
t_{CSOFF}	2.0	–	µs
t_{NXT}	4.0	–	µs
t_{CK}	2.0	–	µs

Notes

(1) Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last. Reply Data is read from the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into and out of the peripheral on the rising Serial Clock edge.
(3) Loaded commands are acted upon at the end of each command.
(4) To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity Serial Clock pulses.

Modem Timing Information

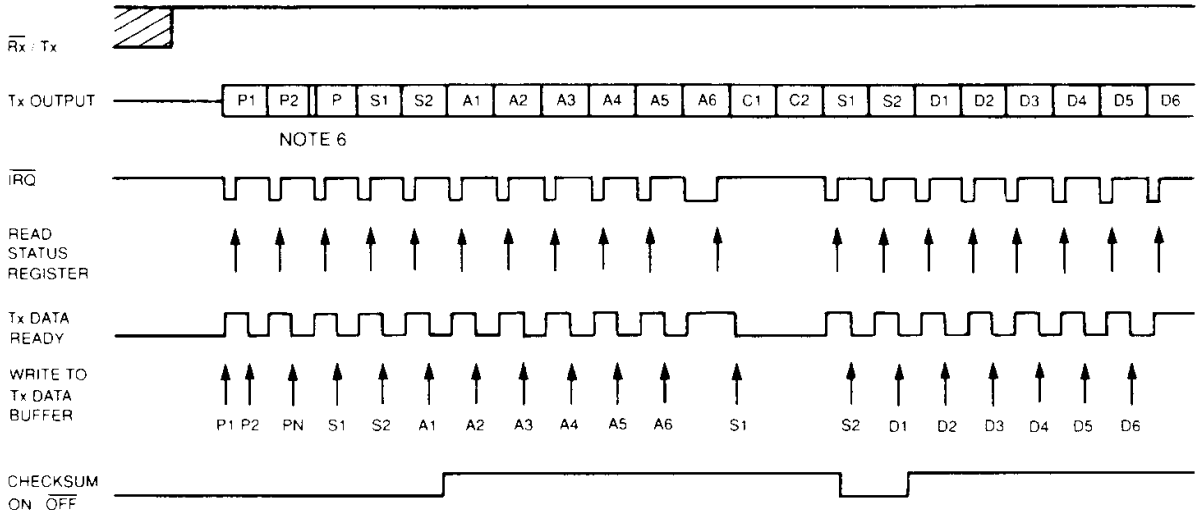


NOTES
1). The SYNC and SYNC detector searches the incoming bit stream starting at the end of the byte in which SYNC/SYNC prime was set.
2). After detection of a SYNC/SYNC word the SYNC/SYNC prime bits automatically go low (control bits 5 and 6: detector off).
3). The checksum checker is inhibited during the time SYNC/SYNC search is operating.
4). The status register will indicate whether SYNC or SYNC was detected here.
5). Any number of preamble bits can occur here
6). Any number of bits can occur here
7). Rx Freeformat set high.

Fig.5 Rx 1

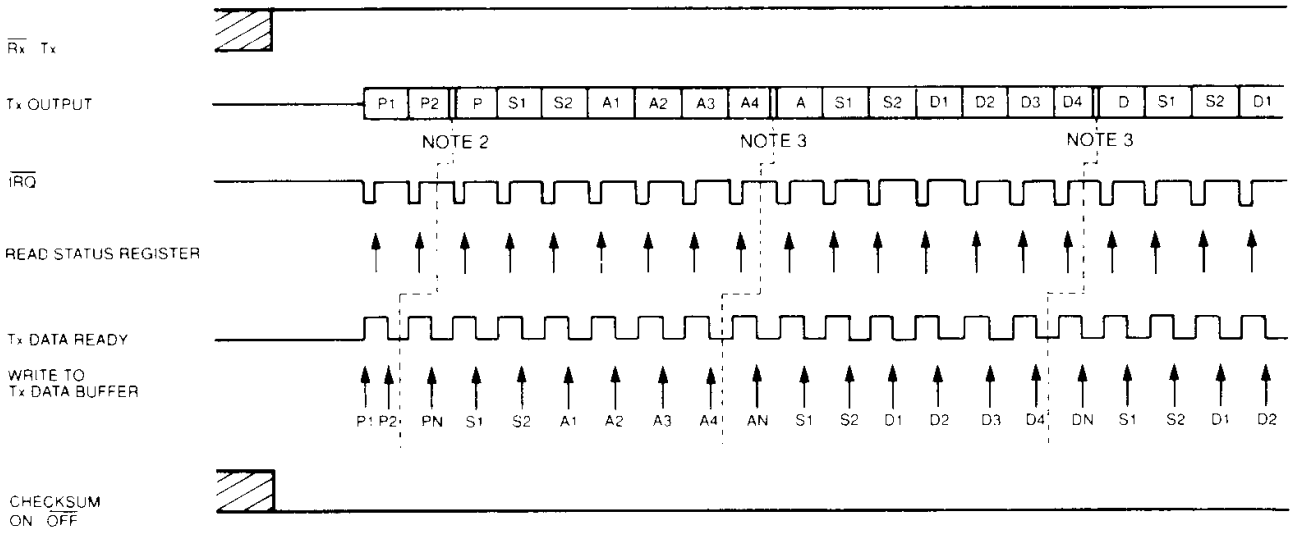
Tx Timing Information

(a) Tx MORE THAN ONE MESSAGE, SYNC BEFORE EVERY MESSAGE, Tx CHECKSUM ENABLED.



NOTES
1). Preamble and SYNC bytes are loaded as data from the µC.
2). The Tx output will be held at bias level when no data is being transmitted.
3). Tx byte synchronisation is established by the loading of the first preamble byte from the µC.
4). Checksum must be turned off during preamble and SYNC words.
5). When Rx/Tx is low Tx output is at bias.
6). Any number of preamble bytes can occur here.

(b) Tx MORE THAN ONE MESSAGE, Tx CHECKSUM NOT ENABLED.

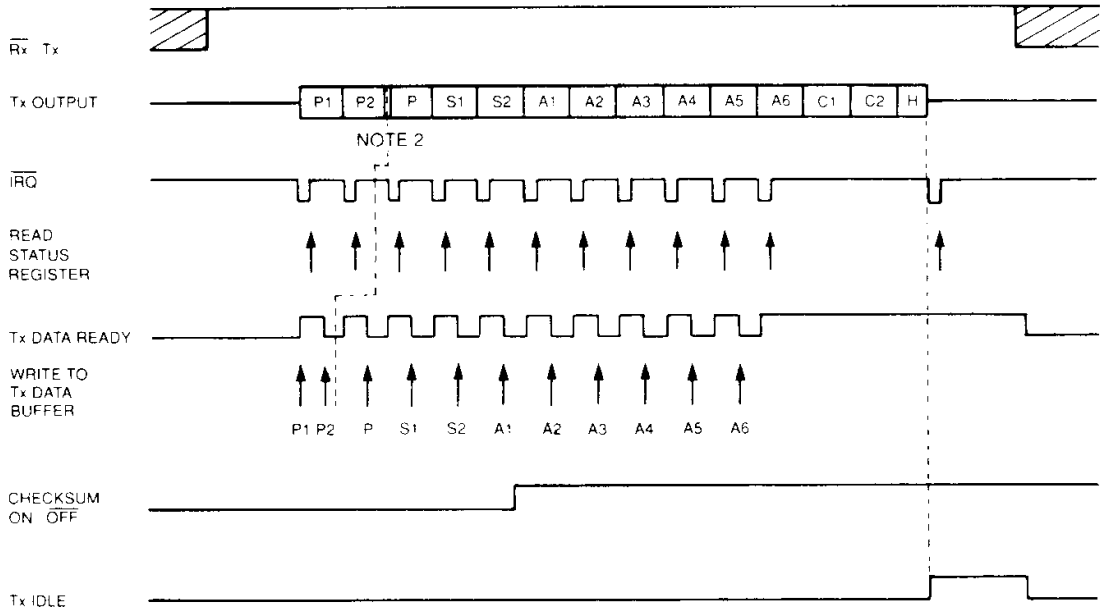


NOTES
1). Preamble, SYNC words and checksums are supplied by the µC in this format as data bytes.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here

Fig.6 Tx Timing

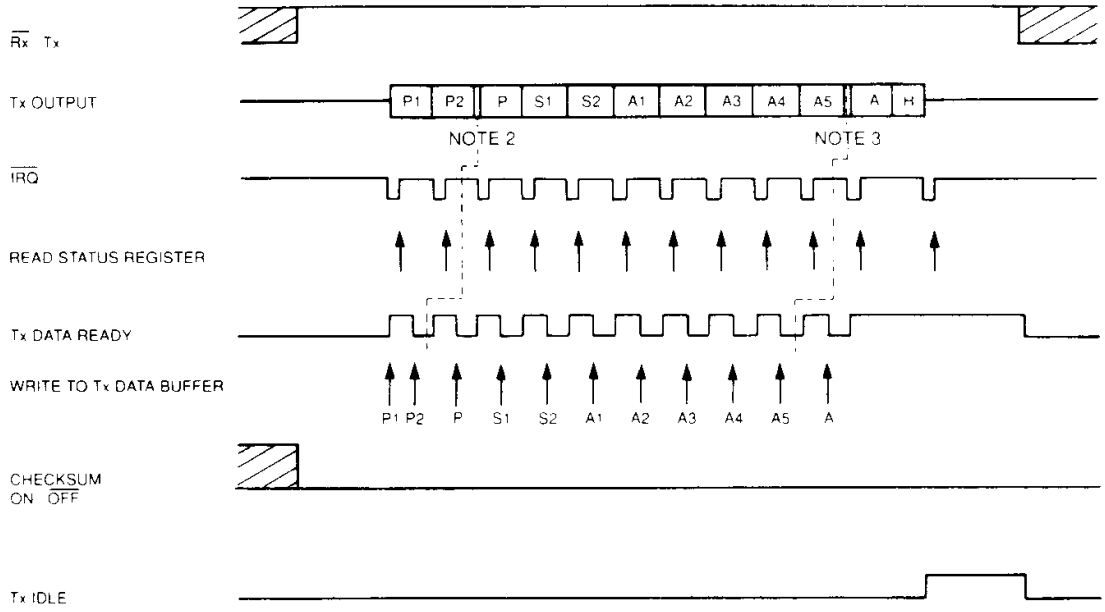
Tx Timing Information...

(a) Tx ONE MESSAGE, Tx CHECKSUM ENABLED.



NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Transmission terminates after C1, C2 and H. Termination occurs when no further data bytes are written to the Tx data buffer.

(b) Tx ONE MESSAGE, Tx CHECKSUM NOT ENABLED.



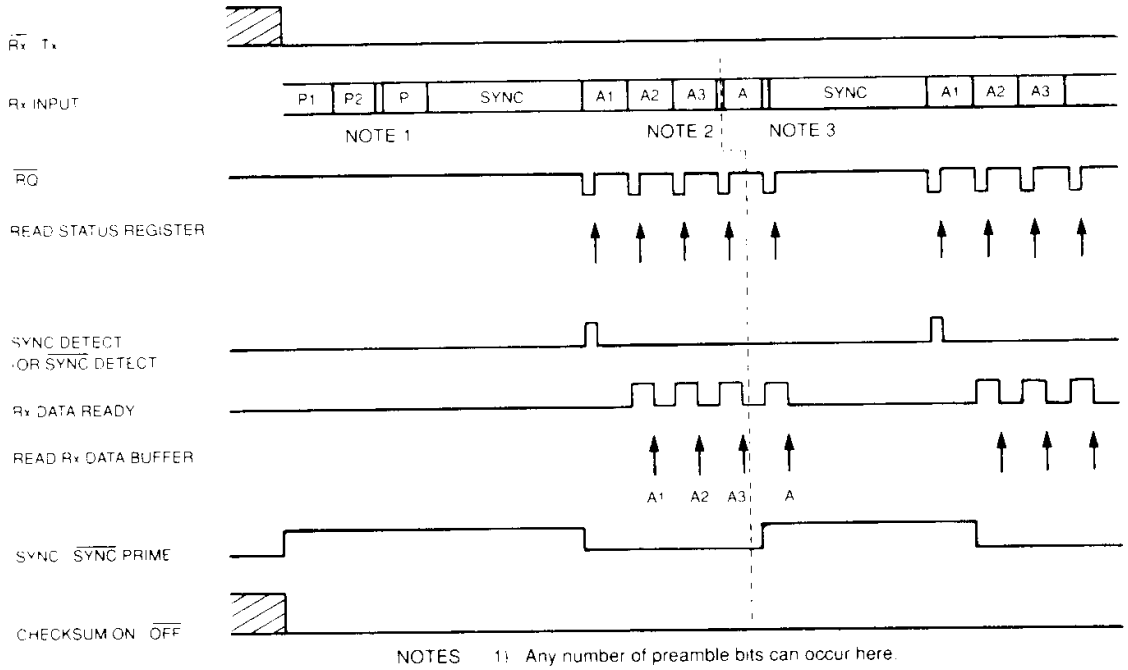
NOTES
1). H is the "Hangover" bit (Logic 1) appended to the transmitted message before transmission is terminated.
2). Any number of preamble bytes can occur here.
3). Any number of address/data bytes can occur here.
4). Transmission terminates when no more data bytes are loaded into the Tx data buffer.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes.
iv). H – Hang bit.
v). P – Preamble bytes.
vi). Z – Don't care state.
vii). Tx only – In Tx, Preamble and SYNC are loaded as data from the microcontroller.

Fig.7 Tx Timing

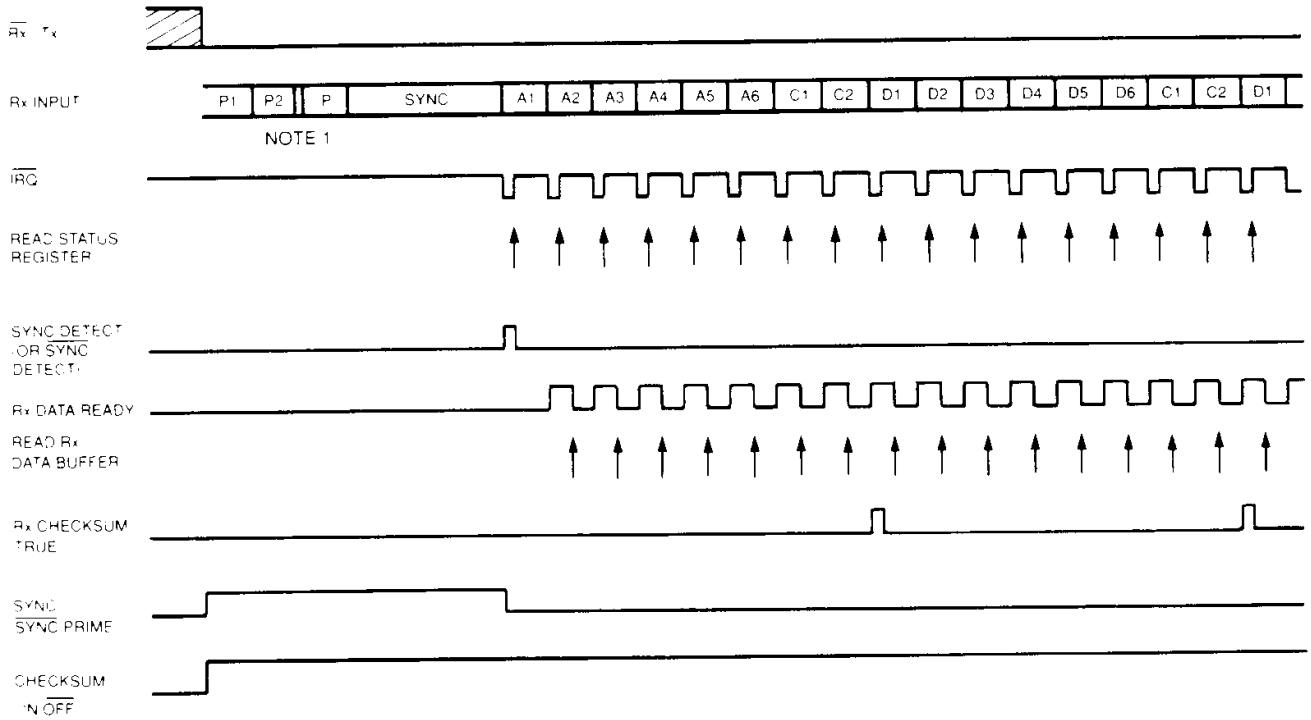
Rx Timing Information

(a) Rx SYNC/ $\overline{\text{SYNC}}$ REQUIRED BEFORE EVERY MESSAGE, Rx CHECKSUM NOT ENABLED.



NOTES
1). Any number of preamble bits can occur here.
2). Any number of address/data bytes can occur here.
3). Any number of bits can occur here.
4). Rx Freeformat set high.

(b) RX ADDITIONAL DATA FOLLOWS INITIAL ADDRESS (6 DATA & 2 CHECKSUM BYTES) DATA, RX CHECKSUM ENABLED.



NOTES
1). Any number of preamble bits can occur here.
2). Rx Freeformat set high.

NOTES
i). A – Address bytes.
ii). C – Checksum bytes.
iii). D – Data bytes
iv). H – Hang bit.
v). P – Preamble bytes.
vi). X – Don't care state
vii). Tx only – In Tx. Preamble and SYNC are loaded as data from the microcontroller

Fig.8 Rx Timing

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX809J**	-40°C to +85°C (cerdip)
	FX809LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX809J**	-55°C to +125°C (cerdip)
	FX809LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.032MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.

Bit Rate = 1200bp/s.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled		–	5.0	–	mA
Powersave		–	2.0	–	mA
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	–	–	V
Output Logic "0" (IOL = 360µA)	2, 3	–	–	0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	1	–	–	1.0	µA
Digital Input Capacitance	1	–	–	7.5	pF
Tri-state "Off" Leakage Current	8	-4.0	–	4.0	µA
Analogue Impedances					
Rx Input		100	–	–	kΩ
Tx Output					
Transmitting Data		–	6.0	10.0	kΩ
Not Transmitting Data		–	1.0	–	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		5.0	–	15.0	kΩ
Gain		–	15.0	–	dB
Frequency	4	–	4.032	–	MHz
Receiver					
Signal Input Levels	5	-9.0	-2.0	10.5	dB
Bit Error Rate					
at 12dB SNR		–	7.0	–	10^{-4}
at 20dB SNR		–	1.0	–	10^{-8}
Synchronization at 12dB SNR	6				
Probability of Bit 8 being correct		–	99.0	–	%
Probability of Bit 16 beng correct		–	99.5	–	%

Specification...

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values					
Transmitter					
Output Level		–	0	–	dB
Output Level Variation		-1.0	–	1.0	dB
Output Distortion		–	3.0	5.0	%
3rd Harmonic Distortion		–	2.0	3.0	%
Logic "1" Frequency	7	–	1200	–	Hz
Logic "0" Frequency	7	–	1800	–	Hz
Isochronous Distortion					
1200Hz – 1800Hz		–	25.0	40.0	µs
1800Hz – 1200Hz		–	20.0	40.0	µs
Uncommitted Amplifier					
Bandwidth		–	200	–	kHz
Gain		–	50.0	–	dB
Input Impedance		1.0	–	–	MΩ
Output Impedance		–	–	10.0	kΩ

Notes

1. Device control pins; Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. $\overline{\text{IRQ}}$ output.
4. For baud rate specified (1200 baud).
5. Signal-to-Noise Ratio = 50dB.
6. The response time is measured using a 10101010.....101 signal input pattern at 230mVrms (-2.5dB) with no noise.
7. Dependant upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs, for $V_{SS} < V_{OUT} < V_{DD}$.

Generation

The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

Checking

The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

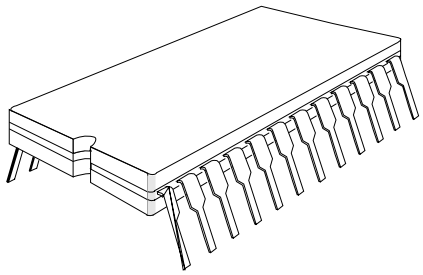
The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (Status Register bit-1) is set.

Package Outlines

The FX809 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX809J 24-pin cerdip DIL (J4)

NOT TO SCALE



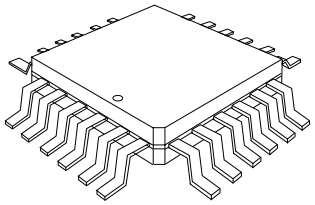
Max. Body Length 32.03mm
Max. Body Width 14.81mm

Handling Precautions

The FX809 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX809LG 24-pin quad plastic encapsulated bent and cropped (L1)

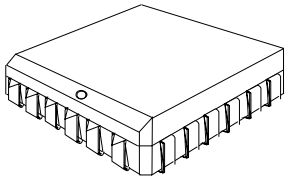
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX809LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX809J	24-pin cerdip DIL	(J4)
FX809LG	24-pin encapsulated bent and cropped	(L1)
FX809LS	24-lead plastic leaded chip carrier	(L2)