CML Semiconductor Products

PRODUCT INFORMATION

FX326 Audio Bandpass Filter

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Features/Applications

- 300Hz – 3000/3400Hz Audio Bandpass Filter
- Low Group Delay Distortion
- On-Chip Uncommitted Amplifier
- Range of Usable Xtal/Clock Frequencies
- Switched Capacitor Filters
- Chip Enable Powersave Feature
- Plastic DIL and SMD Packages
- General Purpose Audio Filtering
- Mobile and Portable Radio
- Data Signalling – Modems
- Portable Audio Equipment
- Delta and PCM Audio Filtering
- Cordless Telephones and Intercoms
- PABX and Trunk Equipment

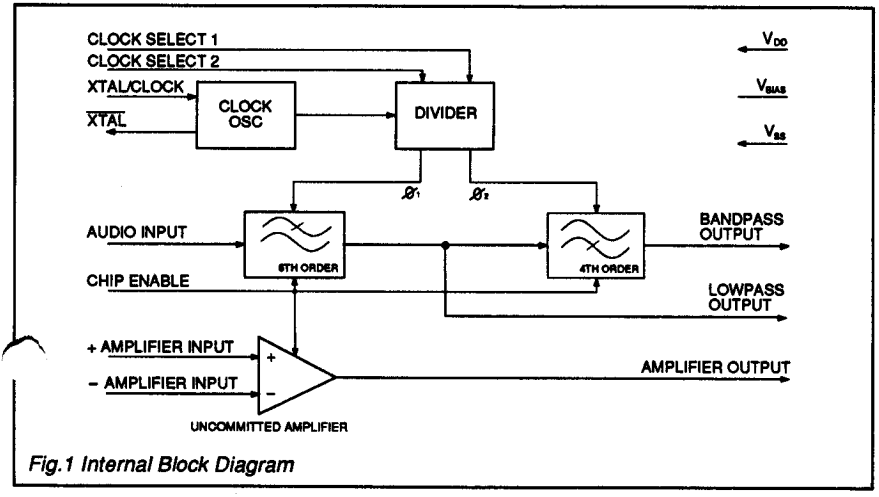


Fig.1 Internal Block Diagram

FX326

Brief Description

The FX326 is a general purpose low-power CMOS switched capacitor audio bandpass filter.
The filter frequency response is clock related and with the pin programmable divider allows for standard (300Hz - 3000/3400Hz) or non-standard frequency responses.

The device in detail consists of:

(1) A 6th order low group delay distortion lowpass filter.
(2) A 4th order highpass filter.
(3) An uncommitted amplifier.
(4) On-chip clock circuitry.

The two filters are connected in series, thus providing an audio bandpass filter output, the lowpass filter output may be used independently.

An on-chip oscillator requiring a Xtal, resonator or external clock pulse input provides all reference clocks for the switched capacitor filters. The two clock select lines (S1, S2) enable the device to be used with various clock frequencies without significantly altering the filter response. Additionally the clock select inputs provide the facility to shift the filter cut-off frequencies, allowing non-standard bandpasses and lowpasses to be produced. The chip enable input, when a logic '0,' will disable the filter and amplifier sections, thus reducing current consumption. The uncommitted amplifier may be used for any specific application such as pre-emphasis, de-emphasis, buffering, gain, etc.
The FX326 Audio Bandpass Filter is available in 14-pin Plastic DIL and 24-pin SMD packages.

Pin Number		Function
Quad FX326LG	DIL FX326P	
1	1	V_{DD} : Positive supply rail. A single +5 volt power supply is required.
2	2	**Select 2** (S2) : Control inputs to the clock programmable divider. The configuration of these inputs selects a division ratio (n), which with the input clock frequency (f_C) is used to select either the *upper* (f_H) or *lower* (f_L) filter cut-off frequency. The division ratio (n) is achieved
3	3	**Select 1** (S1) : using S1 and S2 as shown in the following table :

S1	S2	n
0	0	10
0	1	6
1	0	20
1	1	12

The lower (-3dB) cut-off frequency (f_L) and the upper (-3dB) cut-off frequency (f_H) are calculated using the formulas described below.

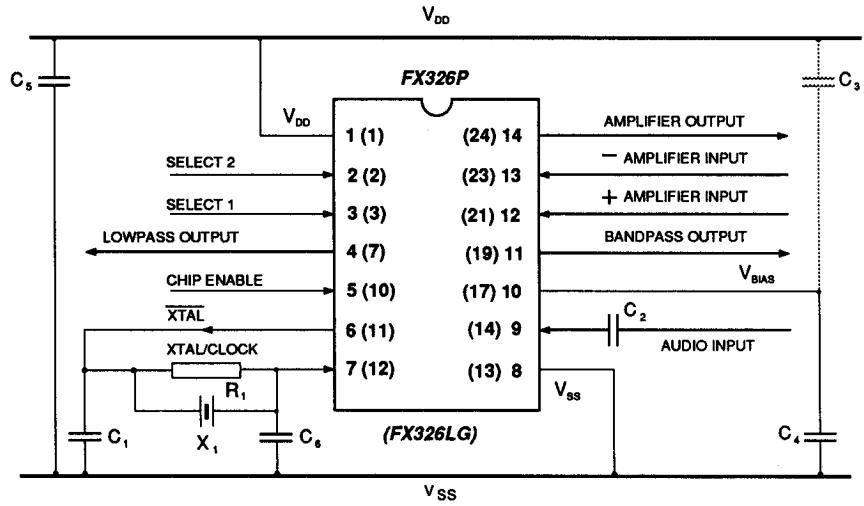
$$f_L = \frac{2.5 \times f_C}{n} \qquad f_H = \frac{34 \times f_C}{n}$$

where : f_L and f_H are calculated in Hz.
f_C is the Clock Frequency in kHz.
n is the Division Ratio set by inputs S1 and S2.

Inputs S1 and S2 each have internal 1MΩ pulldown resistors (n = 10).

7	4	**Lowpass Output :** The audio output of the lowpass filter section whose upper cut-off frequency (-3dB) is determined by the input clock frequency (f_C) and the selection control inputs, S1 and S2, see Figure 5. This output is internally biased to V_{BIAS}.
10	5	**Chip Enable :** Internally pulled to V_{DD} (logic'1') - enabling this device. A logic '0' applied to this pin will disable all filters and the uncommitted amplifier, putting the device into powersave to reduce current consumption.
11	6	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter. The clock oscillator remains powered in powersave. See Figure 2 (circuitry).
12	7	**Xtal/Clock :** The input to the clock oscillator inverter. A Xtal, resonator or externally derived clock pulse (f_C) is applied to this input. The clock frequency (f_C), with selection control inputs S1 and S2 will determine the upper and lower (-3dB) filter cut-off frequencies. See Figures 2, 3, 4 and 5.
13	8	V_{SS} : Negative supply rail (GND).
14	9	**Audio Input :** The input to the Lowpass/Bandpass filters. This input should be a.c. coupled using capacitor C_2, see Figure 2.
17	10	V_{BIAS} : The output of the on-chip analogue bias circuitry, held at $V_{DD}/2$. Remains at V_{BIAS} during powersave. This pin requires to be decoupled to V_{SS} by capacitor C_4, see Figure 2.
19	11	**Bandpass Output :** The audio bandpass output, whose upper and lower cut-off frequencies (-3dB) are determined by the input clock frequency (f_C) and the selection control inputs, S1 and S2.
21	12	**Amplifier Input (+ve) :** The uncommitted amplifier non-inverting input.
23	13	**Amplifier Input (-ve) :** The uncommitted amplifier inverting input.
24	14	**Amplifier Output :** The output of the uncommitted amplifier.
4,5,6, 8,9,15,16, 18,20,22.		No internal connection, do not use.

Application Information



Component	Value	Note	Component	Value	Note
R_1	1MΩ	1	C_4	0.1µF	2
C_1	33pF	1	C_5	0.1µF	
C_2	0.1µF		C_6	33pF	1
C_3	0.1µF	2	X_1	Xtal/Resonator	3

Tolerances : R = 10%. C = 20%.

Notes

1. Xtal/Clock components shown are in accordance with CML application note D/XT/1 April 1986. This input can be either a Xtal/Resonator circuit as shown, or a clock 'pulse' input.
2. V_{BIAS} may be decoupled to V_{SS} and V_{DD}. For input signals referenced to V_{SS}, decouple V_{BIAS} to V_{SS} using C_4 only.
3. Xtal/clock frequencies are dependant upon required filter responses – Table 1, Figures 4 and 5.

Fig.2 Recommended External Component Connections

Table 1 shows the upper or lower cut-off frequencies that can be achieved with differing combinations of Clock Rate (f_C) and Division Ratio (n) using the formulas described on Page 2 (pins 2 and 3). Typical bandpass characteristics using a 1.0MHz clock are displayed in Figure 3.

Clock f_C *(kHz)*	Division Ratio n	Lower Cut-Off *(-3dB)* f_L *(Hz)*		Upper Cut-Off *(-3dB)* f_H *(Hz)*	Bandwidth *(Hz)*
560	6	233	–	3173	2940
	10	140	–	1904	1764
	12	116	–	1586	1470
	20	70	–	952	882
1000	6	416	–	5666	5250
	10	250	–	3400	3150
	12	208	–	2833	2625
	20	125	–	1700	1575
1500	6	625	–	8500	7875
	10	375	–	5100	4725
	12	312	–	4250	3938
	20	187	–	2550	2363
2000	6	833	–	11333	10500
	10	500	–	6800	6300
	12	416	–	5666	5250
	20	250	–	3400	3150
2500	6	1041	–	14166	13125
	10	625	–	8500	7875
	12	520	–	7083	6563
	20	312	–	4250	3983

Table 1 Examples of Upper and Lower Cut-Off Frequencies

Application Information

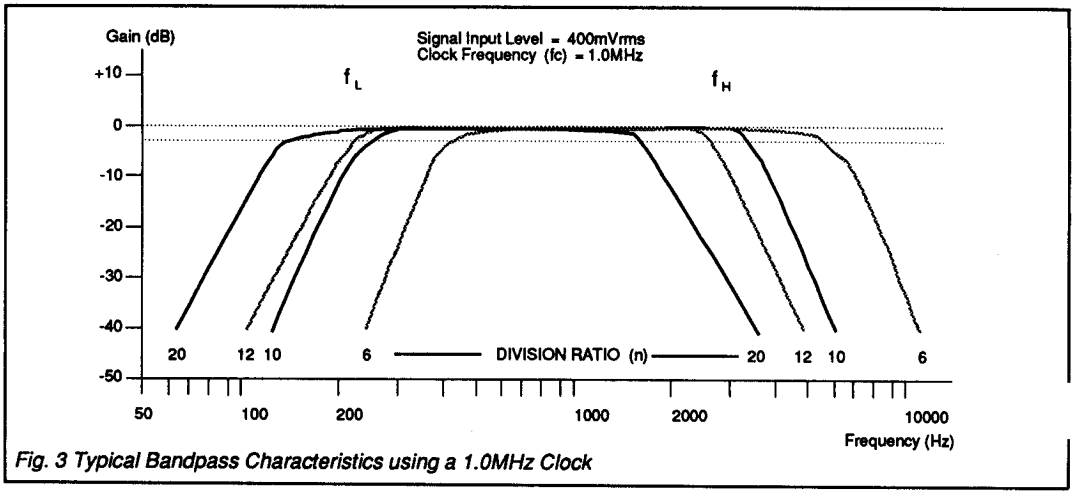


Fig. 3 Typical Bandpass Characteristics using a 1.0MHz Clock

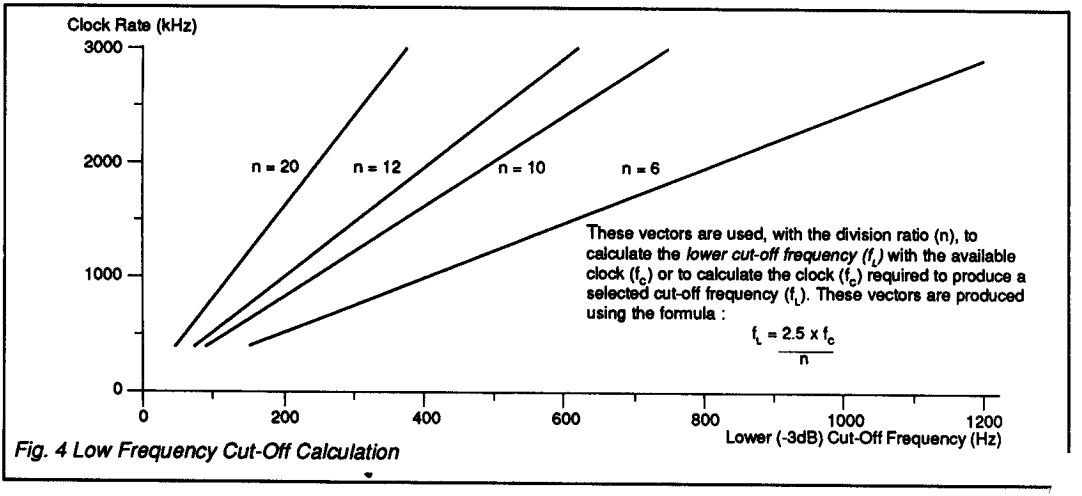


Fig. 4 Low Frequency Cut-Off Calculation

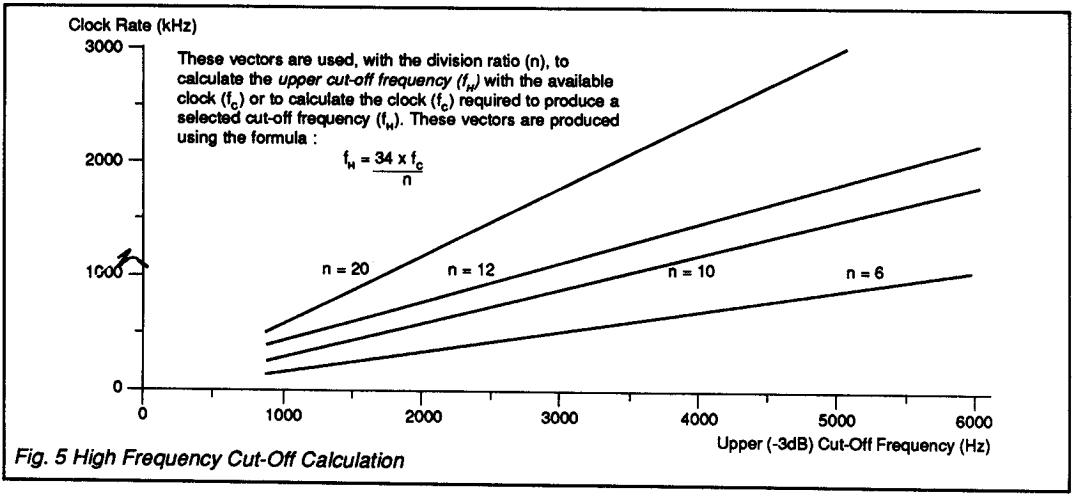


Fig. 5 High Frequency Cut-Off Calculation

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX326LG/P**	-30°C to +70°C
Storage temperature range: **FX326LG/P**	-40°C to +85°C

Operating Limits

All device characteristics are measured using the following parameters unless otherwise specified :
V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_c = 1.0 MHz. n = 10 *(S1 & S2 logic '0')*. Audio level 0dB ref: = 400mV rms.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (Enabled)		–	3.5	–	mA
Supply Current (Powersave)		–	1.0	–	mA
Input Logic '1'		3.5	–	–	V
Input Logic '0'		–	–	1.5	V
Input Impedance					
Filters and Amplifier		100	–	–	kΩ
Logic		–	1.0	–	MΩ
Output Impedance					
Filters		–	3.0	–	kΩ
Amplifier – Open Loop		–	800	–	Ω
Amplifier – Closed Loop		–	6.0	–	Ω
Clock Oscillator Inverter					
R_{in}		–	10.0	–	MΩ
R_{out}		–	10.0	–	kΩ
Gain		–	15.0	–	dB
Gain Bandwidth Product		–	5.0	–	MHz
Clock Frequency (f_c) Limits	1	0.5	–	3.0	MHz
Dynamic Values					
Signal Input Range	2	–	0	8.0	dB
Output Noise Level	3	–	-48.0	–	dB
Insertion Loss	4	–	0	–	dB
Group Delay Distortion (300Hz – 3400Hz)	6	–	–	200	µs
Cut-off Frequency -3dB					
Lowpass - (f_H)		–	3400	–	Hz
Highpass - (f_L)		–	250	–	Hz
Stopband Attenuation					
f > 6kHz		–	47.0	–	dB
f < 200Hz		–	27.0	–	dB
Aliasing Frequency		–	f_c/2n	–	Hz
Uncommited Amplifier					
Open Loop Gain	5	–	30.0	–	dB
Gain Bandwidth Product		–	1.0	–	MHz

Notes
1. These frequency limits are those at which the High or Low cut-off frequencies are in accordance with the formulas described in Figures 4 and 5.
2. Upper figure gives 3% distortion in 30dB SINAD. Typical figure gives minimum distortion in maximum SINAD.
3. Measured at the Bandpass Output with the Audio Input a.c. short circuit.
4. Input frequency 1.0kHz.
5. Relative to 1.0kHz at 100mV rms input.
6. Reference frequency 800Hz. See Figure 7.

Application Information...

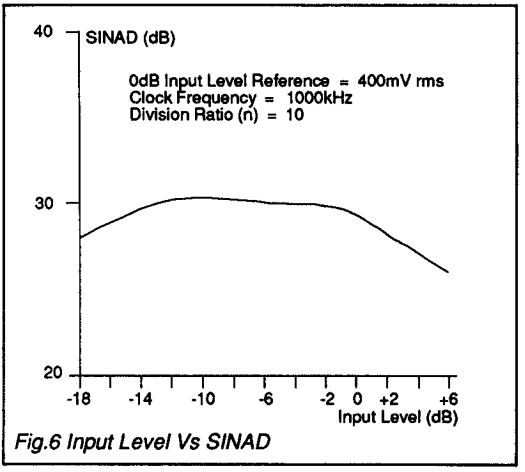


Fig.6 Input Level Vs SINAD

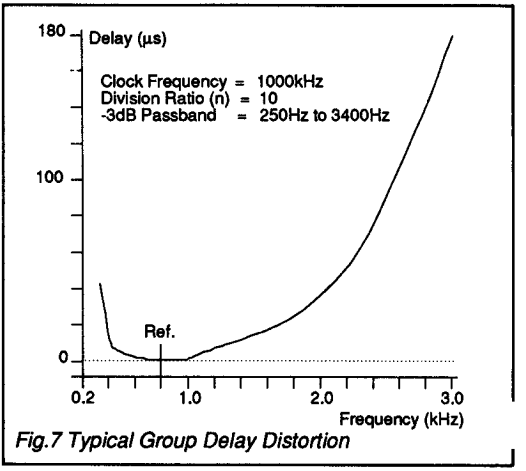


Fig.7 Typical Group Delay Distortion

Package Outlines

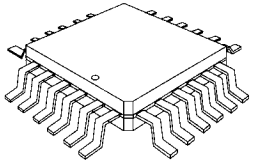
The FX326 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX326 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX326LG 24-pin plastic encapsulated bent and cropped (L1)

NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX326P 14-pin plastic DIL (P2)

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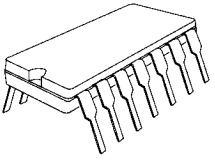

Max. Body Length 19.24mm
Max. Body Width 6.41mm

Ordering Information

FX326LG 24-pin plastic encapsulated bent and cropped (L1)

FX326P 14-pin plastic DIL (P2)