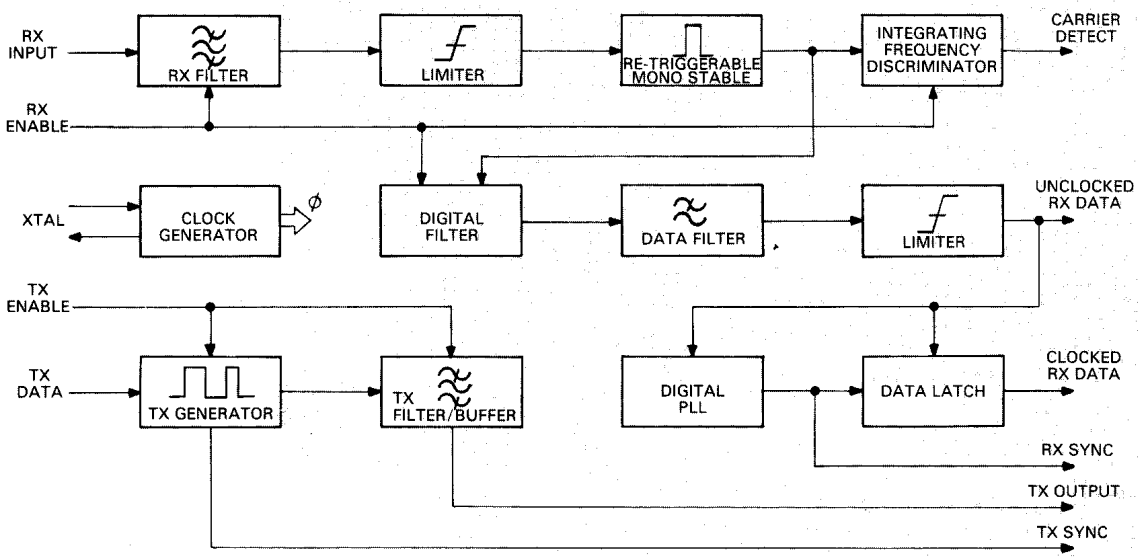
CONSUMER MICROCIRCUITS LTD

Obsolete Product
- For Information Only -

Publication D/409/3 February 1985

Features

- **1200 Baud FFSK Modem**
- **Single Chip CMOS LSI**
- **Low Power Operation**
- **On-Chip Bandpass Filter**
- **On-Chip Clock Recovery**
- **Few External Parts**
- **Carrier Detect Facility**
- **Full Duplex 1200 Baud**
- **Choice of Package Styles**



FX409

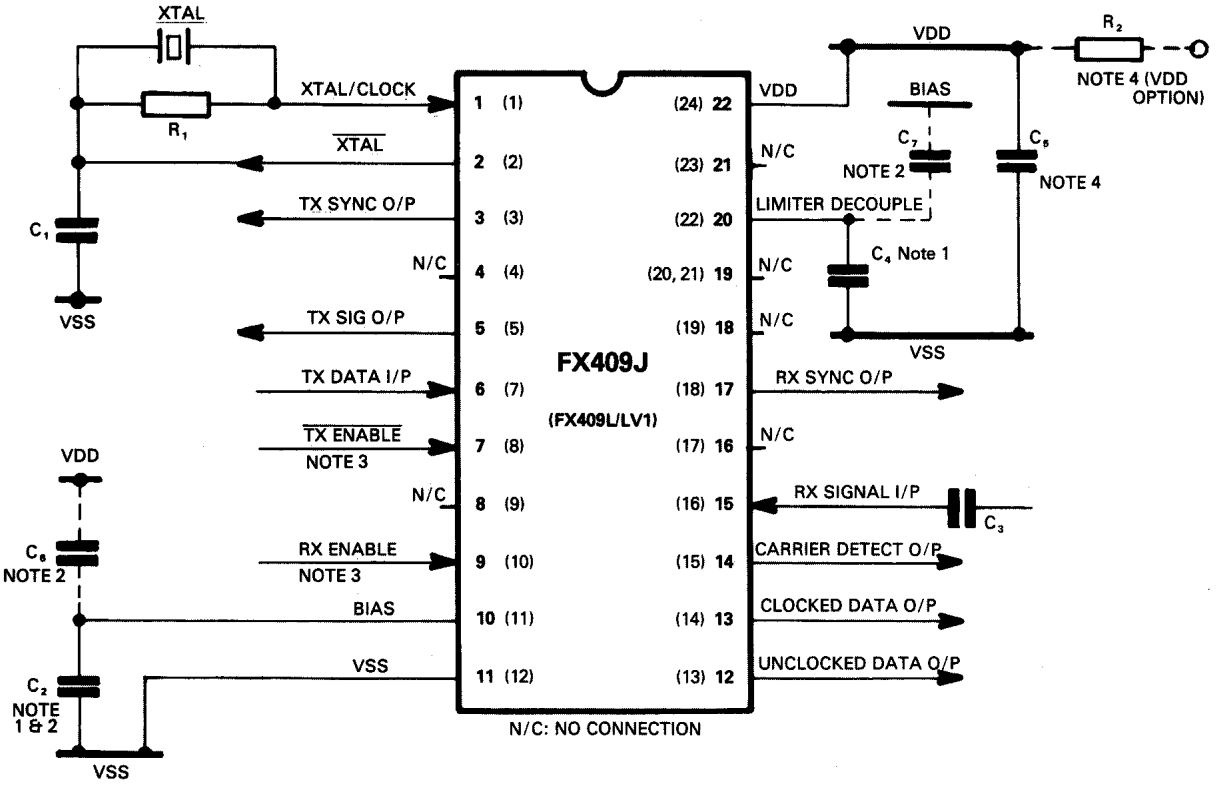
Fig. 1 Internal Block Diagram

Brief Description

The FX409 is a single chip CMOS LSI circuit which operates as a 1200 baud FFSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, TX synchronisation and RX synchronisation are all derived from an on-chip crystal oscillator for high stability and an external 1.008MHz crystal is required for this purpose. The device includes circuitry for carrier detect and facility for the RX clock recovery circuitry. An on-board switched capacitor 900Hz—2100Hz bandpass filter provides optimum noise filtration. The use of switched capacitor analogue filters and digital signal processing results in excellent dynamic performance with few external components, the CMOS process and current saving techniques offer low standby supply current for portable battery powered applications.

Pin Description Function

D.I.L. FX409J	Quad Plastic FX409L/LV1	
1	1	**Xtal/Clock:** The input to an on-chip inverter for use with a 1.008MHz xtal. Alternatively a 1.008MHz clock may be used.
2	2	**$\overline{\text{Xtal}}$:** Output of on-chip inverter.
3	3	**TX Sync O/P:** A 1200Hz squarewave used to synchronize the input of logic data and transmission of the FFSK signal (see Fig. 4).
4	4	**No Connection:** Leave open circuit.
5	5	**TX Signal O/P:** With transmitter disabled, this pin is set to a high impedance state. When transmitter is enabled, this pin outputs the 1200/1800Hz (140 step pseudo-sinewave) FFSK signal (see Fig. 4).
6	7	**TX Data I/P:** Serial logic data to be transmitted, is input to this pin and synchronized by the "TX Sync O/P" (see Fig. 4).
7	8	**$\overline{\text{TX Enable}}$:** A logic 1 applied to this input will put the transmitter into powersave whilst forcing "TX Sync O/P" to logic 1 and "TX Signal O/P" to a high impedance state. A logic 0 will enable the transmitter (see Fig. 4). Note: this input should be tied to either VSS or VDD (no internal pull up).
8	9	**No Connection:** Leave open circuit.
9	10	**RX Enable:** A logic 0 applied to this input will put the receiver into powersave whilst forcing "Clocked Data O/P", "Unclocked Data O/P" and "Carrier Detect" to logic 0. A logic 1 will enable the receiver (see Figures 2 & 5). "RX Sync Out" may be logic 1 or 0 during powersave. Note: This input should be tied to VSS or VDD (no internal pull up).
10	11	**Bias:** Provides bias internally and should be decoupled externally to VSS by a capacitor (see Fig 2).
11	12	**VSS:** Negative supply.
12	13	**Unclocked Data O/P:** This pin outputs recovered asynchronous serial data from the receiver.
13	14	**Clocked Data O/P:** This pin outputs recovered synchronous serial data from the receiver and is internally latched out by a recovered clock appearing on the "RX Sync O/P" pin (see Figures 2 & 5).
14	15	**Carrier Detect:** This pin will output a logic 1 when FFSK Signal is being received.
15	16	**RX Signal I/P:** This is the FFSK signal input pin for the receiver (see Figures 2 & 5).
16	17	**No Connection:** Leave open circuit.
17	18	**RX Sync O/P:** This is a flywheel 1200Hz squarewave output which upon presentation of FFSK data signal is synchronised internally to the incoming data (see Figures 2 & 5).
18	19	**No Connection:** Leave open circuit.
19	20, 21	**No Connection:** Leave open circuit.
20	22	**Limiter Decouple** Limiter decoupling (see Fig. 2)
21	23	**No Connection:** Leave open circuit.
22	24	**VDD:** Positive supply.

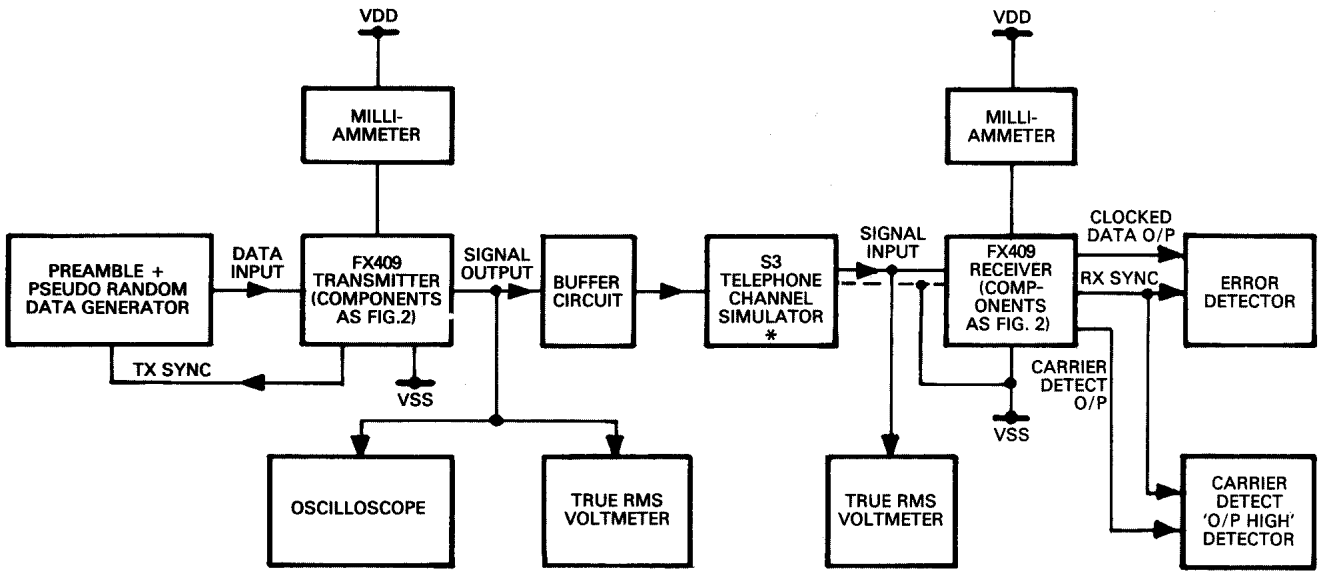


Component References		
Component	Recommended Unit Value	Tolerance %
R_1	1M	±10
R_2	—	±20
C_1	33p	±20
C_2	1μ	±20
C_3	0.1μ	±20
C_4	1μ	±20
C_5	1μ	±20
C_6	1μ	±20
C_7	1μ	±20

NOTES:

1. *Use C_2, C_4 when referencing all signals to VSS.*
2. *Use C_2, C_6, C_7 when referencing all signals to Bias (C_4, C_5 not required).*
3. *These inputs* must be tied *to either VSS or VDD. DO NOT LEAVE FLOATING.*
4. *R_2, C_6 may be used to further decouple power supply noise (R_2, C_6 typically 300μs).*

Fig. 2 External Component Connections



* Incorporates an attenuator & 5kHz BW noise generator.

Fig. 3 FX409 Test set-up

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref VSS = OV)		−0.3V to (VDD + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX409J	−30°C to + 85°C
	FX409L/LV1	−30°C to + 70°C
Storage temperature range:	FX409J	−55°C to +125°C
	FX409L/LV1	−40°C to + 85°C
Maximum device dissipation:		All versions 100mW

Operating Limits

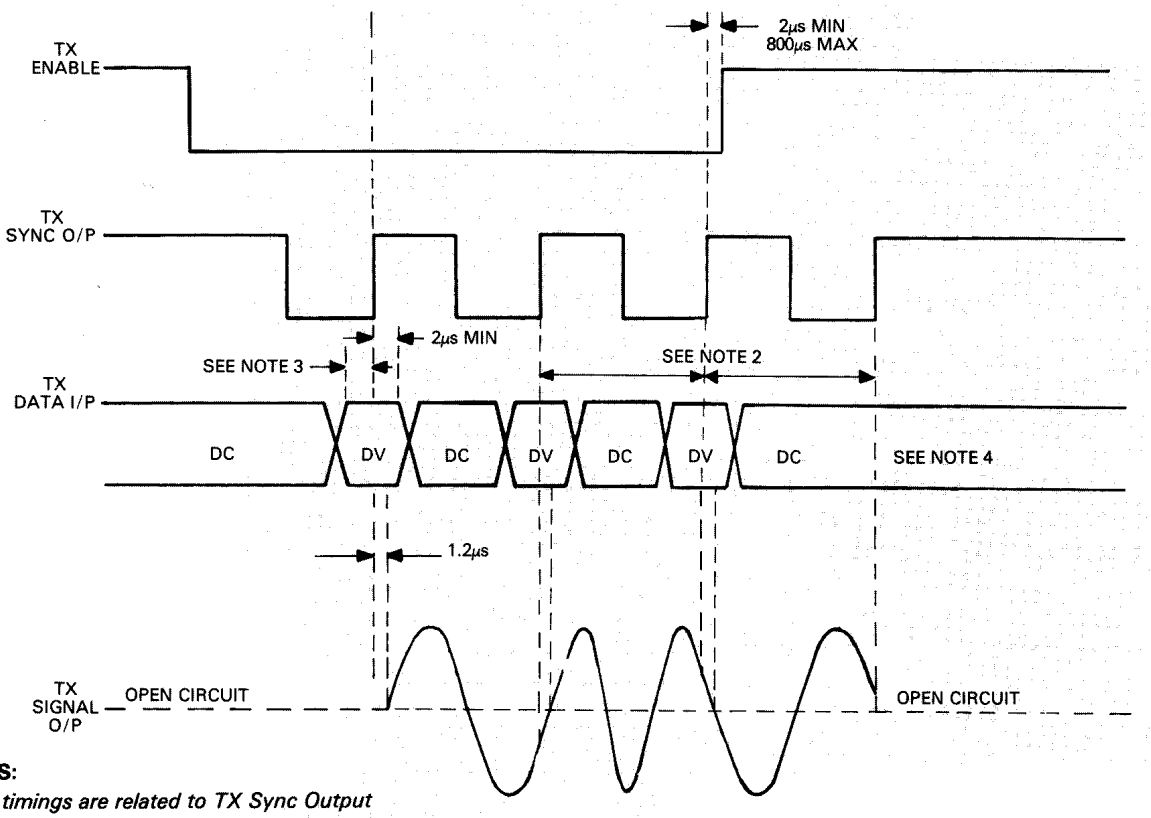
VDD = +5V, T_A = 25°C, ϕ = 1.008MHz (Xtal), $\Delta f\phi$ = 0

All characteristics measured using the standard test circuit (figure 3) with the following test parameters and is valid for all tests unless otherwise stated:

0dB reference	300mV rms
Noise	(band limited 5kHz gaussian white noise)
SNR ratio measured in bit rate bandwidth (1200Hz)	

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply volts		4.5	5.0	5.5	V
Supply current: RX (Enabled) TX (Disabled)			2.7	3.4	mA
RX (Enabled) TX (Enabled)			3.8	4.4	mA
RX (Disabled) TX (Disabled)			450	950	µA
Logic 1 level		80% VDD			V
Logic 0 level				20% VDD	V
Digital O/P Impedance			1		kΩ
Analogue and Digital input impedance		100			kΩ
TX O/P impedance				10	kΩ
On-chip crystal oscillator:					
R in		10			MΩ
R out		5		15	kΩ
Inverter gain		10		20	dB
Gain Bandwidth Product		3×10^6			
Crystal frequency	1		1.008		MHz
Dynamic Characteristics					
Receiver:					
Signal Input: Dynamic range (50dB SNR)	2	100		1000	mV rms
(12dB SNR)		100		700	mV rms
Bit Error Rate: 12dB SNR	2		1.3		10^{-3}
20dB SNR			1.0		10^{-7}
Receiver Synchronization 12dB SNR:					
Probability of bit 8 being correct			0.99		
Probability of bit 16 being correct			0.995		
Carrier Detect (101010 Pattern)					
Probability of Carrier Detect being high:					
12dB SNR after bit 8			0.99	0.98	
12dB SNR after bit 16			0.999	0.995	
0dB noise			0.03	0.065	
Transmitter O/P					
TX O/P level		1.0	1.1	1.2	V rms
Output level variation 1200/1800Hz		0	±0.2	±1.0	dB
O/P distortion			3	5	%
3rd harmonic distortion			2	3	%
Logic 1 carrier frequency	3		1200		Hz
Logic 0 carrier frequency	3		1800		Hz
Isochronous distortion					
1200Hz – 1800Hz			43		µs
1800Hz – 1200Hz			29		µs

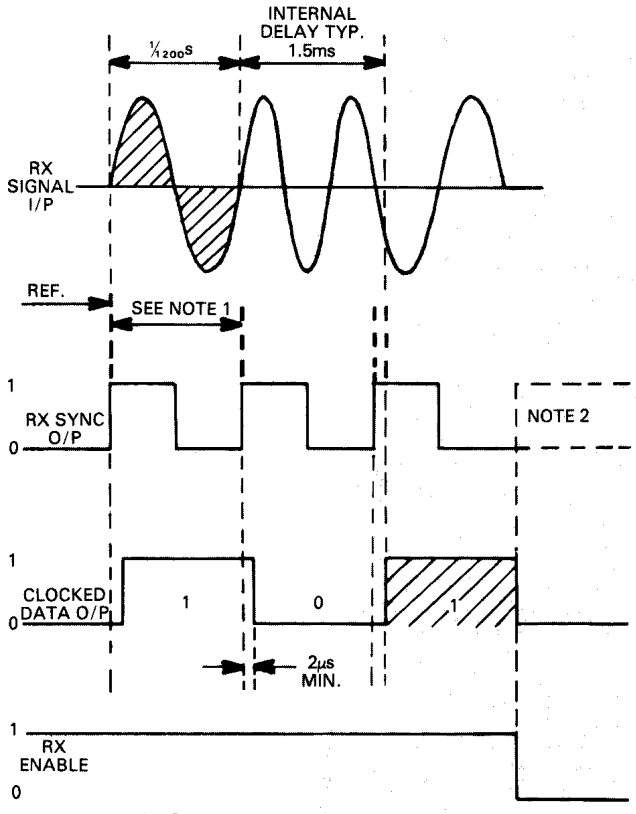
Note: 1. *Crystal tolerance depends on system requirements.*
2. *SNR (Bit Rate Bandwidth 1200Hz).*
3. *Depending on crystal tolerance.*



NOTES:

1. *All timings are related to TX Sync Output*
2. *0.833ms for 1.008MHz Crystal Input*
3. *2μs Min + Crystal tolerance*
4. *DC = Don't Care, DV = Data Valid*

Fig. 4 Transmitter Timing Diagram



NOTES:

1. *Minimum: 800μs* } *Valid for FX409 Xtals*
   Maximum: 865μs } *better than 1000 PPM.*
2. *May latch High or Low.*

Fig. 5 Receiver Timing Diagram

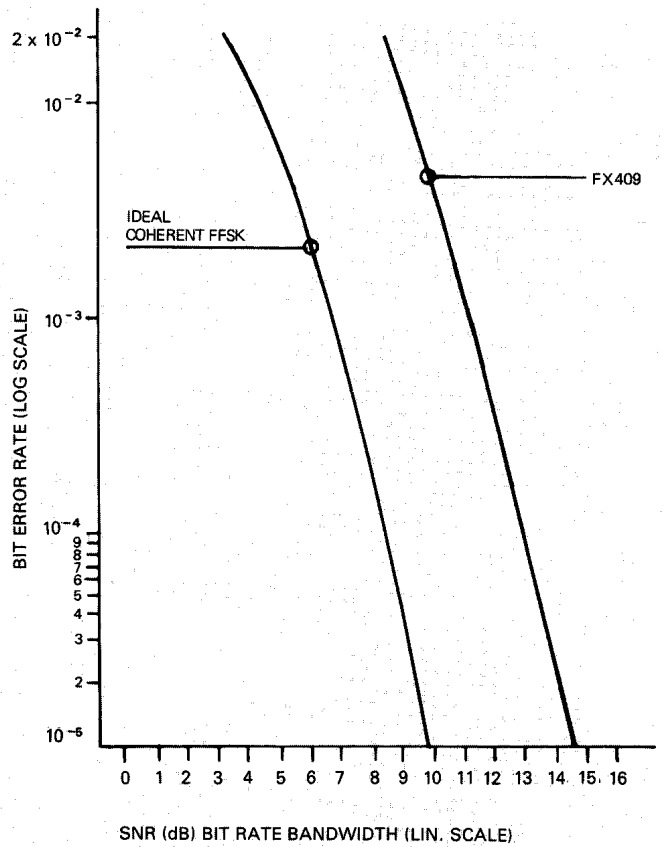
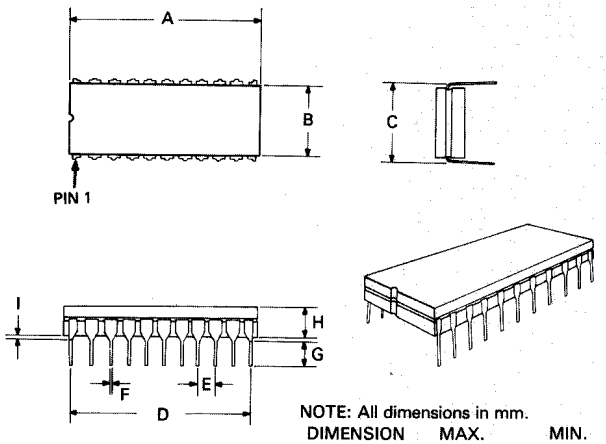


Fig. 6 Receiver B.E.R. vs SNR

Package Outlines

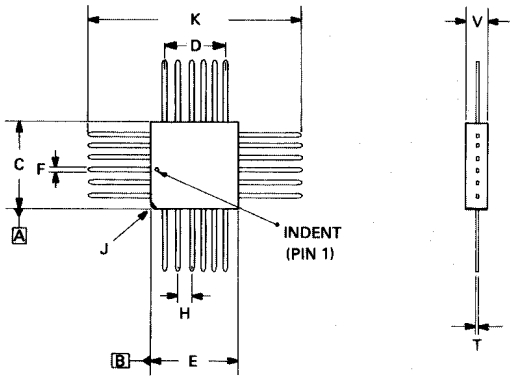
The cerdip package of the FX409J is shown in *Figure 7.* The plastic encapsulated FX409L of *Figure 8* is supplied in the disposable carrier for handling convenience. The FX409LV1 of *Figure 9* is supplied in a conductive tray.
The FX409L/LV1 has an indent (spot) adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 to allow complete identification. Pins number counter-clockwise when viewed from the top (indent side).

Fig. 7 FX409J D.I.L. Package



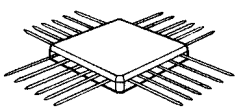
NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.
A	27.38	26.98
B	9.75	9.55
C	10.60	10.40
D	25.50	25.30
E	2.54	TYPICAL DIMENSION
F	0.46	
G	4.35	
H	2.11	1.95
I	—	0.5



NOTE: All dimensions in mm.

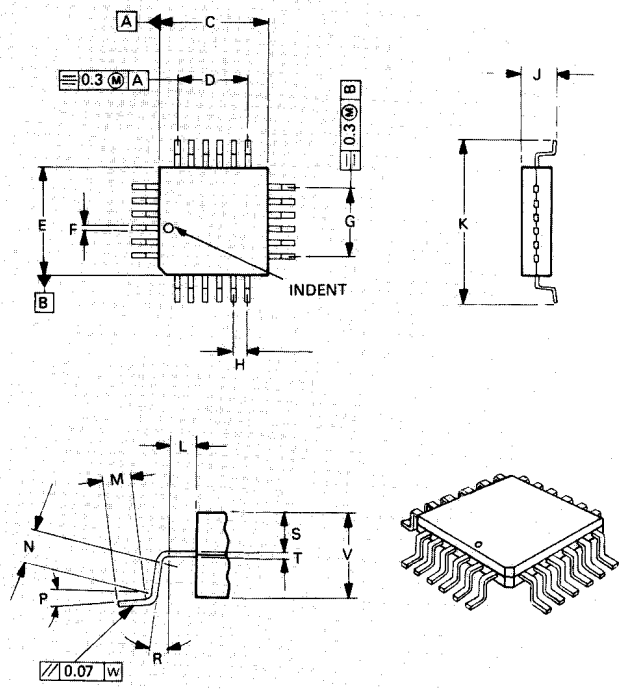
DIMENSION	MAX.	MIN.
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
H	1.30	1.24
J	CHAMFER	
K	21.54	21.24
T	0.22	0.16
V	3.02	2.44



Handling Precautions

The FX409J/L/LV1 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which can cause damage.

Fig. 9 ***FX409LV1*** *Package*



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.	DIMENSION	MAX.	MIN
A, B	Datum & Symmetry		M	1.0	0.8
			N	1.15	1.0
C	10.25	10.0	P	6.0°	5.0°
D	6.38	6.32	R	5.5°	4.5°
E	10.25	10.0	S	1.40	1.14
F	0.55	0.47	T	0.22	0.16
G	6.38	6.32	V	3.02	2.44
H	1.30	1.24	W//	0.07	—
J	3.40	3.33			
K	15.65	—			
L	1.0	0.85			

Ordering Information

FX409J 22-pin Cerdip D.I.L.
FX409L 24-pin quad plastic encapsulated.
FX409LV1 24-pin quad plastic encapsulated, bent and cropped.