CML Semiconductor Products

PRODUCT INFORMATION

FX465

Extended Code CTCSS Encoder/Decoder

Publication D/465/2 May 1996
Advance Information

Features

- **Low-Voltage (3-Volt) Supply**
- **47 Programmable Sub-Audio Tones + NOTONE**
- **Meets MPT1306 and TIA/EIA 603**
- **High Voiceband/CTCSS Isolation**
- **Separate Sub-Audio and Rx/Tx Audio Paths and Filtering**

Applications

- **Mobile Radio Systems**
- **Community Base Stations**
- **"Sports Radio" (Japan)**
- **Sub-Audio Signalling and Selective Calling**
- **Status and Alarm Systems**
- **Amateur Radio**

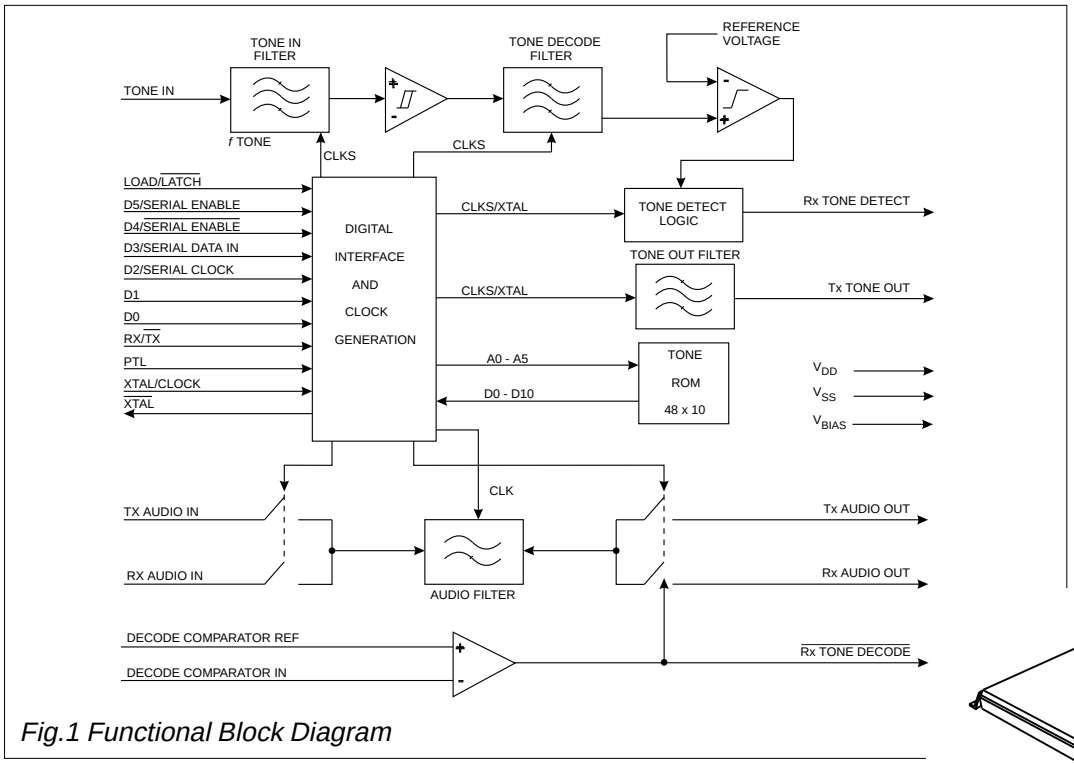
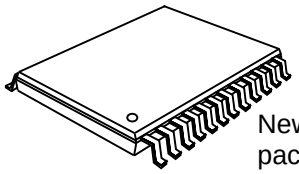


Fig.1 Functional Block Diagram

FX465



New SSOP **D5** package

Brief Description

The FX465 is a 3-volt, half-duplex predictive Continuous Tone Controlled Squelch System (CTCSS) encoder/decoder microcircuit. The FX465 has integral voice-band filtering for prefiltering of Tx audio and the rejection of the CTCSS tone in receive.

Under µProcessor control, the FX465 will encode and decode any one of 47 sub-audio frequencies (+NOTONE) in the range 67.0Hz to 254.1Hz. Tone frequencies and all functional commands can be loaded to the device in either pin-selectable 8-bit parallel or serial format.

A separate, Rx/Tx voice-audio path is available with a highpass (sub-audio reject) filter automatically placed in the relevant Rx or Tx voice line.

The Rx sub-audio (CTCSS) path contains a (selected tone frequency) bandpass filter and period detector providing a logic level output (Rx Tone Detect) to indicate a successful decode operation.

Rx "Press to Listen" (PTL) and Tx "Squelch-Tail Elimination" functions are available in both command loading modes. The squelch-tail elimination function will provide (Tx tone) phase-reversal to minimise the annoying audio outputs that occur at the receiver on completion of a transmission.

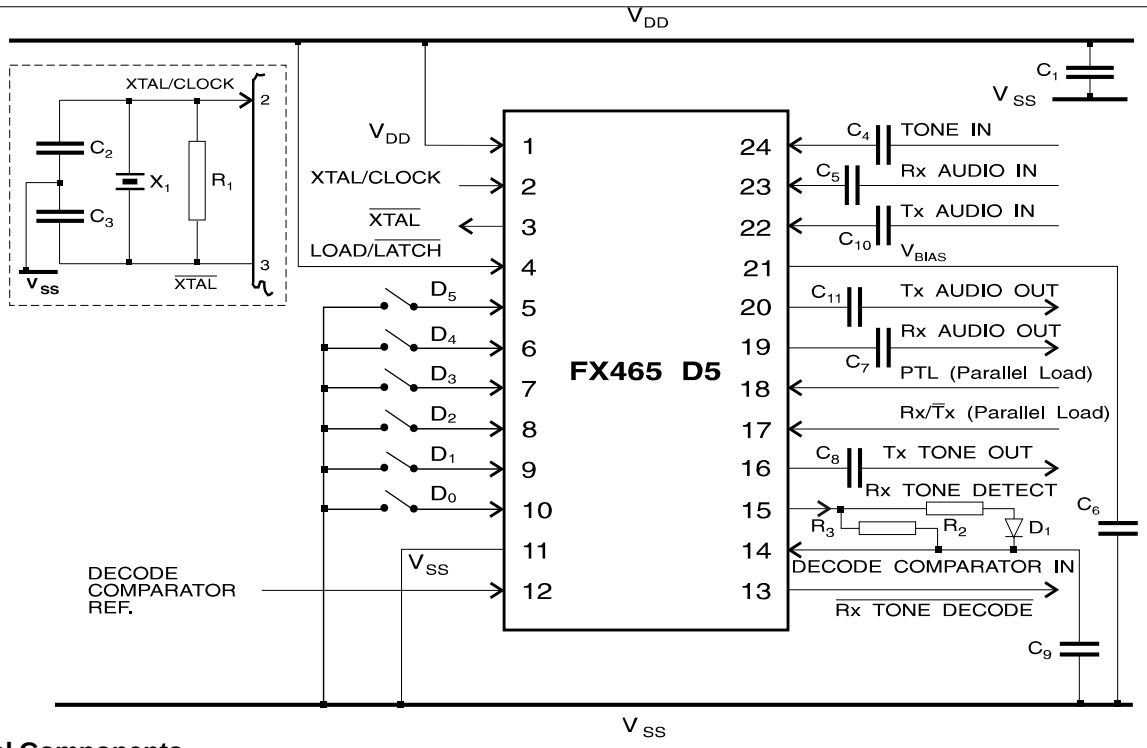
Tone frequencies and filter accuracies are maintained by an on-chip 4.0MHz clock oscillator employing an external crystal or clock pulse input.

The FX465, which exhibits high audio and sub-audio performance with low falsing, is available in a 24-pin plastic small outline SSOP package.

Pin Number FX465 D5	Function
1	**V_{DD}:** Positive supply.
2	**Xtal/Clock:** Input to the on-chip inverter; used with a 4.0MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**$\overline{\text{Load/Latch}}$:** Controls 8 on-chip latches and is used to latch Rx/$\overline{\text{Tx}}$, PTL, D_0 - D_5. This pin is internally pulled to V_{DD}. A logic '1' applied to this input puts the 8 latches into a 'transparent' mode. A logic '0' applied to this input puts the 8 latches into the 'latched' mode. In parallel mode data is loaded and latched by a logic '1' to '0' transition (see Figure 4). In serial mode data is loaded and latched by a '0' to '1' to '0' strobe pulse on this pin (see Figure 4).
5	**D_5/Serial Enable:** Data input D_5 (Parallel Mode); Serial Enable (Serial Mode). A logic 'l' applied to this input, together with a logic '0' applied to D_4/$\overline{\text{Serial Enable}}$, will put the device into 'Serial Mode' (see Figure 4). This pin is internally pulled to V_{DD}.
6	**D_4/$\overline{\text{Serial Enable}}$:** Data input D_4 (Parallel Mode); $\overline{\text{Serial Enable}}$ (Serial Mode). A logic '0' applied to this input, together with a logic '1' applied to D_5/Serial Enable, will place the device into 'Serial Mode' (see Figure 4). This pin internally pulled to V_{DD}.
7	**D_3/Serial Data In:** Data input D_3 (Parallel Mode); Serial Data Input (Serial Mode). In Serial Mode this pin becomes the serial data input for D_5 - D_0, Rx/$\overline{\text{Tx}}$, PTL (see Figure 4). D_5 is clocked-in first and PTL last. This pin internally pulled to V_{DD}.
8	**D_2/Serial Clock:** Data input D_2 (Parallel Mode); Serial Clock Input (Serial Mode). In Serial Mode this pin becomes the Serial Clock input. Data is clocked on the positive-going edge (see Figure 4). This pin is internally pulled to V_{DD}.
9	**D_1:** Data input D_1 (Parallel Mode); Not used (Serial Mode). This pin is internally pulled to V_{DD}.
10	**D_0:** Data input D_0 (Parallel Mode); Not used (Serial Mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.** (I/P)**:** Internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1.0MΩ resistors depending on the logical state of the Rx Tone Decode pin. Rx Tone Decode = logic '1' will bias this input to $2V_{DD}/3$, a logic '0' will bias this input to $V_{DD}/3$. This input provides the decode comparator reference voltage; switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.

Pin Number FX465 D5	Function
13	**$\overline{\text{Rx Tone Decode}}$** (O/P)**:** The gated output of the on-chip Decode Comparator. This output is used to gate the Rx Audio path. A logic '0' on this pin indicates a successful decode and that the 'Decode Comparator In' pin is more positive than the 'Decode Comparator Ref.' input (see Table 1).
14	**Decode Comparator In:** The inverting input of the Decode Comparator. This pin is normally connected to the integrated output of the Rx Tone Detect pin.
15	**Rx Tone Detect** (O/P)**:** In the Rx mode this output will go to a logic '1' during a successful decode (Table 1). This must be externally integrated to control response and deresponse times (Figure 2).
16	**Tx Tone Out:** The CTCSS sinewave output appears on this pin under the control of the Rx/$\overline{\text{Tx}}$ pin. This output, when not transmitting a sub-audio tone, may be biased to $V_{DD}/2$ as described in Table 1.
17	**Rx/$\overline{\text{Tx}}$:** This input (Parallel Mode) selects Rx or Tx modes (see Figure 2). Logic '1' = Rx; logic '0' = Tx. In Serial Mode this (Rx or Tx) function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** A dual-function input. In parallel Rx mode this pin operates as a "Push To Listen" function by enabling the Rx audio path, thus overriding the tone-squelch function. In the parallel load mode, Tx operation this input reverses the phase of the transmitting CTCSS tone (squelch tail elimination). In the serial load mode (Rx and Tx) these functions are serially loaded. Internal pull-up to V_{DD}.
19	**Rx Audio Out:** The high-pass filtered 'Received Audio' output. This pin outputs audio when Rx Tone Decode = '0', or PTL = '1' or when 'Notone' is programmed (Table 2). In Tx Mode this pin is biased to $V_{DD}/2$.
20	**Tx Audio Out:** The high-pass filtered 'Transmit Audio' output. In Tx mode this pin outputs audio present at the Tx Audio input by opening the Tx audio path. In Rx mode this pin is biased to $V_{DD}/2$.
21	**V_{BIAS}:** The output of the on-chip analogue bias circuitry. Held internally at $V_{DD}/2$, this pin should be externally decoupled to V_{SS} via a capacitor.
22	**Tx Audio In:** The Tx Audio Input pin. Tx voice-band audio may be prefiitered, using the audio path, thus helping to avoid talk-off due to the intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**Rx Audio In:** The input to the audio high-pass filter in the Rx Mode. This pin is internally biased to $V_{DD}/2$.
24	**Tone In:** The input to the CTCSS tone detector; this input is internally biased to $V_{DD}/2$.

Application Information



External Components

Component	Value	Tolerance	Component	Value	Tolerance
R_1	1.0MΩ	±10%	C_6	0.47µF	±20%
R_2	560kΩ	±10%	C_7	0.1µF	±20%
R_3	820kΩ	±10%	C_8	0.1µF	±20%
C_1	0.1µF	±20%	C_9	0.1µF	±20%
C_2	18pF	±20%	C_{10}	0.1µF	±20%
C_3	33pF	±20%	C_{11}	0.1µF	±20%
C_4	0.1µF	±20%	D_1	small signal type	
C_5	0.1µF	±20%	X_1	4.0MHz	±0.01%

Note: The values specified for R_1, C_2 and C_3 have been found to be satisfactory when used with a crystal (X_1) whose equivalent series resistance is <= 1000 ohms. The crystal manufacturer should be consulted to determine optimum values for different crystals.
The 0.1µF value for the dc blocking capacitors C_4, C_5, C_7, C_8, C_9, C_{10} and C11 are not a requirement. For the capacitors C_4, C_5 and C_{10}, the input impedance is internal to the device and specified as typically 550kΩ. For the remaining capacitors external circuits will be important in determining input impedance.

Fig.2 Recommended External Components

Input Pin Condition				*Output Pin Condition*		*Result and/or Function*				
D_0 to D_5	Rx/$\overline{Tx}$	PTL	Decode Comp. Input	Rx Tone Detect	$\overline{\text{Rx Tone Decode}}$	Tone Tx Enabled	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	Notes
TONE	0	0	x	0	1	YES	YES	NO	NO (BIAS)	1
NOTONE	0	x	x	0	1	NO (BIAS)	YES	NO	NO (BIAS)	2
TONE	1	0	0	0	1	NO (BIAS)	NO	YES	NO (BIAS)	3
TONE	1	1	0	0	1	NO (BIAS)	NO	YES	YES	4
TONE	1	x	1	1	0	NO (BIAS)	NO	YES	YES	5
NOTONE	1	x	x	x	0	NO (BIAS)	NO	YES	YES	6

NOTES
1 Normal tone transmit condition.
2 NOTONE programmed in Tx mode; tone transmit output set to $V_{DD}/2$. Tx audio path enabled.
3 Normal decode standby.
4 Normal decode standby with PTL used to enable audio.
5 Normal 'decode of correct CTCSS tone' condition; PTL has no effect.
6 NOTONE programmed in Rx mode; tone transmit output (BIAS). Rx audio path enabled.

Table 1 Combinations of Input/Output Conditions *x = don't care*

Application Information .....

Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS (Continuous Tone Controlled Subaudible Squelch) tone as a means of directing messages among user groups sharing the same RF frequencies. CTCSS modulates the transmitter with a discrete tone, from 39 standard CTCSS tones in the range (67.0Hz to 250.0Hz) according to TIA/EIA-603. There are an additional eight CTCSS tones not specified in TIA/EIA-603 that the FX465 will encode and decode. They are: 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz, for a total of 47 CTCSS tones plus NOTONE.

The FX465 also incorporates Tx/Rx on chip speech filters. In early CTCSS designs, Tx speech was not filtered from the CTCSS tone, rather the filtering was dependent upon the host transmitter's pre-emphasis network. At only 6dB/octave, the attenuation of speech components at higher CTCSS tones was only a few dB which resulted in talk-off (low frequency voice components unsquelching the receiver audio).

CTCSS Programming Table (All frequencies in Hertz (Hz))

TIA/EIA-603 Nominal Freq.	FX465 Freq.	Δfo %	D_5	D_4	D_3	D_2	D_1	D_0	Hex
67.0	66.98	-0.029	1	1	1	1	1	1	3F
69.3	69.32	0.024	1	1	1	0	0	1	39
71.9	71.901	0.001	0	1	1	1	1	1	1F
74.4	74.431	0.042	1	1	1	1	1	0	3E
77.0	76.965	-0.046	0	0	1	1	1	1	0F
79.7	79.677	-0.029	1	1	1	1	0	1	3D
82.5	82.483	-0.021	0	1	1	1	1	0	1E
85.4	85.383	-0.020	1	1	1	1	0	0	3C
88.5	88.494	-0.007	0	0	1	1	1	0	0E
91.5	91.456	-0.048	1	1	1	0	1	1	3B
94.8	94.76	-0.042	0	1	1	1	0	1	1D
97.4	97.435	-0.036	1	1	1	0	1	0	3A
100.0	99.96	-0.040	0	0	1	1	0	1	0D
103.5	103.429	-0.069	0	1	1	1	0	0	1C
107.2	107.147	-0.05	0	0	1	1	0	0	0C
110.9	110.954	0.049	0	1	1	0	1	1	1B
114.8	114.84	0.035	0	0	1	0	1	1	0B
118.8	118.793	-0.006	0	1	1	0	1	0	1A
123.0	123.028	0.023	0	0	1	0	1	0	0A
127.3	127.328	0.022	0	1	1	0	0	1	19
131.8	131.674	-0.095	0	0	1	0	0	1	09
136.5	136.612	0.082	0	1	1	0	0	0	18
141.3	141.323	0.016	0	0	1	0	0	0	08
146.2	146.044	-0.107	0	1	0	1	1	1	17
151.4	151.441	0.027	0	0	0	1	1	1	07
156.7	156.875	0.112	0	1	0	1	1	0	16
*159.8	159.936	0.085	1	1	0	0	0	1	31
162.2	162.311	0.069	0	0	0	1	1	0	06
167.9	167.708	-0.114	0	1	0	1	0	1	15
173.8	173.936	0.078	0	0	0	1	0	1	05
179.9	179.654	-0.137	0	1	0	1	0	0	14
* 183.5	183.680	0.098	1	1	0	0	1	0	32
186.2	186.289	0.048	0	0	0	1	0	0	04
* 189.9	190.069	0.089	1	1	0	0	1	1	33
192.8	192.864	0.033	0	1	0	0	1	1	13
* 196.6	196.329	-0.138	1	1	0	1	0	0	34
* 199.5	199.312	-0.094	1	1	0	1	0	1	35
203.5	203.645	0.071	0	0	0	0	1	1	03
* 206.5	206.207	-0.142	1	1	0	1	1	0	36
210.7	210.848	0.070	0	1	0	0	1	0	12
218.1	217.853	-0.113	0	0	0	0	1	0	02
225.7	225.339	-0.160	0	1	0	0	0	1	11
* 229.1	229.279	0.078	1	1	0	1	1	1	37
233.6	233.359	-0.103	0	0	0	0	0	1	01
241.8	241.970	0.070	0	1	0	0	0	0	10
250.3	250.282	-0.007	0	0	0	0	0	0	00
* 254.1	254.162	0.024	1	1	1	0	0	0	38
NOTONE			1	1	0	0	0	0	30
Serial Input Mode			1	0	Data	Clock	x	x	2X

* Not specified in the TIA/EIA-603 tone set.

Table 2 Tone Programming Information

Application Information .....

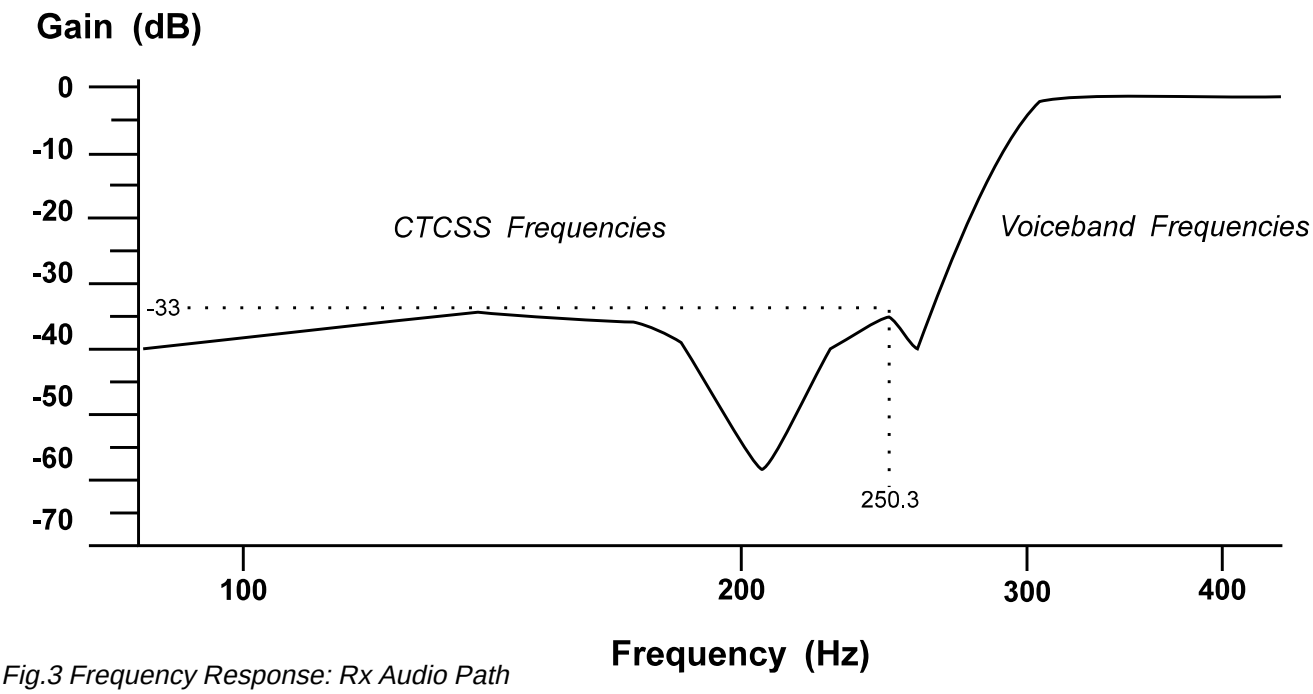


Fig.3 Frequency Response: Rx Audio Path

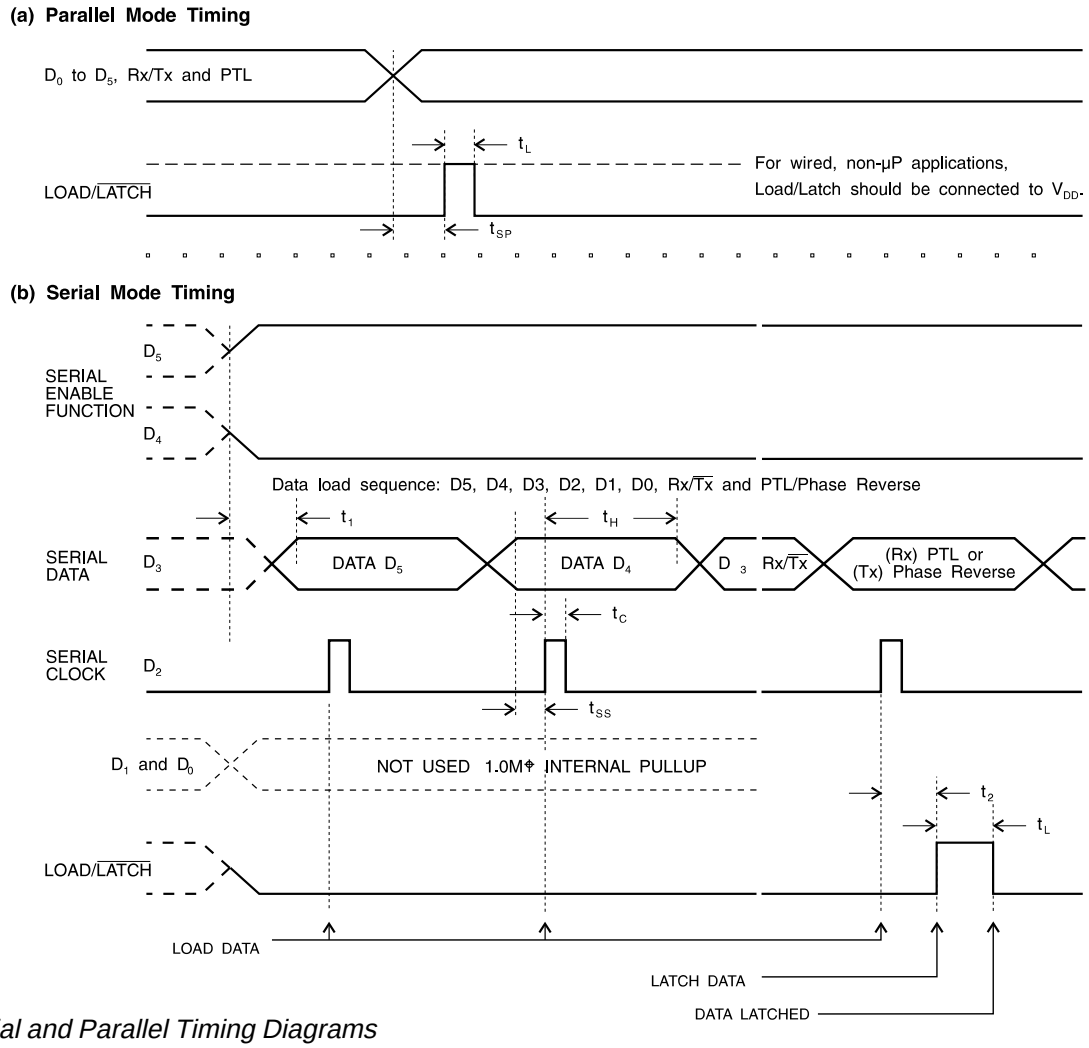


Fig.4 Serial and Parallel Timing Diagrams

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	550mW Max.
Derating	9mW/°C
Operating temperature range: **FX465 D5**	-40°C to +85°C
Storage temperature range: **FX465 D5**	-55°C to +125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:
V_{DD} = 3.3V to 5.0V. V_{SS} = 0V. T_{AMB} = 25°C. Xtal/Clock = 4.0MHz 100ppm. 0dB ref: = 750mVrms (proportional to V_{DD}, see Note 16.)
Composite Signal = 1.0kHz Test Tone at 300mVrms, Noise at 75mVrms (gaussian white noise, band-limited to 6.0kHz), Programmed CTCSS Tone at 30mVrms, fo = 100Hz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Characteristics					
Supply Voltage (V_{DD})		2.7	3.3/5.0	5.5	V
Supply Current					
V_{DD} = 5.0V		-	3.7	4.2	mA
V_{DD} = 3.3V		-	1.3	1.6	mA
Analogue Input Impedance		-	0.55	-	MΩ
Analogue Output Impedance		-	0.45	-	kΩ
Digital Input Impedance	1	-	35.0	-	kΩ
Input Logic '1'	1	70.0	-	-	%V_{DD}
Input Logic '0'	1	-	-	30.0	%V_{DD}
Output Logic '1', source = 0.1mA	2	80.0	-	-	%V_{DD}
Output Logic '0', sink = 0.1 mA	2	-	-	20.0	%V_{DD}
Dynamic Characteristics					
Decoder					
Pure Tone Decode Threshold		-	7.0	15.0	mVrms
Composite Tone Decode Threshold	3	-	-	30.0	mVrms
Decode Input Signal Level	15	-20.0	-	3.5	dB
Pure Tone Decode Response Time	12, 13	95.0	115	140	ms
Pure Tone Decode De-Response Time	12, 14	95.0	130	170	ms
Decode Response Time	3, 6, 9	-	-	250	ms
De-Response Time	3, 9	-	180	250	ms
Decode Selectivity: Decode Bandwidth	3, 10				
Upper Decode Band Edge		1.005fo	1.015fo	0.995fo+1	Hz
Lower Decode Band Edge		1.005fo-1	0.985fo	0.995fo	Hz
Encoder					
Tone Output Level	11	-1.0	0	1.0	dB
Tx Tone Frequency Accuracy (f_O error)		-0.3	-	+0.3	%f_O
Risetime to 90% (nominal output)					
f_O > 100Hz	4, 9	-	15.0	75	ms
f_O < 100Hz	4, 9	-	45.0	120	ms
Total Harmonic Distortion		-	1.5	2.0	%
Audio Filter					
Total Harmonic Distortion	5, 7	-	1.5	2.0	%
Output Noise Level	7	-	0.5	-	mVrms
(Input ac short cct, audio switch enabled)					
SINAD	7, 8	40.0	50.0	-	dB
Spurious Emissions		-	-	-48	dB
Cut-Off Frequency		-	300	-	Hz
Bandpass Ripple (300Hz – 3000Hz)	5, 7	-	1.0	1.8	dB
Stopband Attenuation <250Hz	5, 7	33.0	36.0	-	dB
Passband Gain at 1.0kHz		-0.5	0	0.5	dB

Specification .....

Characteristics	See Note	Min.	Typ.	Max.	Unit
Audio Switch					
Isolation	5	-	60.0	-	dB
Serial/Parallel Inputs					
Parallel Set-Up Time (t_{SP})		400	-	-	ns
Load/Latch Pulse Width (t_L)		400	-	-	ns
Serial Clock Pulse Width (t_C)		400	-	-	ns
Serial Set-Up Time (t_{SS})		400	-	-	ns
Serial Data Hold Time (t_H)		400	-	-	ns
Serial Enable Time (t_1)		400	-	-	ns
Serial Load/Latch Set-up Time (t_2)		400	-	-	ns
Serial Clock Frequency		-	1.0	-	MHz

Notes

1. Refers to Rx/Tx, PTL, Decode Comparator Input, D_0, D_1, D_2, D_3, D_4, D_5 inputs.
2. All logic outputs.
3. Composite Signal Test condition.
4. Any programming tone and RL = 10kΩ. CL = 15pF.
5. With an input level of 0dB at 1.0kHz.
6. f_O > 100Hz, (for 100Hz >f_O >67Hz: t = (100/f_O Hz) x 250ms).
7. Measured in a 30kHz bandwidth.
8. With an input level of -3.5dB at 1.0kHz
9. Per TIA/EIA-603.
10. Per TIA/EIA-603, device will not decode adjacent TIA/EIA-603 tones.
11. Tone output level is proportional to V_{DD}.
12. f_O = 156.7Hz at -20dB.
13. Typically 12.5 tone cycles + 40ms
14. Typically 7 tone cycles + 90ms.
15. Max composite signal is 3.5dB with: Noise (band limited 6kHz Gaussian) -12dB to 1kHz test tone F_0 CTCSS tone -20dB ref to 1kHz test tone.
16. For maximum dynamic range, set audio level to 0dB, V_{DD} x 150mVrms, using minimumV_{DD} under which system is intended to work. e.g. for a 2.7 to 3.3 volt system use 0dB equal to 405mVrms.

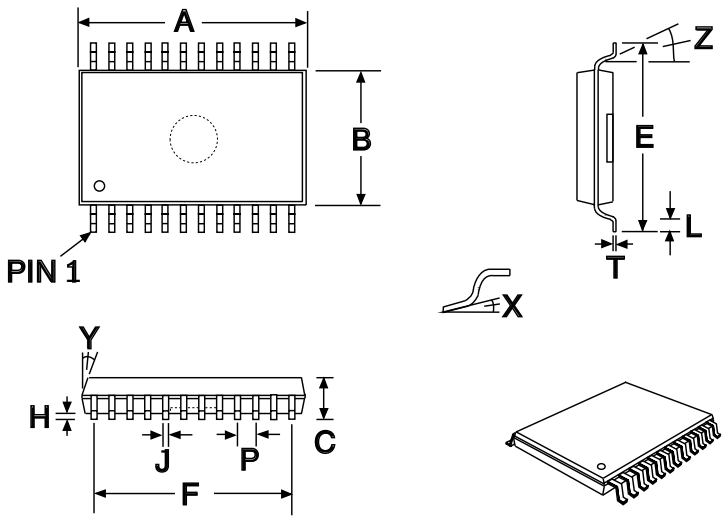
Package Outlines

The FX465 is available in the package styles outlined below. Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX465 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX465 D5 24-pin plastic S.S.O.P.



DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Ordering Information

FX465 D5 24-pin plastic S.S.O.P. (D5)