# CML Semiconductor Products

**PRODUCT INFORMATION**

# FX589 Low-Voltage/High-Speed GMSK Modem

Publication D/589/7 January 1998

## Features

- **Full-Duplex Gaussian Minimum Shift Keying (GMSK)**
  Operating from 3 Volts to 5.5 Volts
- **Data Rates 4kb/s to 64kb/s**
- **Selectable BT (0.3 or 0.5)**
- **Low-Current Analogue/Digital Non-DSP Solution**
- **Meets RCR STD-18**

## Applications

- **Wireless LAN/Modems**
- **Handy Data Terminals**
- **Low-Power Wireless Data Link for PCs, Laptops and Printers**
- **Point-Of-Sale Terminals**
- **Wireless Bar-Code Readers and Stock Controllers**

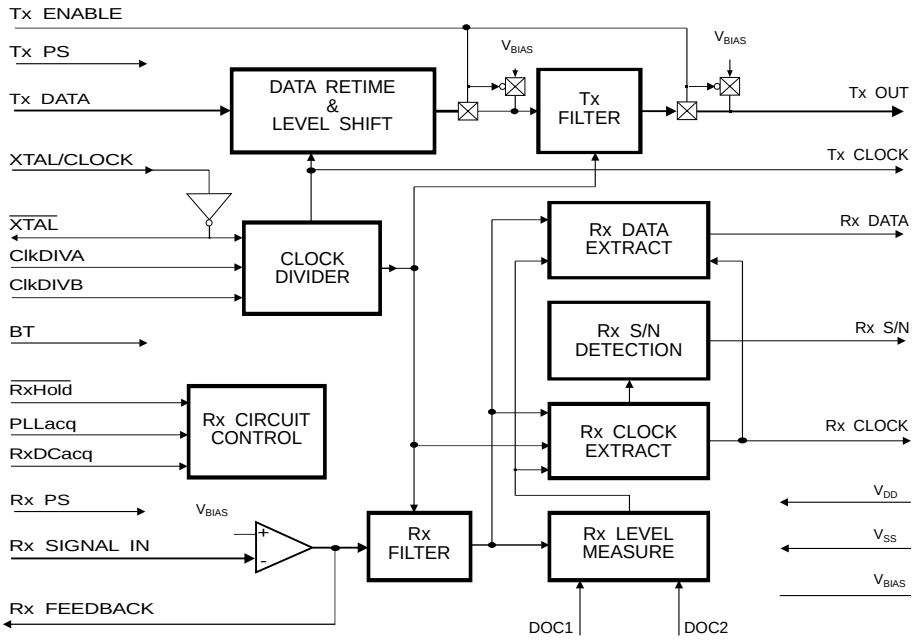



*Fig.1 Functional Block Diagram*

FX589

## Brief Description

The FX589 is a single-chip modem employing Gaussian Minimum Shift Keying (GMSK) modulation.

Data rates of 4kb/s to 64kb/s and the choice of BT to 0.3 or 0.5 are pin-programmable functions to suit radio data channel bandwidth requirements.

The Rx and Tx digital data interfaces are bit-serial and synchronised to Rx and Tx data clocks generated by the modem. Separate Rx and Tx Powersave/Enable inputs allow for full- or half-duplex operation.

Rx input levels can be set by a suitable ac and dc level adjusting circuit built, with external components, around an on-chip Rx input amplifier.

Acquisition, lock and hold of Rx data signals is made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the system µProcessor as required.

Indication is available, from the Rx S/N output, as to the quality of the received signal.

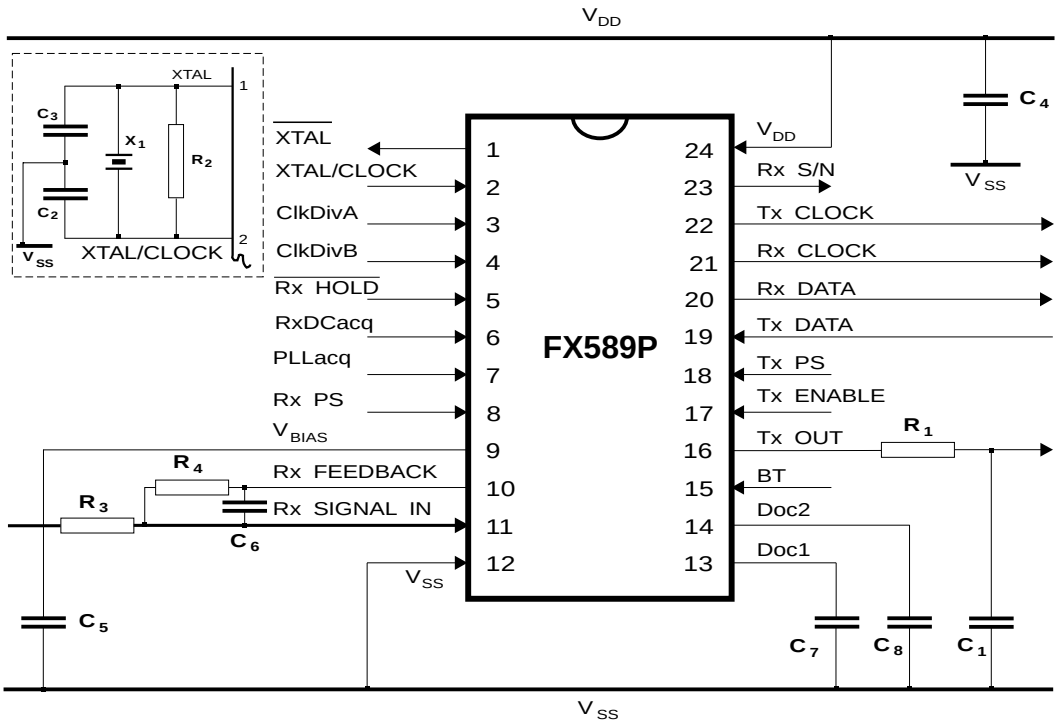
The FX589 design features a low-current analogue/digital ASIC process offering significantly lower current consumption than DSP technology. For data rates up to 32kb/s the FX589 draws typically 1.5mA at 3.0 volts $V_{DD}$ and for data rates up to 64kb/s at 5.0 volts, typically 4.0mA.

This low-power CMOS microcircuit is available in both 24-pin plastic DIL and Small Outline (SOIC and SSOP) packages.

| Pin Number<br>FX589DW<br>FX589D5<br>FX589P | Function |
|---|---|
| 1 | **$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator. |
| 2 | **Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock ($f_{XTAL}$) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{\text{Xtal}}$ pin left unconnected.<br>Note that operation of the FX589 without a suitable Xtal or clock input may cause device damage. |
| 3 | **ClkDivA:**<br>Two logic level inputs that control the internal clock divider and hence the transmit and receive data rate. See Table 1. |
| 4 | **ClkDivB:** |
| 5 | **$\overline{\text{Rx Hold}}$:** A logic “0” applied to this input will ‘freeze’ the Clock Extraction and Level Measurement circuits unless they are in ‘acquire’ mode. |
| 6 | **RXDCacq:** A logic “1” applied to this input will set the Rx Level Measurement circuitry to the ‘acquire’ mode. |
| 7 | **PLLacq:** A logic “1” applied to this input will set the Rx Clock Extraction circuitry to ‘acquire’ mode (see Table 2). |
| 8 | **Rx PS:** A logic “1” applied to this input will powersave all receive circuits except for “Rx Clock” output (which will continue at the set bit-rate) and cause the “Rx Data” and “Rx S/N” outputs to go to a logic “0”. |
| 9 | **$V_{BIAS}$:** The internal circuitry bias line, held at $V_{DD}/2$, this pin must be decoupled to $V_{SS}$ by a capacitor mounted close to the pin. |
| 10 | **Rx Feedback:** The output of the Rx Input Amplifier/the input to the Rx Filter. |
| 11 | **Rx Signal In:** The input to Rx Input Amplifier. |
| 12 | **$V_{SS}$:** Negative supply rail. Signal ground. |

| Pin Number<br>FX589DW<br>FX589D5<br>FX589P | Function |
|---|---|
| 13 | **Doc1:** Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to $V_{SS}$. See Figure 2. |
| 14 | **Doc2:** |
| 15 | **BT:** A logic level to select the modem 'BT' (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic "1" sets the modem to a BT of 0.5, a logic "0" to a BT of 0.3. |
| 16 | **Tx Out:** The Tx signal output from the FX589 GMSK Modem. |
| 17 | **Tx Enable:** A logic "1" applied to this input enables the transmit data path through the Tx Filter to the "Tx Out" pin. A logic "0" will put the "Tx Out" pin to $V_{BIAS}$ via a high impedance. |
| 18 | **Tx PS:** A logic "1" applied to this input will powersave all transmit circuits except for the "Tx Clock". |
| 19 | **Tx Data:** The logic level input for the data to be transmitted. This data should be synchronous with the "Tx Clock". |
| 20 | **Rx Data:** A logic level output carrying the received data, synchronous with the "Rx Clock". |
| 21 | **Rx Clock:** A logic level clock output at the received data bit-rate. |
| 22 | **Tx Clock:** A logic level clock output at the transmit-data rate. |
| 23 | **Rx S/N:** A logic level output which may be used as an indication of the quality of the received signal. |
| 24 | **$V_{DD}$:** Positive supply rail. A single, stable power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor mounted close to the pin. |

## Application Information




**External Components**

| Component | Value | Tolerance |
|---|---|---|
| $R_1$ | Note 1 | ±5% |
| $R_2$ | 1.0MΩ | ±10% |
| $R_3$ | Note 2 | ±10% |
| $R_4$ | 100kΩ | ±10% |
| $C_1$ | Note 1 | ±10% |
| $C_2$ | Note 5 | |
| $C_3$ | Note 5 | |
| $C_4$ | 100nF | ±20% |
| $C_5$ | 1.0µF | ±20% |
| $C_6$ | 22.0pF | ±20% |
| $C_7$ | Note 4 | |
| $C_8$ | Note 4 | |
| $X_1$ | Note 3 | |

*Fig.2 Recommended External Components*

**Notes**

1. The RC network formed by $R_1$ and $C_1$ is required between the Tx Out pin and the input to the modulator. This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering.
   The ground connection to the capacitor $C_1$ should be positioned to give maximum attenuation of high-frequency noise into the modulator.
   The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is: BT of 0.3 = 0.34/bit rate (bits/second)
   BT of 0.5 = 0.22/bit rate (bits/second).

| Data Rate | BT = 0.3 | | BT = 0.5 | |
|---|---|---|---|---|
| (b/s) | R1 (kΩ) | C1 (pF) | R1 (kΩ) | C1 (pF) |
| 4000 | 120 | 680 | 120 | 470 |
| 4800 | 100 | 680 | 100 | 470 |
| 8000 | 91 | 470 | 120 | 220 |
| 9600 | 91 | 390 | 47 | 470 |
| 16000 | 47 | 470 | 91 | 150 |
| 19200 | 100 | 180 | 91 | 120 |
| 32000 | 47 | 220 | 47 | 150 |
| 38400* | 47 | 180 | 47 | 120 |
| 64000* | 56 | 100 | 51 | 68 |

* $V_{DD}$ >= 4.5V

Note that in all cases, the value of $R_1$ should be not less than 47.0kΩ and that the calculated value of $C_1$ includes calculated parasitic (circuit) capacitances.

2. $R_3$, $R_4$ and $C_6$ form the gain components for the Rx Input signal. $R_3$ should be chosen as required by the signal input level.
3. The FX589 can operate correctly with Xtal/Clock frequencies of 1.0MHz to 8.2MHz ($V_{DD}$ = 5.0V) and 1.0MHz to 5.0MHz ($V_{DD}$ = 3.0V); see Table 1 for examples. Operation of this device without a Xtal or Clock input may cause device damage.
4. $C_7$ and $C_8$ should both be 15.0nF for a data rate of 8kb/s, and inversely proportional to the data rate for other data rates, e.g. 30.0nF at 4kb/s, 1.8nF at 64kb/s.
5. The value chosen for $C_2$ and $C_3$ (including stray capacitances) should be suitable for the applied $V_{DD}$ and the frequency of $X_1$.
   As a guide: $C_2 = C_3$ = 33.0pF at 1.0MHz falling to 18pF at the maximum frequency.
   At 3 volts, $C_2 = C_3$ = 33.0pF falling to 18pF at 5.0MHz.
   The equivalent series resistance of $X_1$ should be less than 2.0kΩ falling to 150Ω at the maximum frequency.
   Stray capacitance on the Xtal/clock circuit pins must be minimised.

## Application Information .....

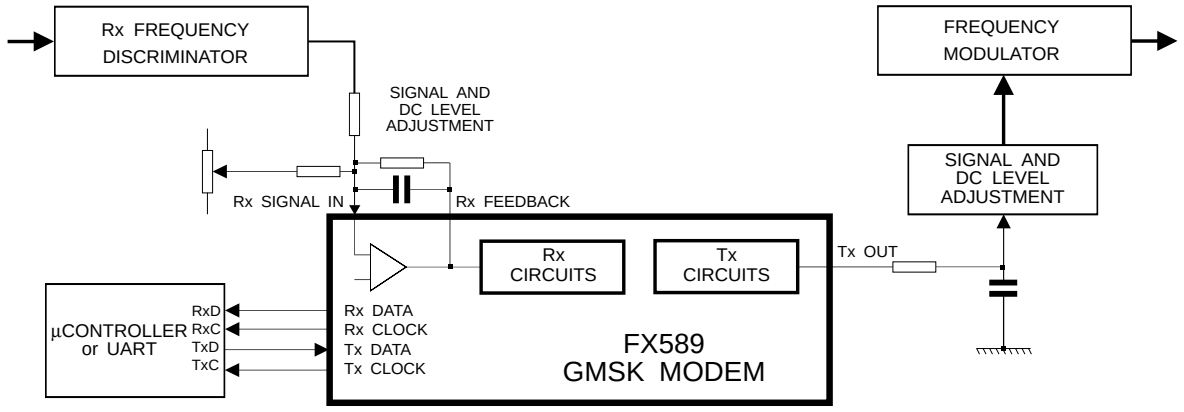



*Fig.3 External Signal Paths*

### Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz ($V_{DD}$ = 3.0V) or 1.0MHz to 8.2MHz ($V_{DD}$ = 5.0V) may be employed, depending upon the desired data rate.

A division ratio to facilitate data-rate setting is controlled by the logic level inputs on the ClkDivA/B pins, and is shown in Table 1 (below) - together with examples of how various 'standard' data-rates may be derived from common µP or Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (ClkDivA/B)}}$$

| ***Note*** *the device operation is not guaranteed above 64,000 bits/s or below 4,000 bits/s at the relevant supply voltage* | | | **Xtal/Clock Frequency (MHz)** | | | | |
|---|---|---|---|---|---|---|---|
| | | | 8.192 | 4.9152 | 4.096 [12.288/3] | 2.4576 [12.288/5] | 2.048 [6.144/3] |
| **Inputs** **ClkDiv A** | **Inputs** **ClkDiv B** | **Division Ratio: Xtal Freq / Data Rate** | **Data Rate (b/s)** | | | | |
| 0 | 0 | 128 | 64000* | 38400* | 32000 | 19200 | 16000 |
| 0 | 1 | 256 | 32000 | 19200 | 16000 | 9600 | 8000 |
| 1 | 0 | 512 | 16000 | 9600 | 8000 | 4800 | 4000 |
| 1 | 1 | 1024 | 8000 | 4800 | 4000 | | |

*Table 1 Clock/Data Rates* * $V_{DD}$ >= 4.5V

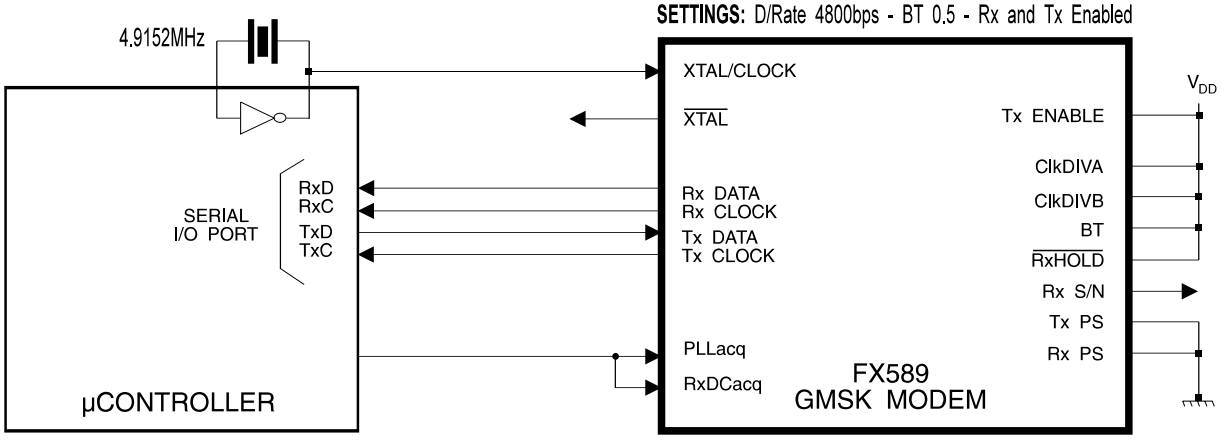



*Fig.4 Minimum µController System Connections*

# Application Information .....

## Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide dc level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the FX589's Rx Filter via a suitable gain and dc level adjusting circuit. This gain circuit can be built, with external components, around the on-chip Rx Input Amplifier, with the gain set so that the signal level at the Rx Feedback pin is nominally 1 Volt peak-to-peak (for $V_{DD}$ = 5.0 V) centred around $V_{BIAS}$ when receiving a continuous "1111000011110... " data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic "0" at the Rx Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors. One of which measures the amplitude of the 'positive' parts of the received signal; the other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage- 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum dc level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude, BT and any dc offset present.

## Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the 'PLLacq,' '$\overline{\text{Rx Hold}}$' and 'RxDCacq' pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram: In general, a data transmission will begin with a preamble of, for example, "1100110011001100," to allow the receive modem to establish timing -and level-lock- as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the 'RxDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The '$\overline{\text{Rx Hold}}$' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the '$\overline{\text{Rx Hold}}$' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RxDCacq' to a logic "1" for 10 to 20 bit periods.

'$\overline{\text{Rx Hold}}$' has no effect on the Level Measuring circuits while 'RxDCacq' is at a logic "1", and has no effect on the PLL while 'PLLacq' is at a logic "1".

A logic "0" on '$\overline{\text{Rx Hold}}$' does not disable the 'Rx Clock' output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

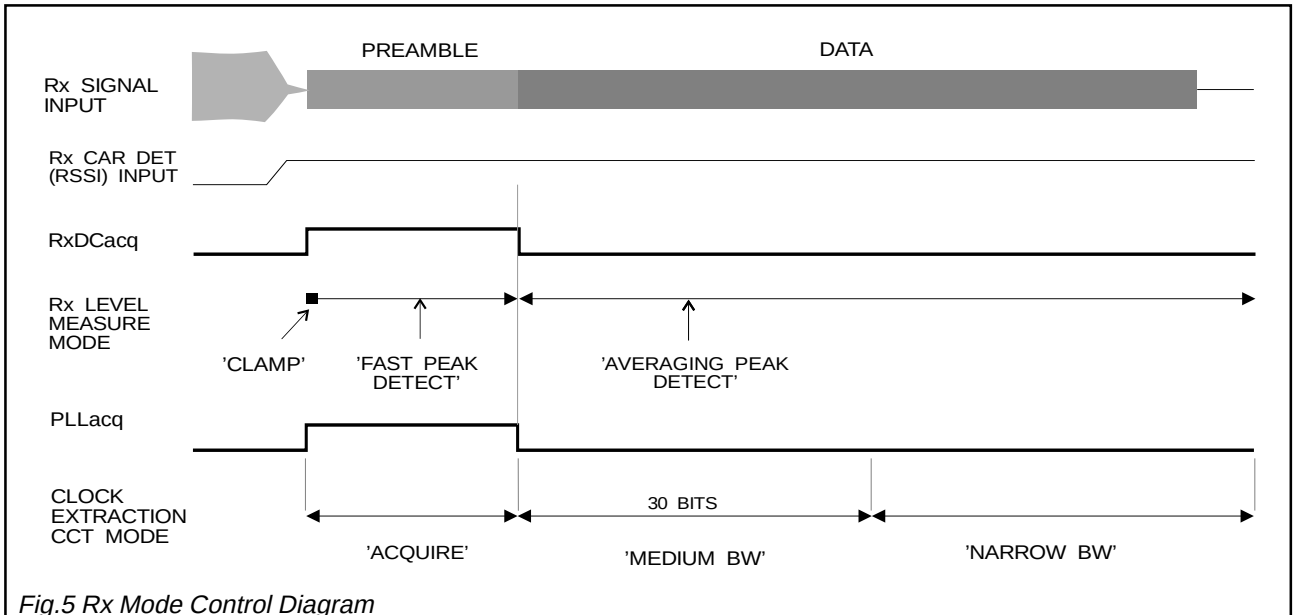



*Fig.5 Rx Mode Control Diagram*

## Application Information .....

| PLLacq | $\overline{\text{Rx Hold}}$ | PLL Action |
|---|---|---|
| "1" | X | **Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic "1". |
| "1" to "0" | "1" | **Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/16th bit-period for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the Rx Hold input is a logic "1". |
| "0" | "1" | **Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±1/64th bit-period for every two received zero-crossings. The PLL operates in this mode whenever the Rx Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation for instance). |
| "0" | "0" | **Hold:** The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods. |
| **RxDCacq** | **$\overline{\text{Rx Hold}}$** | **Rx Level Measure Action** |
| "0" to "1" | X | **Clamp:** Operates for one bit-time after a "0" to "1" transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid-way between the received signal input level and $V_{BIAS}$, with the charge time-constant being of the order of 0.5bit-time. |
| "1" | X | **Fast Peak Detect:** The voltage detectors act as peak-detectors, one capacitor is used to capture the 'positive'-going signal peaks of the Rx Filter output signal and the other capturing the 'negative'-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic "1," except for the initial 1-bit Clamp-mode time. |
| "0" | "1" | **Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes. |
| "0" | "0" | **Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000bits] towards $V_{BIAS}$). |

*Table 2 PLL and Rx Level Measurement Operational Modes* *X = don't care*

### Rx Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'Rx Clock Extraction' circuitry controls the 'Rx Clock' output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'Rx Circuit Control' inputs PLLacq and Rx Hold to operate in one of four PLL modes as described in Table 2.

### Rx Data Extraction

The 'Rx Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the Rx Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference depending on the chosen BT. The extracted data is output from the 'Rx Data' pin, and should be sampled externally on the rising edge of the 'Rx Clock.'

### Rx S/N Detection

The 'Rx S/N Detector' system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the 'Rx S/N' pin; a 'high' level indicates a series of GOOD crossings, a 'low' level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and hence the Bit-Error-Rate of the received signal.

## Application Information .....

### Bit Error Rate Performance

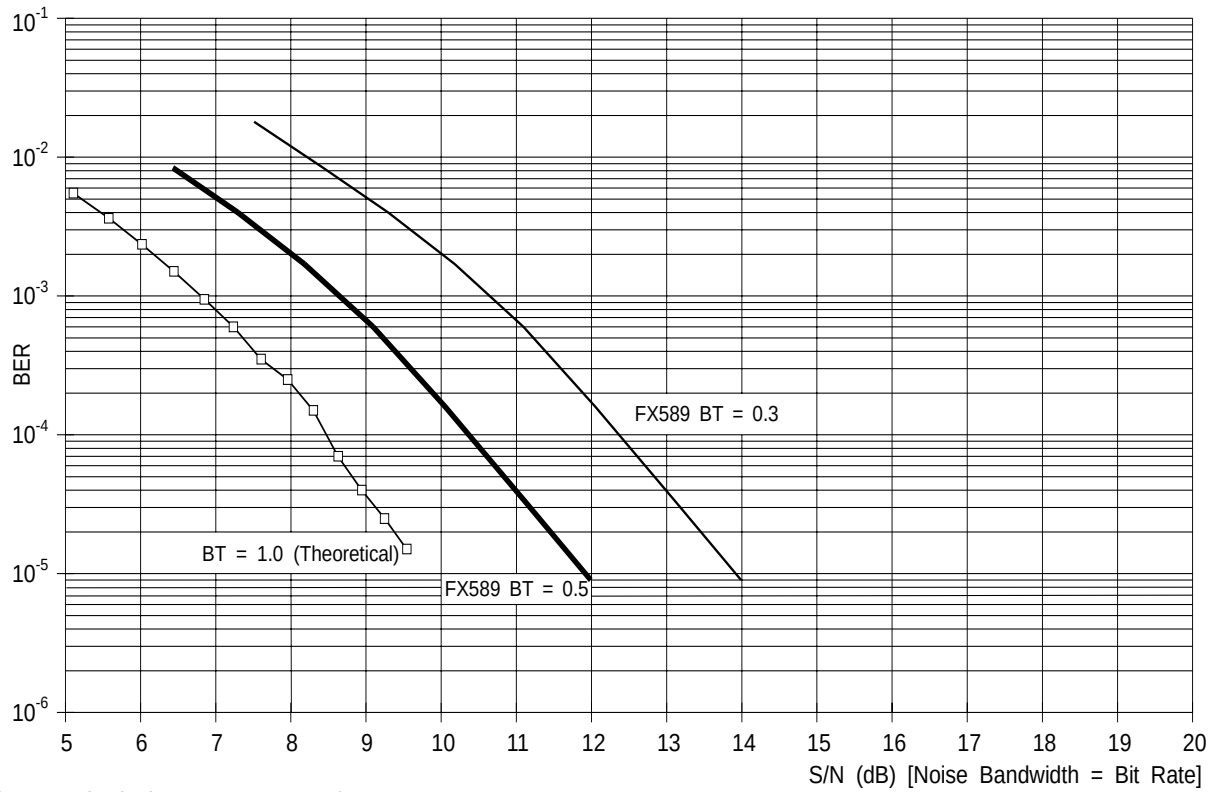



*Fig.6 Typical Bit-Error-Rate Performance*

### Rx Signal Quality

Figure 7 shows, diagrammatically, the effect of input Rx signal quality on the “Rx S/N” output.

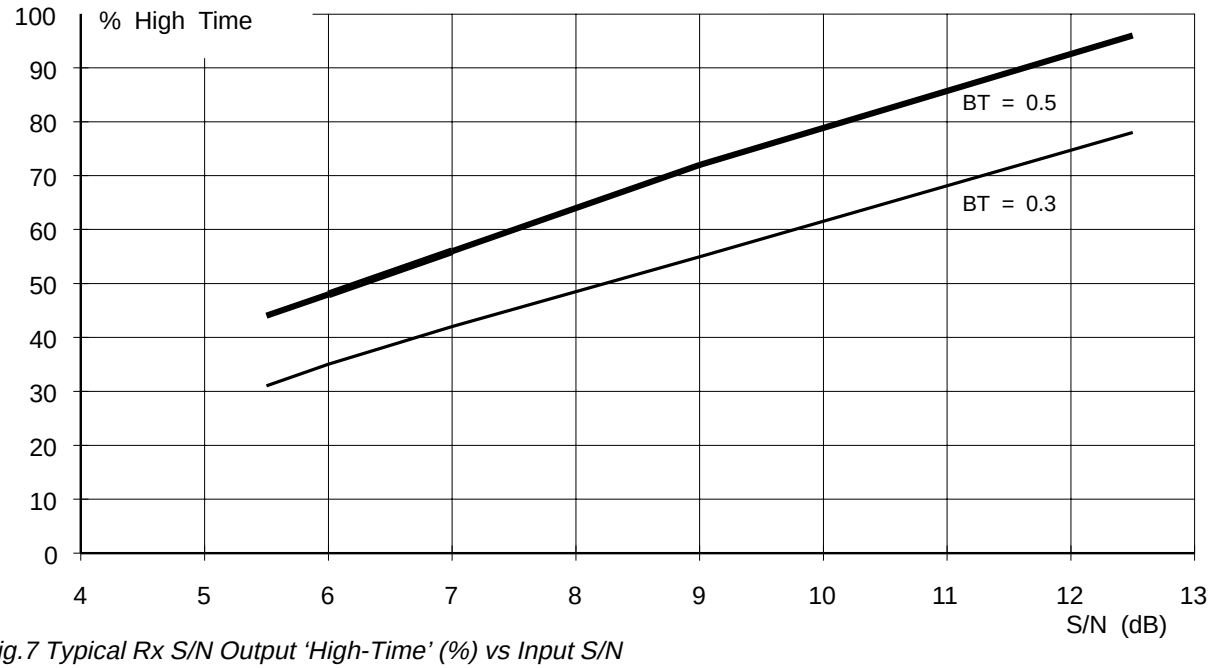



*Fig.7 Typical Rx S/N Output ‘High-Time’ (%) vs Input S/N*

# Application Information .....

## Tx Signal Path Description

The binary data applied to the 'Tx Data' input is re-timed within the chip on each rising edge of the 'Tx Clock' and then converted to a 1 Volt peak-to-peak binary signal centred about $V_{BIAS}$ (for $V_{DD}$ = 5.0 V).

If the 'Tx Enable' input is 'high,' then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the 'Tx Out' pin.

| Tx Enable | Tx Filter Input | Tx Out Pin |
|---|---|---|
| "1" (high) | $^{VDD}/_{5}$Volt p-p Data | Filtered Data |
| "0" (low) | $V_{BIAS}$ | $V_{BIAS}$ via 500kΩ |

A 'low' input to the 'Tx Enable' will connect the input of the Tx Filter to $V_{BIAS}$, and disconnect the 'Tx Out' pin from the filter, connecting it instead to $V_{BIAS}$ through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimise amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the FX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note that an external RC network is required between the 'Tx Out' pin and the input to the Frequency Modulator (see Figures 2 and 3). This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering, and the ground connection to the capacitor $C_1$ should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The signal at 'Tx Out' is centred around $V_{BIAS}$, going positive for logic "1" (high) level inputs to the 'Tx Data' input and negative for logic "0" (low) inputs.

When the transmit circuits are put into a 'powersave' mode (by a logic "1" to the 'Tx PS' pin) the output voltage of the Tx Filter will be undefined.

When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The 'Tx Enable' input can be used to prevent these abnormal voltages from appearing at the 'Tx Out' pin.

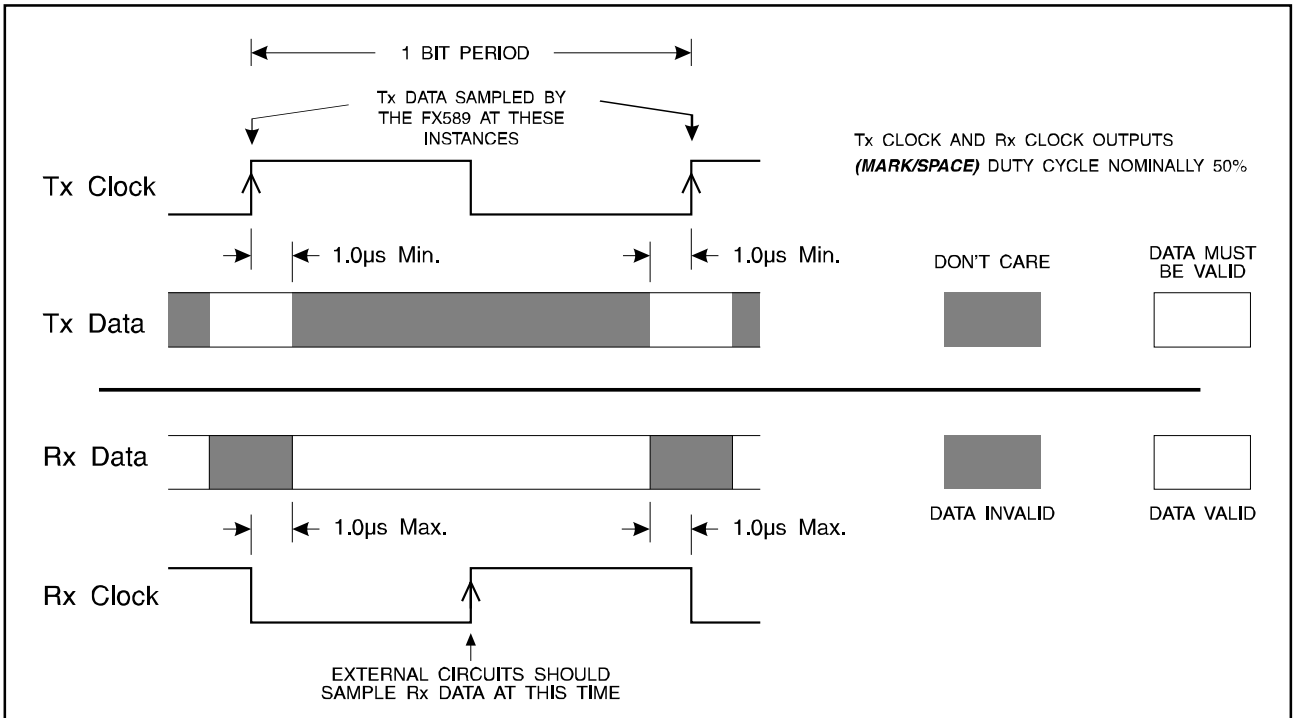



*Fig.8 Rx and Tx Clock Data Timings*

## Application Information .....

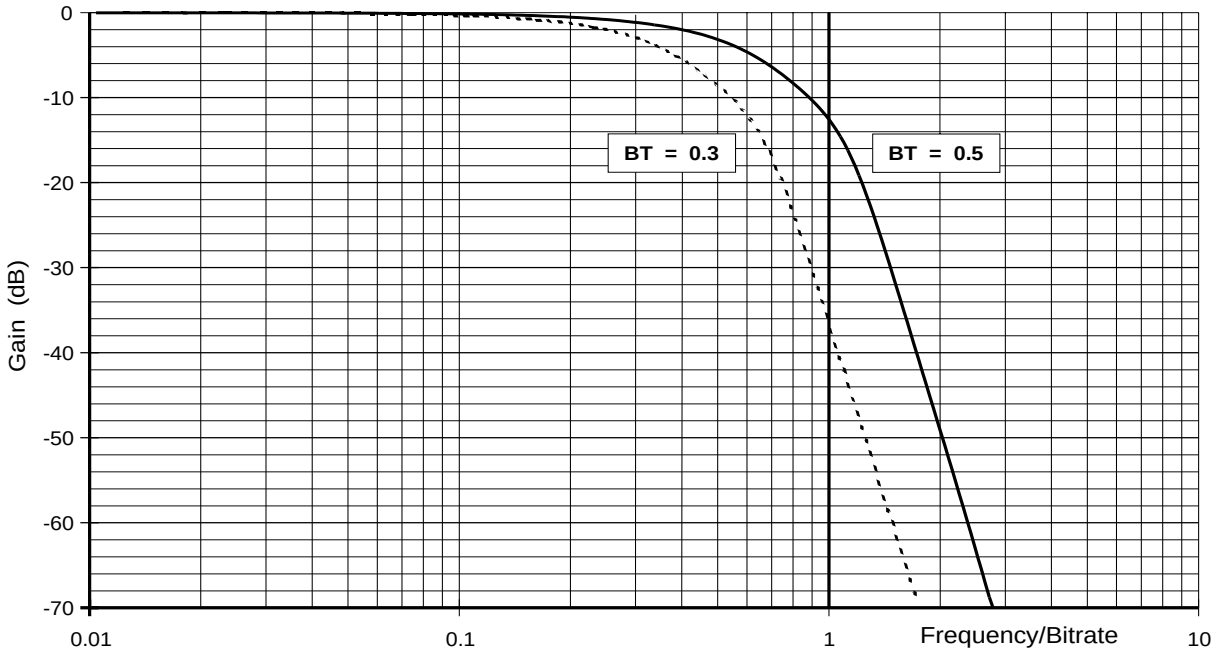



*Fig.9 Tx Filter Response*

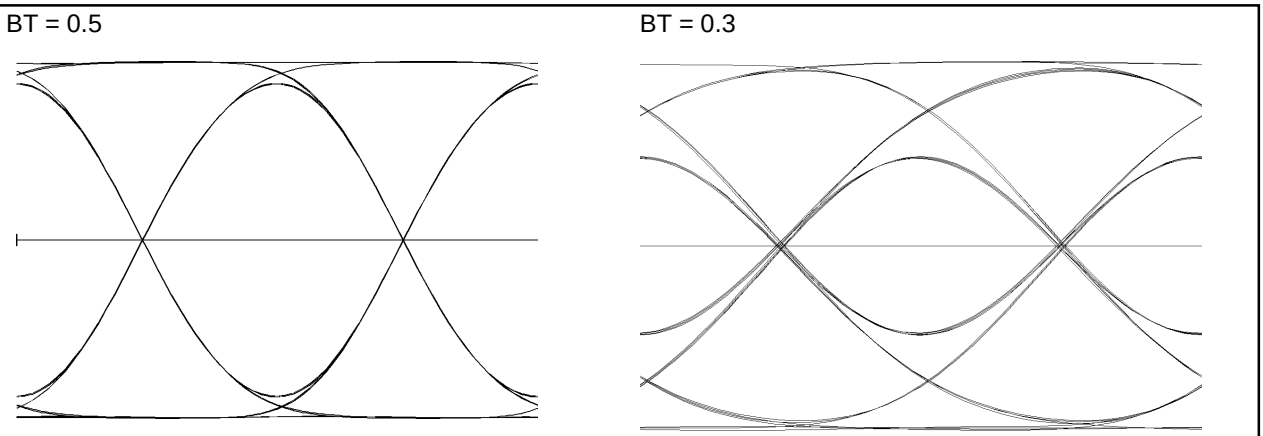



*Fig.10 Typical Transmit Eye Patterns*

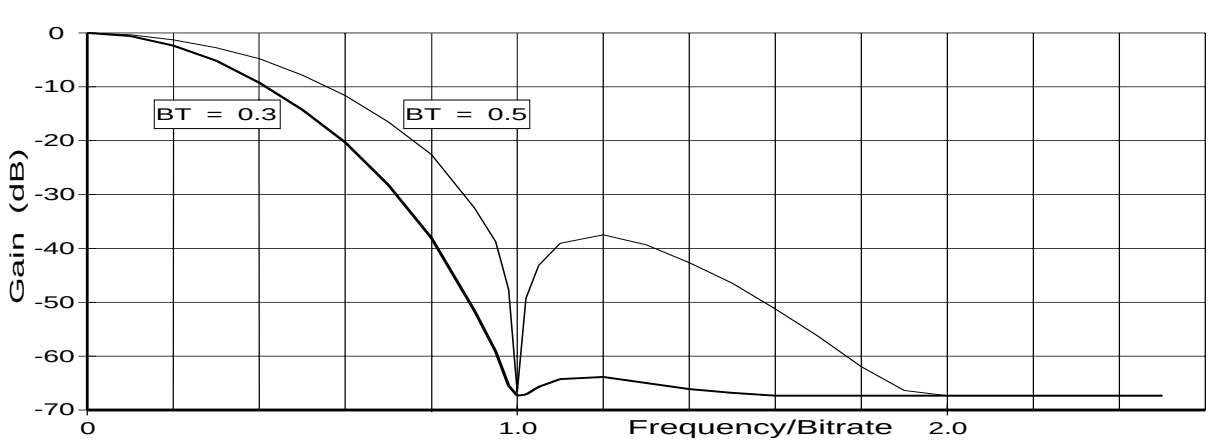



*Fig.11 Tx Output Spectrum (Random Data)*

# Application Information .....

## Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index will be required.

To achieve optimum channel utilization, (eg. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

## Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on:

- Channel spacing
- Allowable adjacent channel interference
- Tx filter bandwidth (BT)
- Peak carrier deviation (Modulation Index)
- Tx and Rx carrier frequency accuracies
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

As a guide, a raw data-rate of 8,000b/s at 12.5kHz channel spacing may be achievable -depending on local regulatory requirements- using a BT of 0.3 +/- 2kHz maximum deviation and no more than 1.5kHz discrepancy between Tx and Rx carrier frequencies. Forward Error Correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4,800b/s would allow the BT to be increased to 0.5, improving the error-rate performance.

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## FM Modulator, Demodulator and IF

For optimum performance, the ‘eye’ pattern of the received signal (when receiving random data) applied to the FX589 should be as close as possible to the Transmit ‘eye’ pattern examples shown in Figure 10.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few Hertz, two-point modulation being necessary for synthesised radios.
- Bandwidth and phase response of the Rx IF filters.
- Accuracy of the Tx and Rx carrier frequencies - any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be dc coupled to the FX589 ‘Rx Signal In’ pin (with a dc bias added to centre the signal at the Rx Feedback pin around $V_{DD}/2$ [$V_{BIAS}$] ), however ac coupling can be used provided that:

- The 3dB cut-off frequency for 8kb/s is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the FX589 to settle before the ‘RxDCacq’ line is strobed.

## Application Information .....

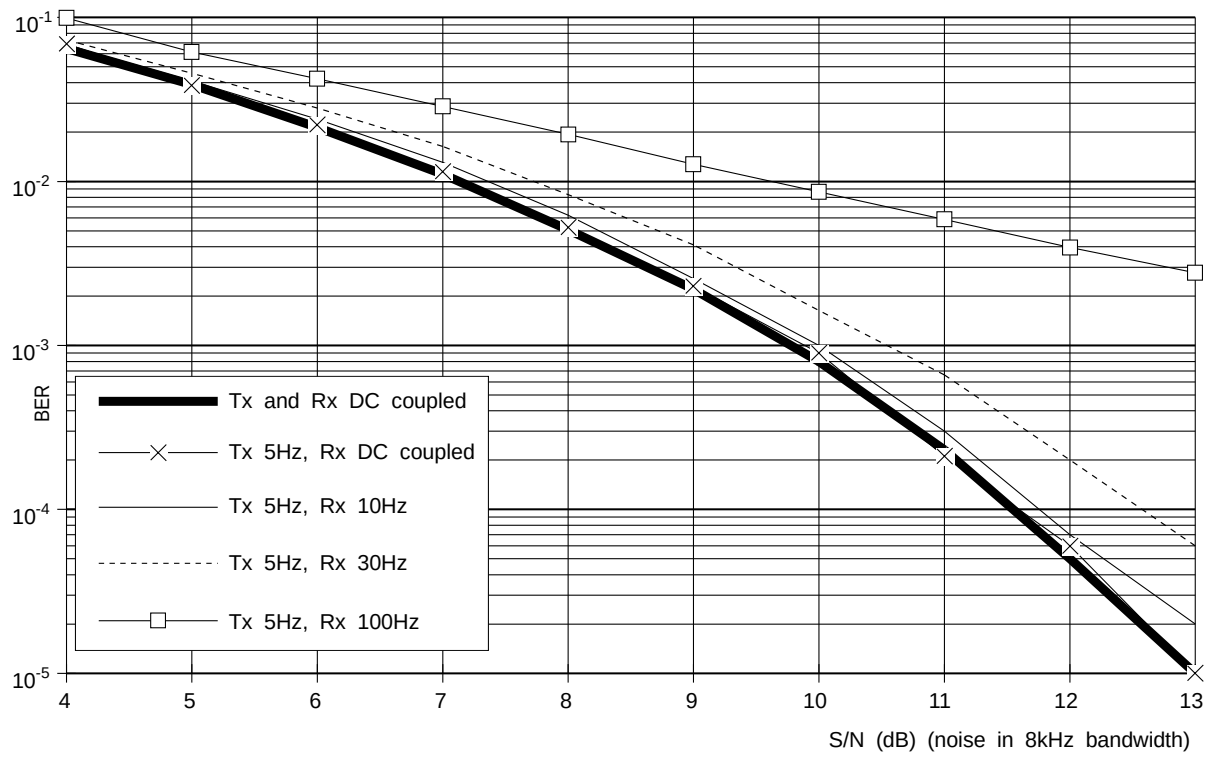



*Fig.12 Effect of AC Coupling on Typical Bit-Error Rate*

### AC Coupling of Rx and Tx Signals

In practical applications, it will usually be possible to arrange for any ac coupling between the FX589 Tx Output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but ac coupling between the receive discriminator and the input of the FX589 may need to have a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.
For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.0Hz in the Rx path.

The chart in Figure 12 (above) shows the typical static Bit-Error-Rate performance of the FX589 operating under nominal conditions for various degrees of ac coupling at the Rx Input and the Tx Output:

| | | |
|---|---|---|
| Data Rate | = | 8kb/s |
| $V_{DD}$ | = | 5.0V |
| Tamb | = | $25^{o}$C |
| Tx BT | = | 0.3 |

### Two Point Modulation

In a radio employing a frequency synthesiser, to prevent the radio's PLL circuitry counteracting the modulation process, and to provide a clean flat modulation response down to dc, it is recommended that a two-point modulation technique is employed when using the FX589.

Figure 13 shows a suggested basic configuration to provide a two-point modulation drive at 8kb/s from the FX589 Tx Output using the FX019 (a CML product) Digitally Controlled 'Quad' Amplifier Array.
The FX019 elements will provide individual setting-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the FX019 is via an 8-bit data word.

With reference to Figure 13:

The buffer amplifier is required to prevent loading of the FX589 external RC circuit.

Stage B, with $R_1/R_2$, provides suitable signal and dc levels for the VCO varactor; $C_1$ is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with $R_3/R_4$, provides the Reference Oscillator drive (application dependant). This parameter is set by adjusting for minimum ac signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D, with its attendant components, could be employed if a negative reference drive is required.

Stage A provides buffering and overall level control.

# Application Information .....

## Two Point Modulation .....

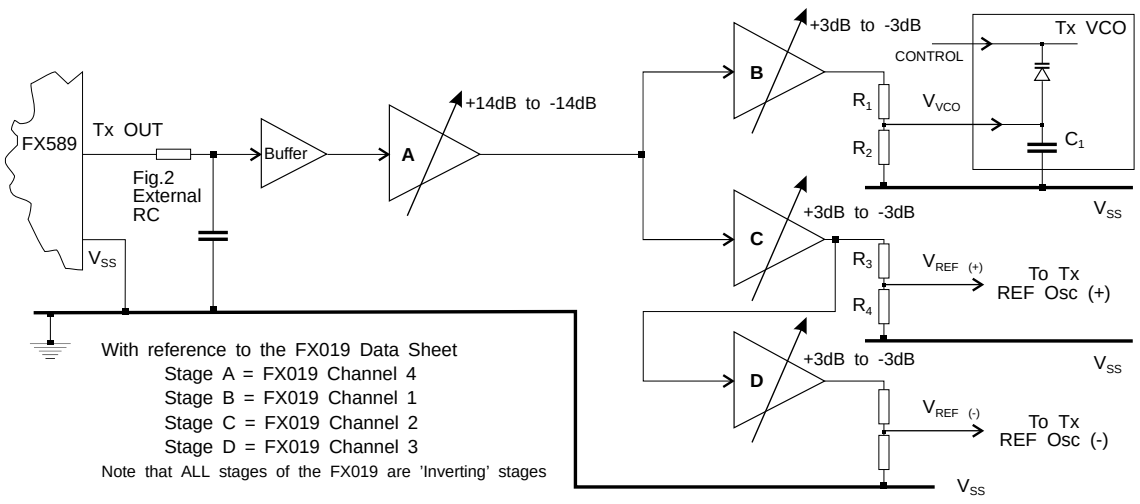



*Fig.13 An Example of Two-Point Modulation Drive with Individual Adjustment Using the FX019*

## Data Formats

The receive section of the FX589 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is scrambled in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should not be used.

## 'Acquisition' and 'Hold' Modes

The 'RxDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the dc measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a dc step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The FX589 can tolerate dc offsets in the received signal of at least +/- 0.5V with respect to $V_{BIAS}$, (measured at the Rx Feedback pin) however to ensure that the dc offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RxDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the FX589 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronisation.
To achieve this, the FX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more that about 0.1 bit time from the actual received data-rate during the time that the 'RxHold' input is 'Low'.

The 'RxDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.
Note however, that these pins are driven from very high-impedance circuits, so that the dc load presented by any external circuitry should exceed 10MΩ to $V_{BIAS}$.

# Specification

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

| | | |
|---|---|---|
| Supply voltage | | -0.3 to 7.0V |
| Input voltage at any pin (ref $V_{SS}$ = 0V) | | -0.3 to ($V_{DD}$ + 0.3V) |
| Sink/source current (supply pins) | | +/- 30mA |
| (other pins) | | +/- 20mA |
| Total device dissipation | (DW/P) @ $T_{AMB}$ 25°C | 800mW Max. |
| | (D5) @ $T_{AMB}$ 25°C | 550mW Max. |
| Derating | (DW/P) | 13mW/°C |
| | (D5) | 9mW/°C |
| Operating temperature range: | **FX589DW/D5/P** | -40°C to +85°C |
| Storage temperature range: | **FX589DW/D5/P** | -40°C to +85°C |

## Operating Limits

Correct operation of the device outside these limits is not implied.

| | Remarks | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | | 3.0 | 5.5 | V |
| Operating Temperature | | -40.0 | +85.0 | °C |
| Rx and Tx Data Rate | ($V_{DD} \geq 3.0V$) | 4,000 | 32,000 | bits/sec |
| | ($V_{DD} \geq 4.5V$) *Note 13 | 4,000 | 64,000 | bits/sec |
| Xtal/Clock Frequency | ($V_{DD} \geq 3.0V$) | 1.0 | 5.0 | MHz |
| | ($V_{DD} \geq 4.5V$) | 1.0 | 10.3 | MHz |
| "High" Pulse Width | Note 10 | 40.0 | | ns |
| "Low" Pulse Width | Note 10 | 40.0 | | ns |

## Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD}$ = 5.0V, $T_{AMB}$ = 25°C. Xtal/Clock Frequency = 4.096MHz. Data Rate = 8,000 bits/sec.
Noise Bandwidth = Bit Rate.

| Characteristics | | | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Static Values** | | | | | | | |
| Supply Current (($I_{DD}$) $V_{DD}$ = 3.0V) | **Tx PS** | **Rx PS** | 1 | | | | |
| | 1 | 1 | | - | 0.5 | - | mA |
| | 0 | 1 | | - | 1.0 | - | mA |
| | 1 | 0 | | - | 1.0 | - | mA |
| | 0 | 0 | | - | 1.5 | - | mA |
| (($I_{DD}$) $V_{DD}$ = 5.0V) | 1 | 1 | | - | 1.0 | - | mA |
| | 0 | 1 | | - | 2.0 | - | mA |
| | 1 | 0 | | - | 3.0 | - | mA |
| | 0 | 0 | | - | 4.0 | - | mA |
| Input Logic Levels | | | | | | | |
| Logic "1" | | | | 3.5 | - | - | V |
| Logic "0" | | | | - | - | 1.5 | V |
| Logic Input Current | | | 2 | -5.0 | - | 5.0 | µA |
| Logic "1" Output Level at IOH = -120µA | | | | 4.6 | - | - | V |
| Logic "0" Output Level at IOL = 120µA | | | | - | - | 0.4 | V |
| **Transmit Parameters** | | | | | | | |
| Tx OUT, Output Impedance | | | 3 | - | 1.0 | - | kΩ |
| Tx OUT, Level | | | 4, 11 | 0.8 | 1.0 | 1.2 | V p-p |
| Tx Data Delay (BT = 0.3) | | | 5 | - | 2.0 | 2.5 | bit-periods |
| (BT = 0.5) | | | 5 | - | 1.5 | 2.0 | bit-periods |
| Tx PS to Output-Stable Time | | | 6 | - | 4.0 | - | bit-periods |

## Specification .....

| Characteristics | See Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Receive Parameters** | | | | | |
| Rx Amplifier - | | | | | |
| Input Impedance | | 1.0 | - | - | MΩ |
| Output Impedance | 7 | - | 10.0 | - | kΩ |
| Voltage Gain | | - | 50.0 | - | dB |
| Rx Filter Signal Input Level | 8, 11 | 0.7 | 1.0 | 1.3 | V p-p |
| Rx Time Delay | 9 | - | - | 3.0 | bit-periods |
| **On-Chip Xtal Oscillator** | | | | | |
| $R_{IN}$ | | 10.0 | - | - | MΩ |
| $R_{OUT}$ | 12 | - | 50.0 | - | kΩ |
| Voltage Gain | 12 | - | 25.0 | - | dB |

**Notes**

1. Not including current drawn from the FX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For $V_{IN}$ in the range $V_{SS}$ to $V_{DD}$.
3. For a load of 10kΩ or greater. Tx PS input at logic “0”; Tx Enable = “1”.
4. Data pattern of “1111000011110000 ..”
5. Measured between the rising edge of ‘Tx Clock’ and the centre of the corresponding bit at ‘Tx Out.’
6. Time between the falling edge of ‘Tx PS’ and the ‘Tx Out’ voltage stabilising to normal output levels.
7. For a load of 10kΩ or greater. Rx PS input at logic “0”.
8. For optimum performance, measured at the ‘Rx Feedback’ pin for a “1111000011110000 ...” pattern.
9. Measured between the centre of bit at ‘Rx Signal In’ and corresponding rising edge of the ‘Rx Clock’.
10. Timing for an external clock input to the Xtal/Clock pin.
11. 'Typical' level shown is at $V_{DD}$ = 5.0V; actual levels are proportional to applied $V_{DD}$.
12. Small signal measurement at 1.0kHz with no load on $\overline{\text{Xtal}}$ output.
13. Data rate may be extended to 80kb/s at BT = 0.5 and $V_{DD}$ = 4.5 to 5.5 V only. In this case a 10.24MHz Xtal may be used, care must be taken with the external components.

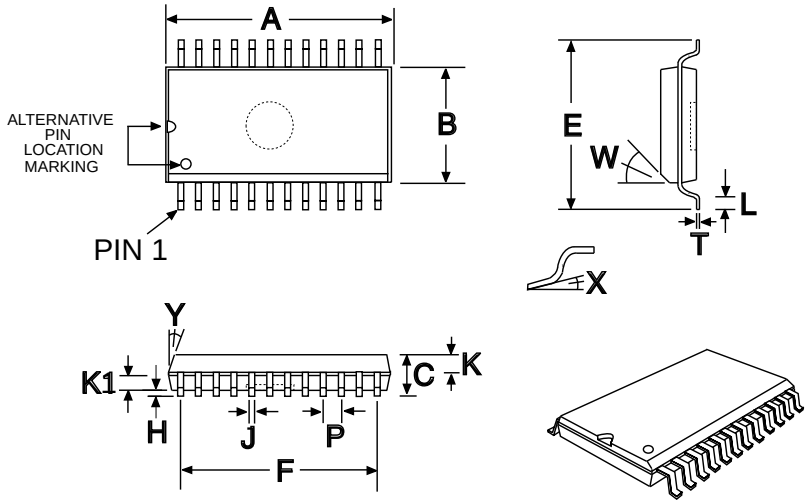
## Package Outlines

The FX589 is available in the package styles outlined below. Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

## Handling Precautions

The FX589 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

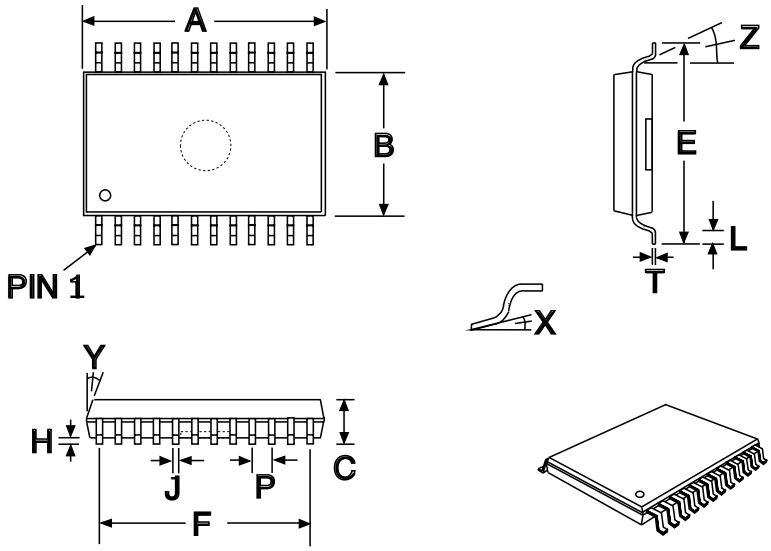
**FX589DW** 24-pin plastic S.O.I.C. (D2)




| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.597 (15.16) | | 0.613 (15.57) |
| B | 0.291 (7.39) | | 0.299 (7.59) |
| C | 0.093 (2.36) | | 0.105 (2.67) |
| E | 0.394 (10.01) | | 0.419 (10.64) |
| F | | 0.566 (14.37) | |
| H | 0.004 (0.10) | | 0.012 (0.30) |
| J | 0.014 (0.36) | | 0.018 (0.46) |
| K | 0.036 (0.91) | | 0.046 (1.17) |
| K1 | 0.036 (0.91) | | 0.046 (1.17) |
| L | 0.016 (0.41) | | 0.050 (1.27) |
| P | | 0.050 (1.27) | |
| T | 0.009 (0.23) | | 0.012 (0.30) |
| W | | 45° | |
| X | 0° | | 8° |
| Y | | 7° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

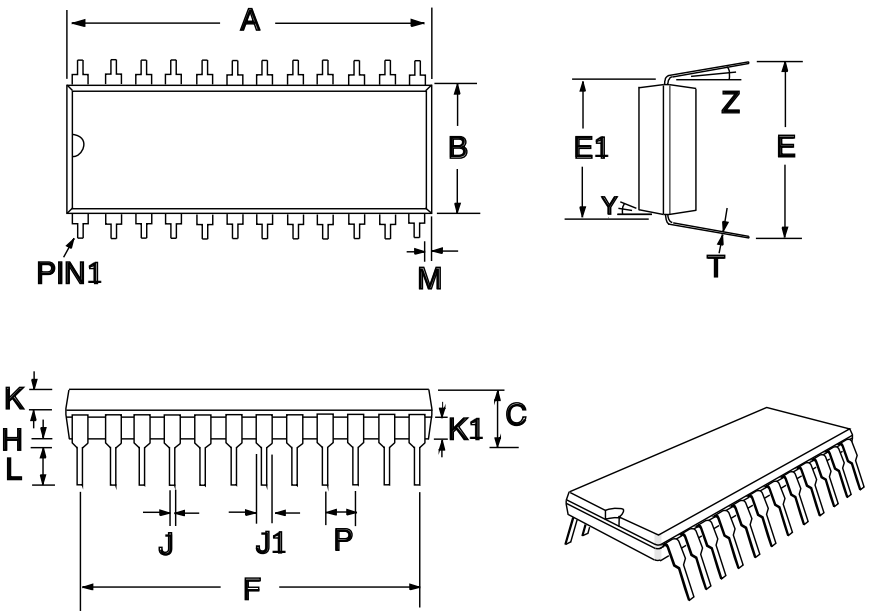
**FX589D5** 24-pin plastic S.S.O.P.




| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.318 (8.07) | | 0.328 (8.33) |
| B | 0.205 (5.20) | | 0.212 (5.38) |
| C | 0.068 (1.73) | | 0.078 (1.99) |
| E | 0.301 (7.65) | | 0.311 (7.90) |
| F | | 0.286 (7.15) | |
| H | 0.002 (0.05) | | 0.008 (0.21) |
| J | 0.010 (0.25) | | 0.015 (0.38) |
| L | 0.022 (0.55) | | 0.037 (0.95) |
| P | | 0.026 (0.65) | |
| T | 0.005 (0.13) | | 0.009 (0.22) |
| X | 0° | | 8° |
| Y | 7° | | 9° |
| Z | 4° | | 10° |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**FX589P** 24-pin plastic DIL (P4)




| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 1.200 (30.48) | | 1.270 (32.26) |
| B | 0.500 (12.70) | | 0.552 (14.02) |
| C | 0.151 (3.84) | | 0.220 (5.59) |
| E | 0.600 (15.24) | | 0.670 (17.02) |
| E1 | 0.590 (14.99) | | 0.625 (15.88) |
| F | | 1.10 (27.94) | |
| H | 0.015 (0.38) | | 0.045 (1.14) |
| J | 0.015 (0.38) | | 0.023 (0.58) |
| J1 | 0.040 (1.02) | | 0.065 (1.65) |
| K | 0.066 (1.68) | | 0.074 (1.88) |
| K1 | 0.060 (1.52) | | 0.074 (1.88) |
| L | 0.121 (3.07) | | 0.150 (3.81) |
| M | | 0.180 (4.58) | |
| P | | 0.100 (2.54) | |
| T | 0.008 (0.20) | | 0.015 (0.38) |
| Y | | 7° | |
| Z | | 4° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

## Ordering Information

**FX589DW** 24-pin plastic S.O.I.C. (D2)

**FX589D5** 24-pin plastic S.S.O.P.

**FX589P** 24-pin plastic DIL (P4)



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