

Pin Number

Function

DIL FX609J	Quad Plastic FX609LG	Quad Plastic FX609L2
1	1	1
	2	2
2	3	3
3	4	4
4	5	5
5	6	6
6	7	7
7	8	8
8	9	9
9	10	10
10	11	11
11	12	12
12	13	13
13	14	14
14	15	15
15	16	16
	17	17
16	18	18
17	19	19
18	20	20
19	21	21
20	22	22
21	23	23
22	24	24

Xtal/Clock: Input to the clock oscillator inverter. A nominal 1.024MHz xtal input or externally derived clock is injected here. See Fig. 2.

No connection.

Xtal: Output of clock oscillator inverter.

No Connection.

Encoder Data Clock: A Logic I/O port. External encode clock input or internal data clock output. Clock frequency dependent upon clock mode 1, 2 inputs and xtal frequency (see **Clock Mode** pins).

Encoder Output: The encoder digital output, this is a three state output:

Data Enable	Powersave	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	V _{SS}

No Connection.

Encoder Force Idle: When this pin is at logical '0' the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical '1' the encoder encodes as normal. Internal 1MΩ Pullup.

Data Enable: Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1MΩ Pullup.

No Connection.

Bias: Normally at V_{DD}/2 bias, this pin requires to be externally decoupled by a capacitor, C₂. Internally pulled to V_{SS} when "Powersave" is logical '0'.

Encoder Input: The analogue signal input. Internally biased at V_{DD}/2, an external 1μF input coupling capacitor, C₁, is required on this input. See Fig. 2 Note 3 for source impedance details.

V_{SS}: Negative Supply (GND).

No connection.

Decoder Output: The recovered analogue signal is output at this pin, it is the buffered output of a low pass filter. During "Powersave" this output is o/c.

No Connection.

Powersave: A logical '0' at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical '1' the codec operates normally. Internal 1MΩ Pullup.

No Connection.

Decoder Force Idle: A logical '0' at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to V_{DD}/2. When this pin is at a logical '1' the decoder operates as normal. Internal 1MΩ Pullup.

Decoder Input: Received digital signal input. Internal 1MΩ Pullup.

Decoder Data Clock: A Logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1, 2 inputs, see **Clock Mode** pins.

Algorithm: A logical '1' at this pin sets this device for a 3-bit companding algorithm. A logical '0' sets a 4-bit companding algorithm. Internal 1MΩ Pullup.

Clock Mode 2: These inputs select encoder and decoder data clock modes.

Clock Mode 1:

Internal
1MΩ pull-ups.

Clock	Mode	
1	2	
0	0	External Clocks
0	1	Internal, 64kb/s = f + 16
1	0	Internal, 32kb/s = f + 32
1	1	Internal, 16kb/s = f + 64

Clock rates refer to f = 1.024MHz Xtal/Clock input.

During Internal Data Clock operation the data clock frequencies are available at the ports for external circuit synchronisation. Independent or Common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

V_{DD}: Positive Supply: A single +5 volt power supply is required.

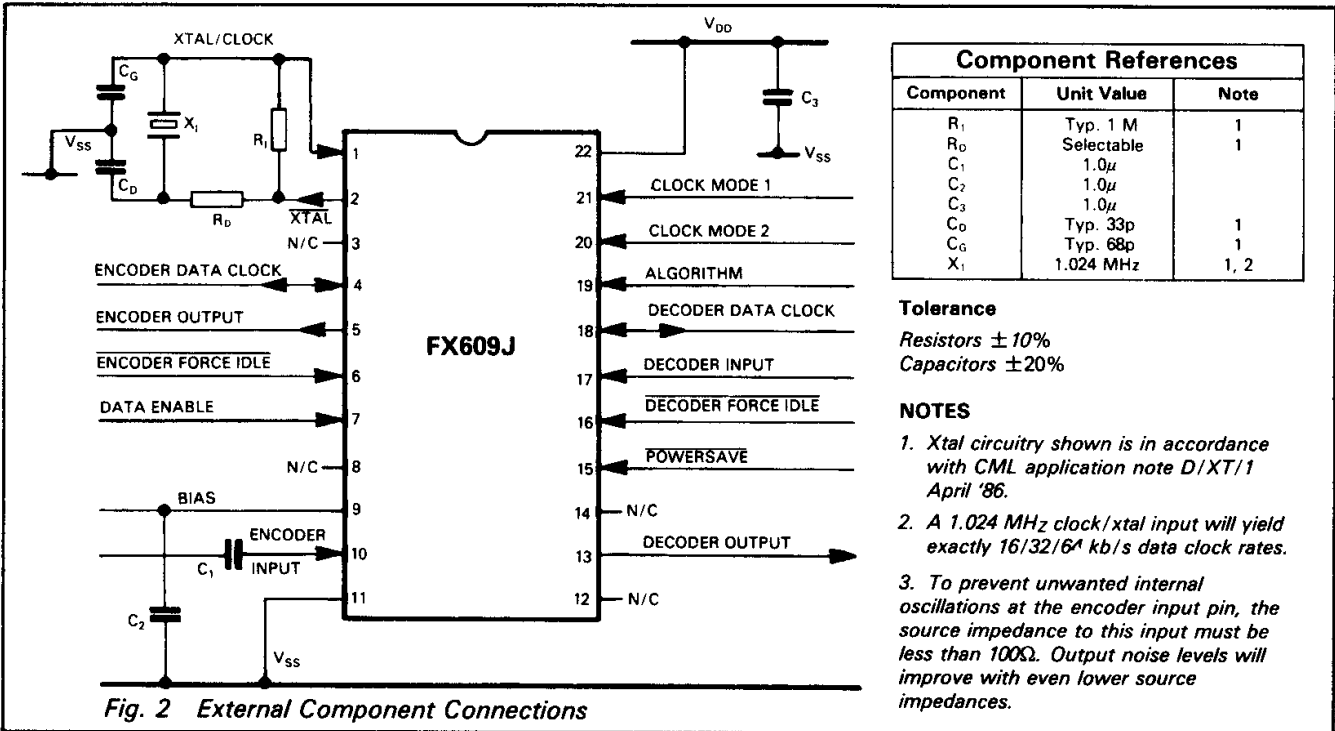


Fig. 2 External Component Connections

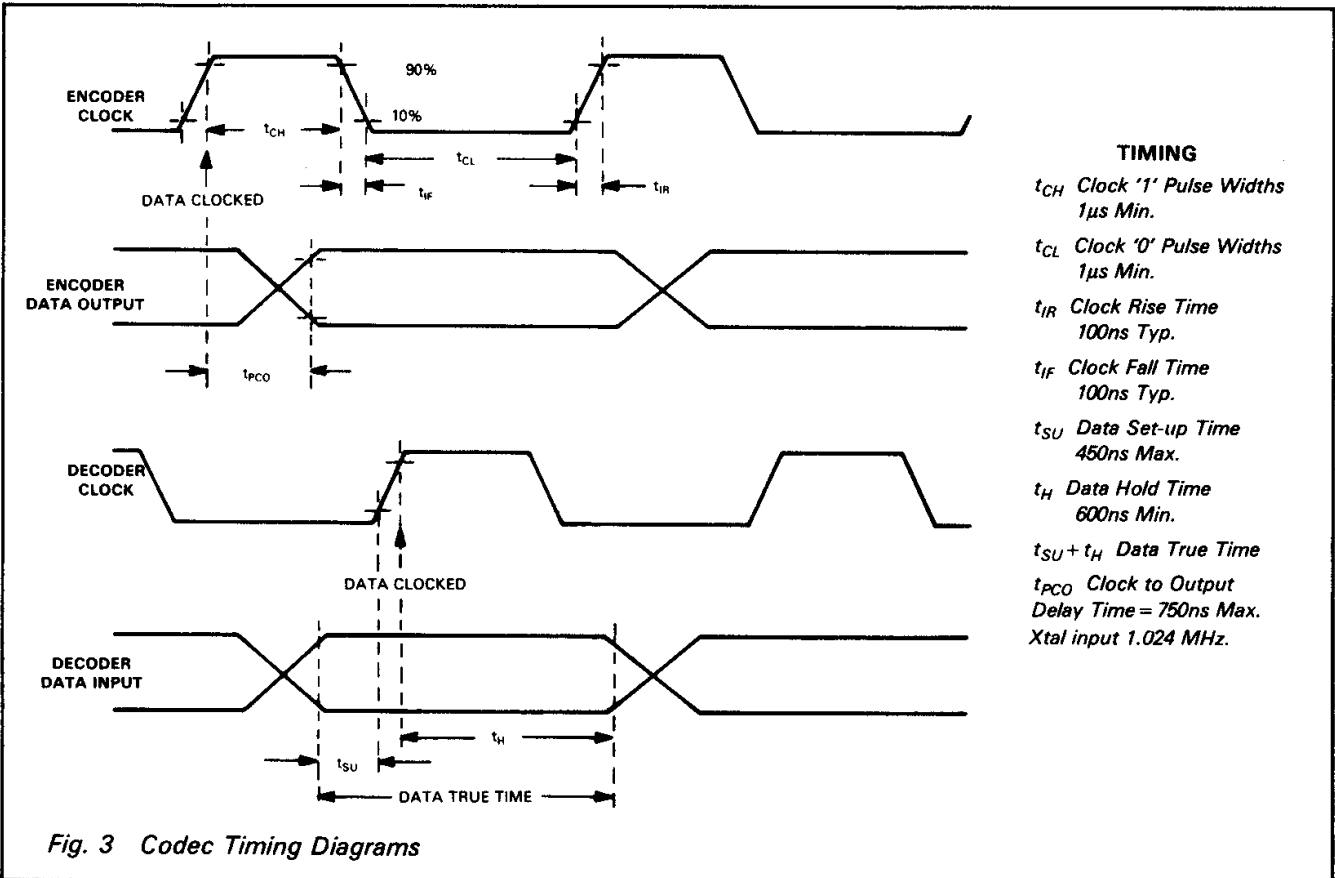


Fig. 3 Codec Timing Diagrams

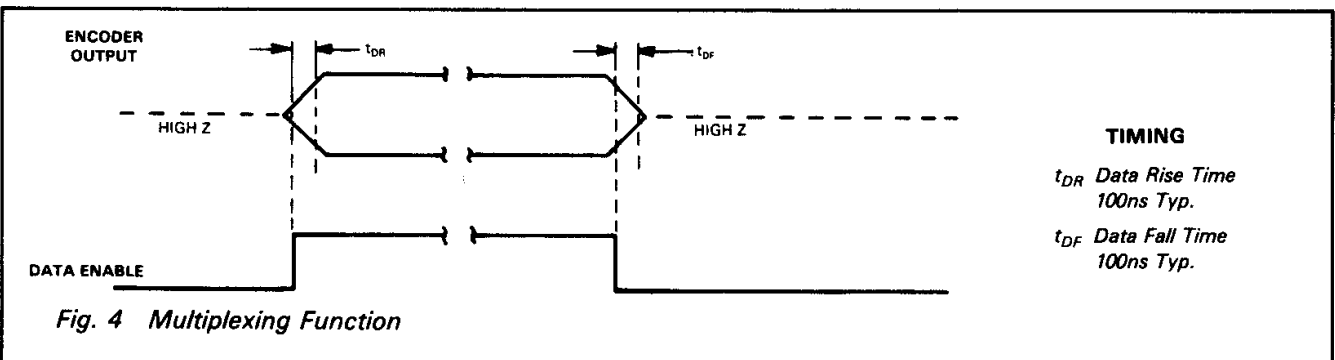


Fig. 4 Multiplexing Function

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3V to 7.0V
Input voltage at any pin (ref $V_{SS} = 0V$)		-0.3 to ($V_{DD} + 0.3V$)
Output sink/source current (supply pins)		$\pm 30mA$
(other pins)		$\pm 20mA$
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	FX609J	-30°C to +85°C (Ceramic)
	FX609LG/L2	-40°C to +85°C (Plastic)
Storage temperature range:	FX609J	-55°C to +125°C (Ceramic)
	FX609LG/L2	-40°C to +85°C (Plastic)

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:

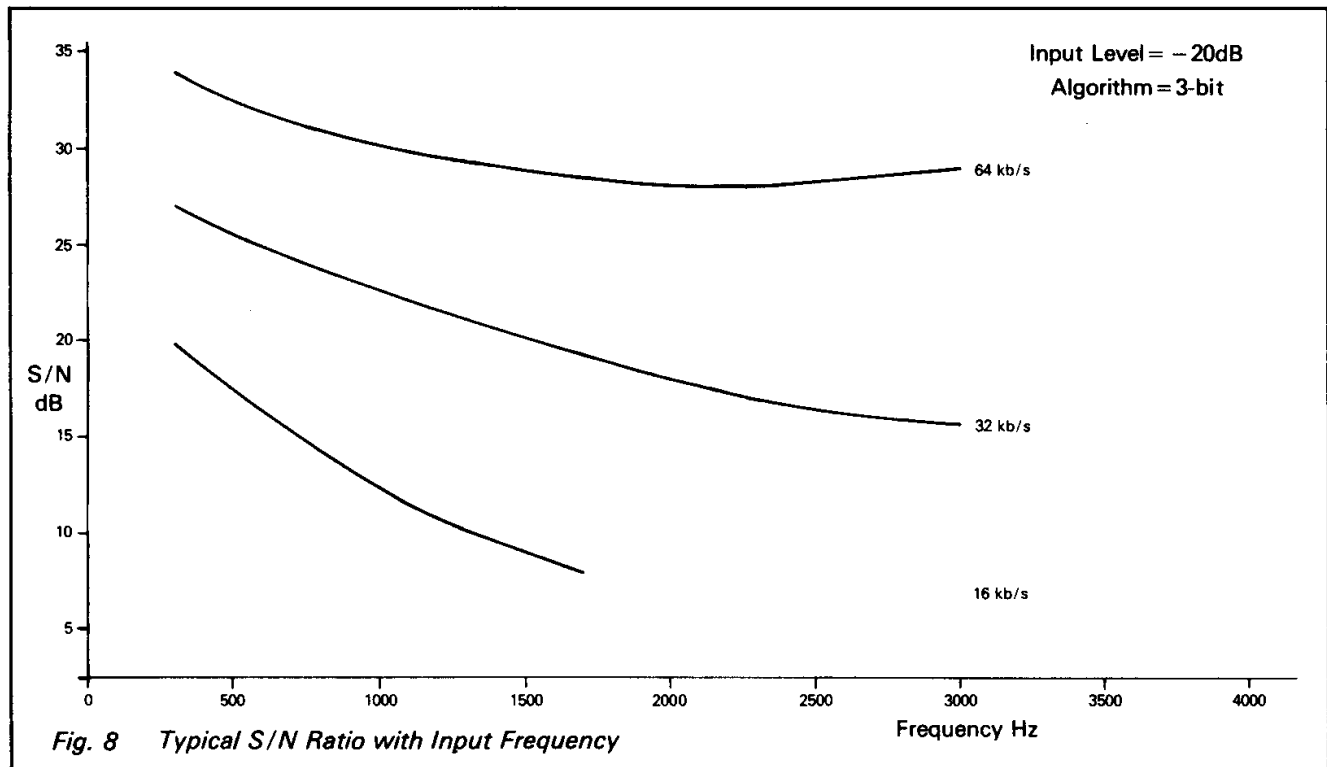
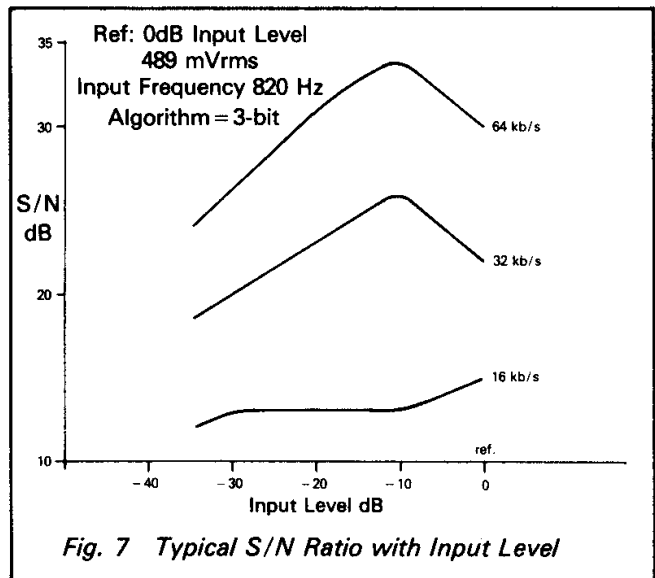
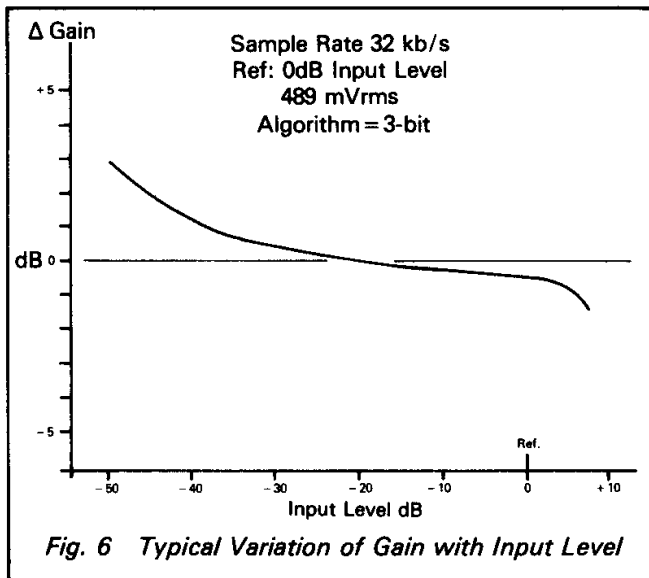
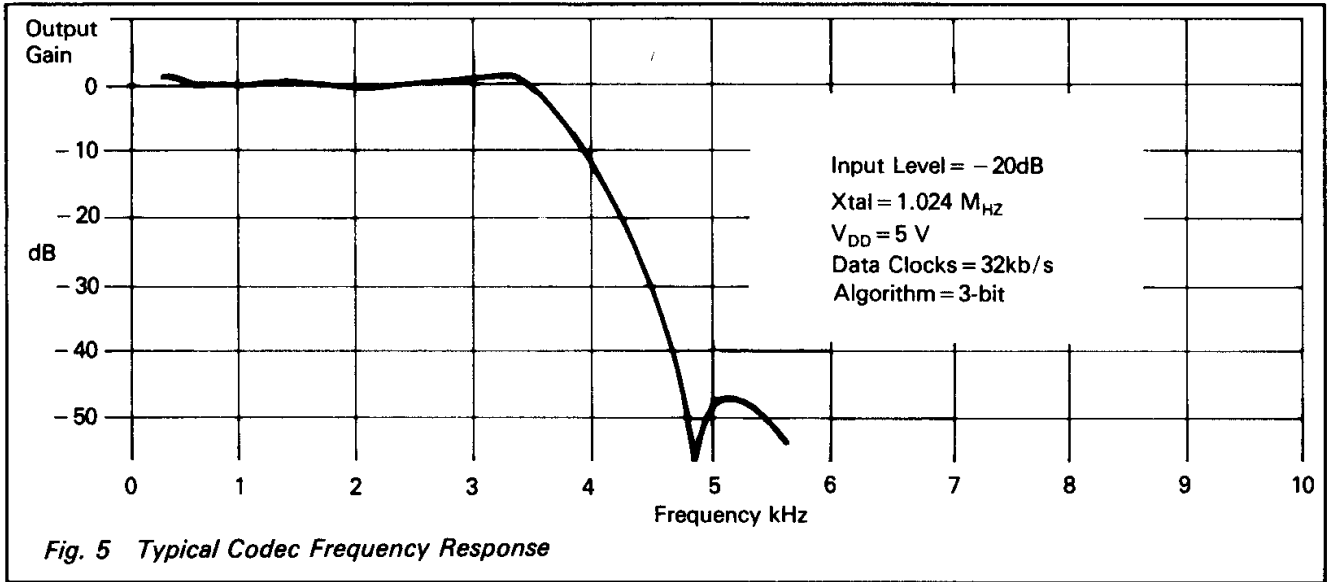
$V_{DD} = 5V$, $T_{amb} = 25°C$, Xtal/Clock (f) = 1.024 MHz, Sample Rate 32kb/s.

[Standard Test Signal 820Hz, ref. 0dB = 489mV (rms)]

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		—	3.5	—	mA
Supply Current (Powersave)		—	500	—	μA
Inputs Logic '1'		3.5	—	—	V
Inputs Logic '0'		—	—	1.5	V
Outputs Logic '1'		4.0	—	—	V
Outputs Logic '0'		—	—	1.0	V
Digital Input Impedance (logic I/O pins)		—	10	—	M Ω
Digital Input Impedance (logic input pins, pullup resistor)	2	300	—	—	k Ω
Digital Output Impedance		—	4	—	k Ω
Analogue Input Impedance		—	100	—	k Ω
Analogue Output Impedance		—	800	—	Ω
Three State Output leakage Current (output disabled)		—	± 4	—	μA
Insertion Loss		—	0	—	dB
Dynamic Values					
Encoder:					
Analogue Signal Input levels	5	-30	—	+8	dB
Principal Integrator Frequency		—	275	—	Hz
Encoder Passband		—	3400	—	Hz
Comand Time Constant		—	4	—	ms
Decoder:					
Analogue Signal Output levels	5	-30	—	+8	dB
Decoder Passband		300	—	3400	Hz
Encoder Decoder (Full codec):					
Passband		300	—	3400	Hz
Stopband		6	—	10	kHz
Stopband Attenuation		—	60	—	dB
Passband Gain		—	0	—	dB
Passband Ripple		-3	—	+3	dB
Output Noise (Input short circuit)		—	-60	—	dB
Perfect Idle Channel Noise (Encode Forced)		—	-63	—	dB
Group Delay Distortion	3	—	—	—	ms
1000 – 2600Hz		—	—	450	μs
600 – 2800Hz		—	—	750	μs
500 – 3000Hz		—	—	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

- Notes:**
1. Dynamic characteristics specified at 5V only.
 2. All logic Inputs except, Encoder and Decoder Data Clocks.
 3. Group delay distortion for full codec relative to the delay at 820Hz, -20dB at the encoder input.
 4. Relative timings are shown on Figures 3 and 4.
 5. Recommended values—see graph Fig. 7.

Codec Performance



Package Outlines

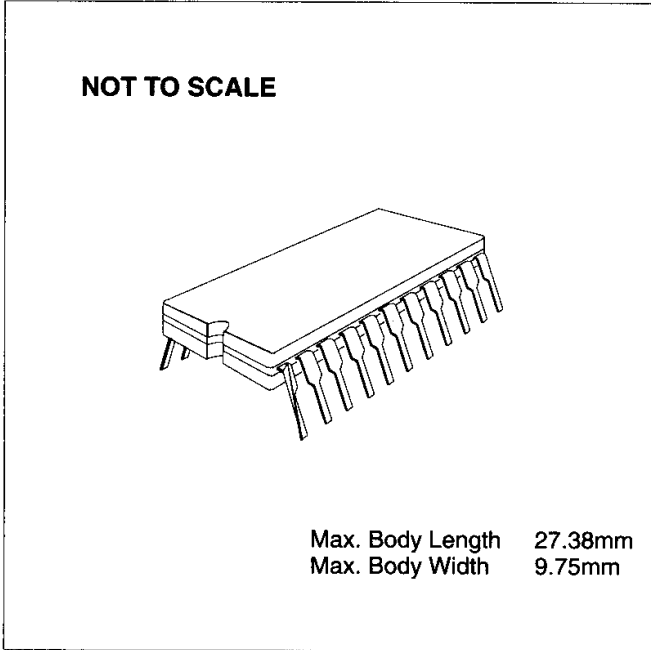
The FX609 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.

Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

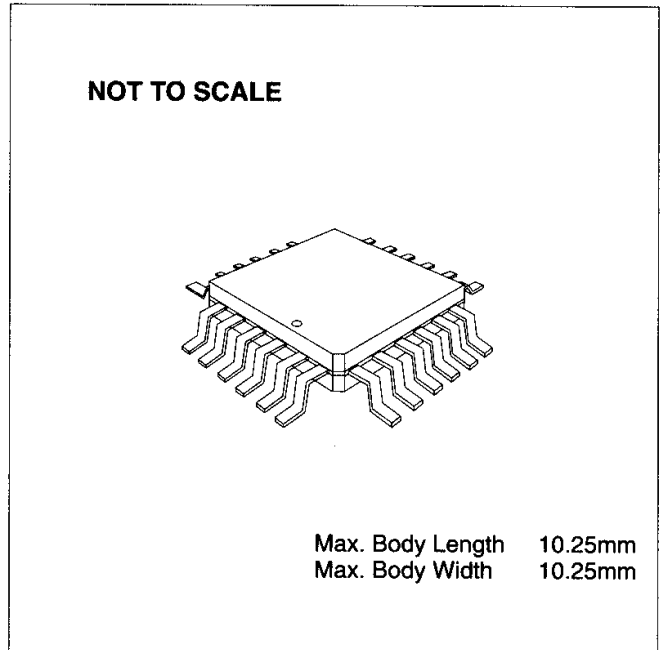
Handling Precautions

The FX609 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

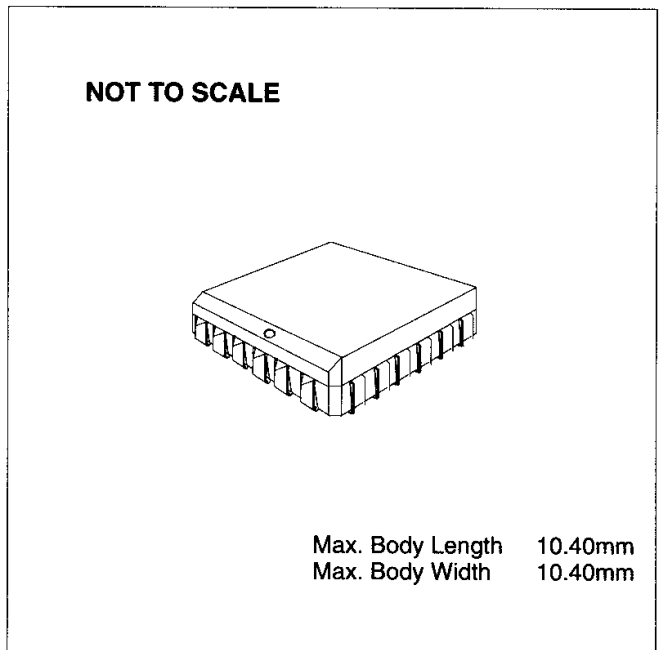
FX609J 22-pin cerdip DIL (J3)



FX609LG 24-pin quad plastic encapsulated bent and cropped (L1)



FX609L2 24-lead plastic leaded chip carrier (LS)



Ordering Information

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