CML Semiconductor Products

PRODUCT INFORMATION

FX621 Low-Power Subscriber Private Metering (SPM) Detector

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Provisional Issue

Features/Applications

- **Meets 12kHz and 16kHz SPM Specifications**
- **Low-Power CMOS [3.5 – 5 Volt Operation]**
- **Tone Follower and SPM Packet Detection Modes**
- **Adjustable Input Gain**
- **PABX, Payphone and Telephone Applications**
- **General-Purpose Tone Detection**
- **Crystal Oscillator Stability**

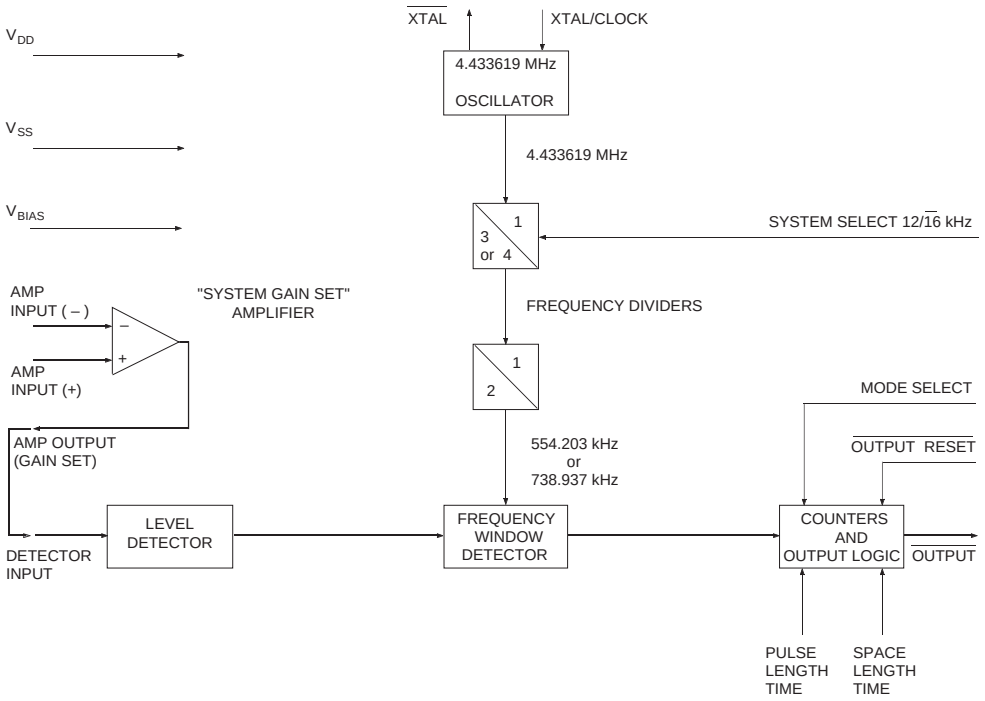


Fig.1 Internal Block Diagram

FX621

Brief Description

The FX621 is a single-chip, low-power CMOS tone detector designed for use in both PABX and general payphone applications for Subscriber Private Metering.

The Decode and Not-Decode band edges are accurately defined by the use of an external 4.433619MHz crystal.

Operation to either of the 12kHz or 16kHz SPM systems is pin programmable, with system amplitude sensitivities and pulse-length timing being provided by the use of external components.

The FX621 has 2 pin-selectable modes of operation:

1) *Tone Follower Mode.*
   A logic “0” is output whenever a tone of the correct frequency and length is detected.
2) *SPM Packet Mode.*
   An output is obtained only when both the mark and space timing criteria of an input SPM tone have been fulfilled.

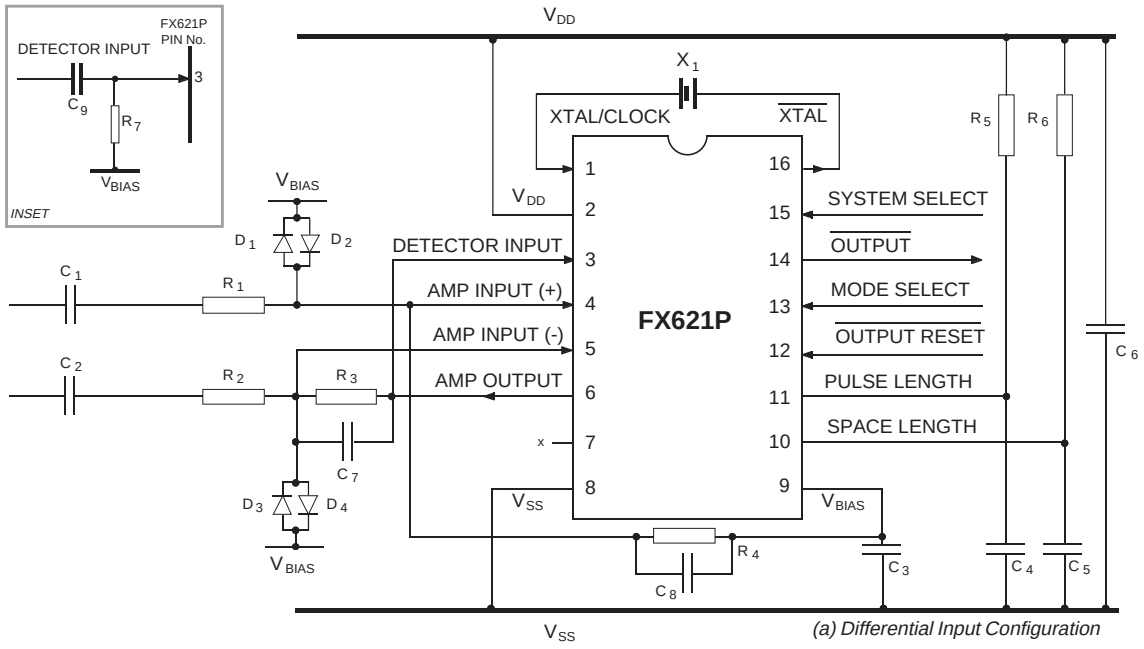
The FX621, which is available in plastic DIL and SMD packages, requires only a single 3.5-volt (min.) power supply, a 4.433619MHz crystal with external gain and timing components to meet most SPM specifications.

Pin Number Function

DIL FX621P	Quad FX621LG/LS	
1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A single 4.433619MHz Xtal or external clock pulse input is required (see Figure 2).
2	2	**V_{DD}:** The positive supply rail. A single, stable supply in the range 3.5V to 5V is required.
3	5	**Detector Input:** "Schmitt Trigger" level detector circuitry whose input thresholds are set internally and dependent on the applied V_{DD}. For use with low signal-level systems this input should be preceded by the "System Gain Set" amplifier. To use this input without the "System Gain Set" amplifier, the components indicated in Figure 2 (inset) should be used with the protection diodes (D_1 - D_4).
4	6	**Amplifier Input (+):** The positive and negative inputs to the "System Gain Set" Amplifier. With single or differential inputs this amplifier and its external circuitry can be used to provide the extra gain required to set the device to the user's National Level Specification. External diodes are used at both inputs (if in use) to provide protection when the line input level exceeds the supply rails (above the Absolute Maximum Rating).
5	7	**Amplifier Input (–):** If this device is used without this amplifier, the protection diodes should be employed at the Detector Input. See Figure 2.
6	8	**Amplifier Output:** The output of the "System Gain Set" Amplifier, is used with gain setting components. See Figures 1 and 2.
8	12	**V_{SS}:** The negative supply rail, (GND).
9	13	**V_{BIAS}:** The internal analogue bias pin, this point is at $V_{DD}/2$ and requires to be externally decoupled to V_{SS} via capacitor C_3.
10	14	**Space Length Time:** Active only in the 'SPM Packet' mode, this input, with an external RC network, sets the minimum valid No-Tone (Space) period for the incoming packet using the formula: $t_S = 0.7 (R_6 \times C_5)$. If the 'SPM Packet' mode is not required these timing components may be omitted. See Page 4.
11	17	**Pulse Length Time:** Active only in the 'SPM Packet' mode, this input, with an external RC network, sets the minimum valid Tone period for the incoming packet using the formula: $t_M = 0.7 (R_5 \times C_4)$. If the 'SPM Packet' mode is not required these timing components may be omitted. See Page 4.
12	18	**$\overline{\text{Output Reset}}$:** This input is used only in the 'SPM Packet' mode. Once an SPM packet has been detected and an output generated (logic "0") from this device the output remains as set until this input is strobed to a logic "0." See Figure 3. This input has an internal 1MΩ pullup resistor.
13	19	**Mode Select:** A control pin to select either the 'Tone Follower' mode or the 'SPM Packet' mode. A logic "1" selects 'Tone Follower', a logic "0" selects 'SPM Packet.' This input has an internal 1MΩ pullup resistor (Tone Follower).
14	20	**$\overline{\text{Output}}$:** The digital output of the SPM Detector. In the 'Tone Follower' mode a valid tone gives a logic "0" and no-tone gives a logic "1." Tonebursts and tone dropouts of less than 16 cycles are ignored. In the 'SPM Packet' mode the output is set to a logic "0" when a valid 'packet' is measured. The output remains as set until reset by a logic "0" at the Output Reset function, see Figure 3.
15	23	**System Select:** A control pin to set the device to work on either a 12kHz (logic "1") or 16kHz (logic "0") SPM system. This input has an internal 1MΩ pullup resistor (12kHz).
16	24	**$\overline{\text{Xtal}}$:** The output of the clock oscillator inverter, see Figure 2.
7	3, 4, 9, 10, 11, 15, 16, 21, 22.	No internal connection – leave open circuit.

Application Information

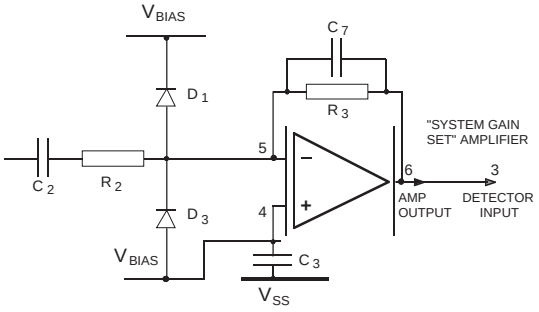
The notes on these pages are intended to assist in calculating the external components required to operate the FX621 as an SPM Detector.



(a) Differential Input Configuration

Component References

Component	Reference	Component	Reference
R_1	Note 4	C_1	Note 4
R_2	Note 4	C_2	Note 4
R_3	390kΩ ± 1.0%	C_3	1.0µF ± 20%
R_4	390kΩ ± 1.0%	C_4	Note 5
R_5	Note 5	C_5	Note 5
R_6	Note 5	C_6	1.0µF ± 20%
R_7	1.0MΩ	C_7	12.0pF ± 10.0%
D_1 to D_4	1N4148 or equivalent (small signal type)	C_8	12.0pF ± 10.0%
		C_9	0.1µF ± 10.0%
X_1	4.433619MHz		



(b) Single Input Configuration

Fig.2 Recommended External Components

Gain Component Calculations

(1) **Calculate** the FX621 sensitivity.

Device Sensitivity – at the Detector Input (Figure 1) is dependent upon the V_{DD} value and is calculated as:

$$\text{Device Sensitivity} \approx \frac{0.2 \times V_{DD}}{2 \times \sqrt{2}} \quad \textit{(Vrms)}$$

(2) **Ascertain** the required National {Minimum Will-Decode} and [Maximum Will-Not Decode] Levels.

(3) **Calculate** the acceptable range of required Gain/ Attenuation for the levels in Note 2, using the "System Gain Set" amplifier.

The gain requirement is calculated as :

$$\text{[Max] / \{Min\} Gain} = \frac{\text{Device Sensitivity}}{\text{\{ Minimum Will-Decode Level \}}}$$

[or] [Maximum Will-Not Decode Level]

Choose a gain figure that meets both level requirements.

(4) **Calculate** the gain/attenuation components for the chosen gain.

Gain Components – for a differential input:

$R_1 = R_2$ $\quad C_8 = C_7$

$R_3 = R_4$ $\quad C_1 = C_2$

$$\text{Gain} = \frac{Z_{Feedback}}{Z_{Input}} \quad \frac{(R_4 \,//\, X(C_8))}{(R_1 + X(C_1))}$$

This calculation approximates as:

$$R_1 \approx \frac{R_4}{1.2 \times (\text{selected gain})}$$

and $$C_1 \approx \frac{1}{2\pi \times R_1 \times 6.0\text{kHz}}$$

– using the nearest preferred value components.

The values of R_1 and C_1 have been calculated to give a high-pass cut-off between the audio and SPM tone frequencies, approximately 6kHz. C_7 and C_8 are anti-alias components and are calculated for an approximate cut-off frequency of 32kHz.

Application Information .....

(5) Timing Components

In the 'SPM Packet' mode R_5 and C_4 set the minimum 'Tone' period (t_M), R_6 and C_5 set the minimum 'Space' period (t_S), and are calculated as follows:

$$t_M = 0.7(R_5 \times C_4). \qquad t_S = 0.7(R_6 \times C_5).$$

When calculating Tone and Space time settings the following points should be taken into consideration:

(1) Response and De-response times t_R and t_D.
(2) Component tolerances can alter the calculation.
(3) The MINIMUM expected pulse/space length must be catered for.

(6) Protection Diodes

As most telephone systems operate at voltages in excess of the Absolute Maximum Limits for damage, diodes D_1 – D_4 are essential for device protection.

(7) Component Tolerances

The tolerances of external components used with this device are dependent upon the required accuracy of the gain and pulse period timings.

Timing

Figure 3 shows the FX621 output timing – Timing value limits are given on the "Specification" page.

Note – There is no reaction to pulses or drop-outs of less than the valid Response or De-response time.

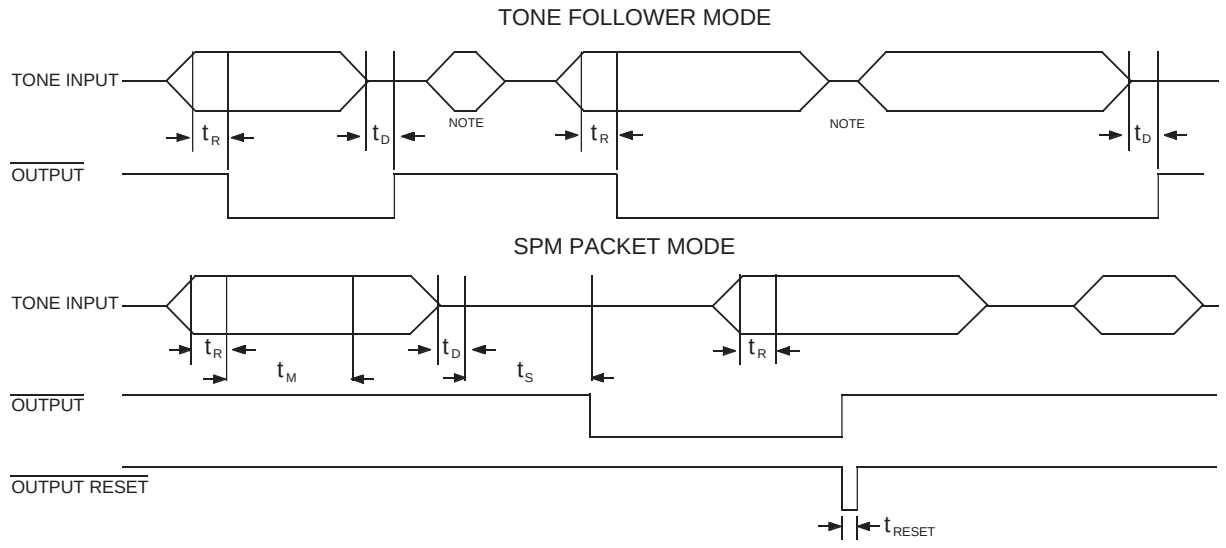


Fig.3 Output Timing

Example Values – for the FX621 to operate with the West German (16kHz) 'FTZ' Specification.

(a) Min. 'Will Decode' Level		=	71.3 mV rms
(b) Max. 'Will Decode' Level		=	10.0 V rms
(c) Max. 'Will-Not Decode' Level		=	34.6 mVrms
(d) Device Sensitivity @ 3.5V V_{DD}		≈	248.0 mVrms
Min. Gain Required	*(d÷a)*	≈	3.47
Max. Gain Allowed	*(d÷c)*	≈	7.17
Chosen Gain Figure		=	4.7

For a chosen gain figure of 4.7, a minimum Tone length of 80ms, a minimum Space length of 135ms and a V_{DD} of 3.5V, the required component values are :

R_1	68kΩ	C_1	330pF
R_2	68kΩ	C_2	330pF
R_3	390kΩ	C_3	1.0µF
R_4	390kΩ	C_4	820nF
R_5	100kΩ	C_5	1.0µF
R_6	120kΩ	C_6	1.0µF
		C_7	12pF
X_1	4.433619MHz	C_8	12pF

Tolerances: Resistors = ±1%. Capacitors = ±10%.

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply Voltage		-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		± 30mA
(other pins)		± 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX621P/LG/LS**	-30°C to + 70°C
Storage temperature range:	**FX621P/LG/LS**	-40°C to + 85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified :

V_{DD} = 3.5V T_{AMB} = 25°C Xtal/Clock f_C = 4.433619MHz Audio level 0dB ref = 775mV rms

Characteristics	System	See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage (V_{DD})			3.5	–	5.0	V
Supply Current (I_{DD})			–	1.0	1.4	mA
Input Logic “1”			70.0	–	100	% V_{DD}
Input Logic “0”			0	–	30.0	% V_{DD}
Output Logic “1”			80.0	–	–	% V_{DD}
Output Logic “0”			–	–	20.0	% V_{DD}
Impedances						
"Gain Set" Amplifier Input			1.0	–	–	MΩ
"Gain Set" Amplifier Output			–	–	10.0	kΩ
Analogue Detector Input			1.0	–	–	MΩ
Digital Inputs			0.5	1.0	–	MΩ
Digital Output			–	–	10.0	kΩ
Dynamic Values						
Sensitivity	12kHz/16kHz	1, 2	–	248	–	mVrms
Required Signal to Noise Ratio		7	–	45.0	–	dB
Upper Detector Threshold		2	2.06	2.1	2.14	V
Lower Detector Threshold		2	1.36	1.4	1.44	V
Amplifier Input Offset			–	15.0	–	mV
Xtal Oscillator Frequency				4.433619		MHz
Frequency Discrimination						
'Will-Decode' Frequency Limits	12kHz		11.82	–	12.18	kHz
	16kHz		15.76	–	16.24	kHz
'Will-Not Decode' Frequency Limits	12kHz		0	–	11.52	kHz
	12kHz		12.48	–	–	kHz
	16kHz		0	–	15.36	kHz
	16kHz		16.64	–	–	kHz
Timing Information – Fig.3						
Valid Tone Burst Length (t_M)	12/16kHz	3, 4	16.0	–	–	cycles
Valid Space Length (t_S)	12/16kHz	4	5.0	–	–	ms
Tone Response Time (t_R)	12kHz	5, 7	–	1.7	3.0	ms
	16kHz	5, 7	–	1.2	2.0	ms
De-response Time (t_D)	12kHz	6, 7	–	1.7	3.0	ms
	16kHz	6, 7	–	1.2	2.0	ms
SPM Output Reset Time (t_{RESET})	12/16kHz	4	150.0	–	–	ns

Notes

1. Device sensitivity at the Detector Input pin, or using the 'Gain Set' Amplifier at unity.
2. These values are quoted at 3.5 volt V_{DD}, any supply variation will alter levels accordingly.
3. Tone Follower mode.
4. SPM Packet mode, in this mode the minimum valid Pulse (Space) length is programmable by means of an RC network on the Pulse (Space) Length Time pin. If no RC network is used, the minimum valid tone length reverts to 16 cycles.
5. The time for the circuit to recognize a valid 'Tone' in the Tone Follower mode.
6. The time for the circuit to recognize a valid 'No Tone' in the Tone Follower mode.
7. The FX621 is a low-power zero crossing detector without on-chip filtering, for use with a good Signal-to-Noise ratio. The *FX611* is recommended for high noise environments. If the supply current requirement of the *FX611* is unacceptable, separate external filters should be employed with the FX621.

Package Outlines

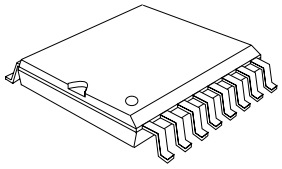
The FX621 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX621 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX621P 16-pin DIL Package

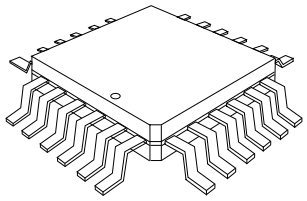
NOT TO SCALE



Max. Body Length	10.49mm
Max. Body Width	7.59mm

FX621LG 24-pin Package

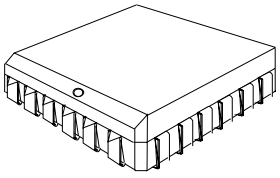
NOT TO SCALE



Max. Body Length	10.25mm
Max. Body Width	10.25mm

FX621LS 24-lead Package

NOT TO SCALE



Max. Body Length	10.40mm
Max. Body Width	10.40mm

Ordering Information

FX621P	16-pin plastic DIL
FX621LG	24-pin quad plastic encapsulated bent and cropped
FX621LS	24-lead plastic leaded chip carrier