# CML Semiconductor Products

# Tone Detector     FX105A

## 1.0    Features

- **Operates in High Noise Conditions**

- **≥ 36dB Signal Input Range**

- **High Sensitivity**

- **Low Power**

- **Adjustable Bandwidth**

- **Adjustable Frequency**

- **Wide Voltage Range (2.7V to 5.5V)**

- **Single and Multitone System Applications**
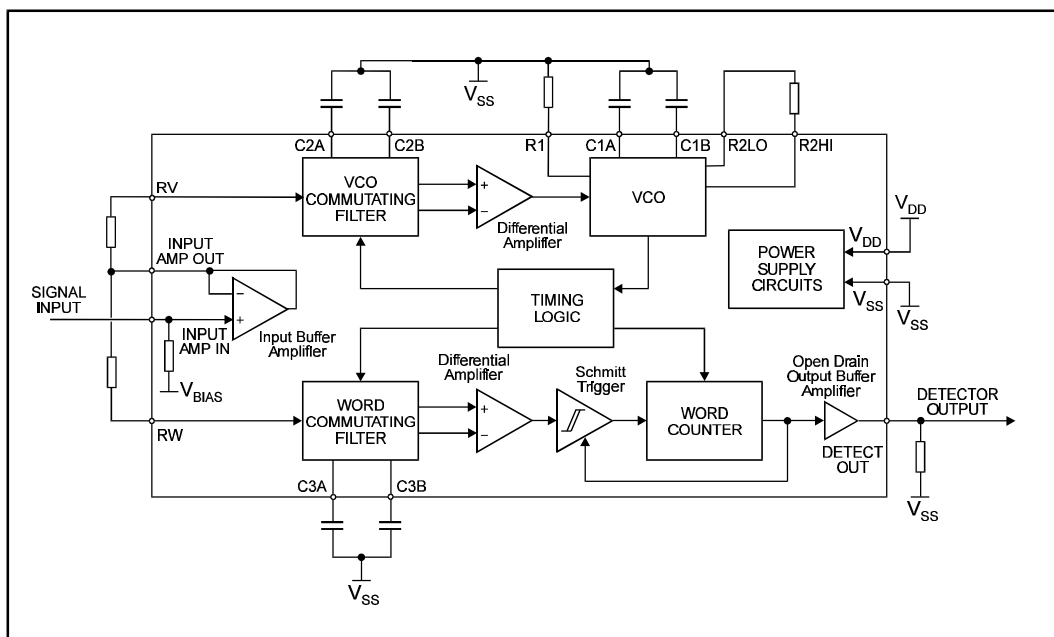


## 1.1    Brief Description

The FX105A is a monolithic CMOS tone operated switch, designed for tone decoding in single and multitone signalling systems.  The FX105A uses decoding techniques which allow a tone to be recognised in the presence of high noise levels or strong adjacent signals.  Detection centre frequency and bandwidth can each be independently adjusted.  The design is immune to high levels of harmonic and sub-harmonic interference.  Excellent noise immunity and constant bandwidth are maintained over a wide range of input signal levels.

**CONTENTS**

## 1.2    Block Diagram



**Figure 1 Block Diagram**

## 1.3    Signal List

| Package D4/P3 | Signal | | Description |
|---|---|---|---|
| Pin No. | Name | Type | |
| 1 | INPUT AMP IN | I/P | AC couple to this input of the input buffer amplifier. |
| 2 | INPUT AMP OUT | O/P | The input buffer amplifier output. |
| 3 | RW | I/P | The input to the Detect/Word filter. |
| 4 | RV | I/P | The input to the VCO loop filter. |
| 5 | C3A | O/P | Word filter capacitor pin A. |
| 6 | C3B | O/P | Word filter capacitor pin B. |
| 7 | C2A | O/P | VCO Loop filter capacitor pin A. |
| 8 | C2B | O/P | VCO Loop filter capacitor pin B. |
| 9 | DETECT OUT | O/P | Open drain PMOS output, active on detect. Note that a load resistor to $V_{SS}$ is required. |
| 10 | $V_{SS}$ | Power | Ground. |
| 11 | R2HI | I/P | Bandwidth control resistor pin A. |
| 12 | R2LO | I/P | Bandwidth control resistor pin B. |
| 13 | C1B | O/P | VCO capacitor B. |
| 14 | C1A | O/P | VCO capacitor A. |
| 15 | R1 | I/P | VCO discharge resistor.  When potentiometer tuning is required, a series resistor is recommended to prevent possible shorting to ground. |
| 16 | $V_{DD}$ | Power | Power supply. |

**Notes:**  I/P   =   Input
O/P   =   Output

## 1.4    External Components
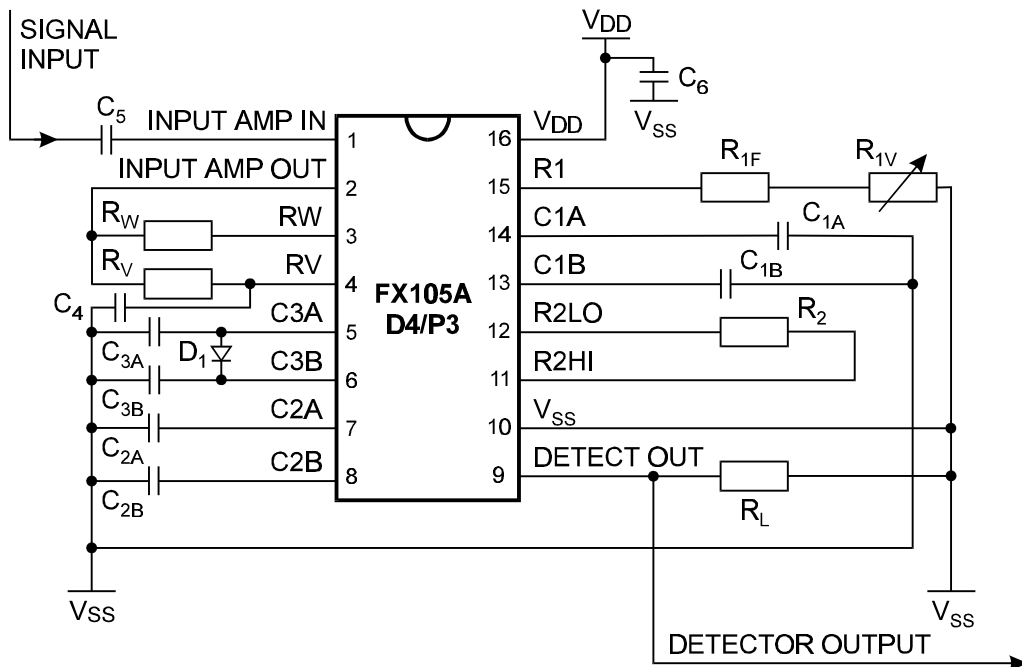


| | | | |
|---|---|---|---|
| $C_{1A}$ | See section 1.6 | $R_{1F}$ | See section 1.6 |
| $C_{1B}$ | See section 1.6 | $R_{1V}$ | See section 1.6 |
| $C_{2A}$ | See section 1.6 | $R_2$ | See section 1.6 |
| $C_{2B}$ | See section 1.6 | $R_L$ | 20kΩ    ±20% |
| $C_{3A}$ | See section 1.6 | $R_V$ | See section 1.6 |
| $C_{3B}$ | See section 1.6 | $R_W$ | See section 1.6 |
| $C_4$ | See section 1.6 | $D_1$ | IN914 or similar |
| $C_5$ | 0.27µF    ±20% | | |
| $C_6$ | 0.1µF    ±20% | | |

Notes:    1.   For improved performance C4 may be chosen to provide 30° phase shift at the VCO
loop filter input.
2.   For compatibility with the FX105P; capacitors (C1 .... C4) may be connected to $V_{DD}$
instead of $V_{SS}$.
3.   For improved de-response time, a diode ($D_1$) may be added.
4.   Any value load resistance ($R_L$) may be used, providing the maximum load current does
not exceed the value given in section 1.7.1

**Figure 2  Recommended External Components**

## 1.5    General Description

The input signal to the FX105A is ac coupled to the buffer amplifier input, which is internally biased at 50% of supply voltage.  The signal appears at the output of the buffer amplifier as an ac voltage superimposed on the dc bias level.  The signal is then coupled via $R_V$ and $R_W$ to the voltage controlled oscillator (VCO) and word sampling switches, which cyclically connect $C_2$ and $C_3$ into the circuit to form four sample-and-hold RC circuit integrators.  See Figure 3.

With no input signal level, each capacitor charges to the dc bias level so differential voltages are zero. When an input signal is applied each capacitor receives an additional charge.  This charge is determined by the integrated average of the signal waveform during the time the capacitor is switched into the circuit.

Figure 3 shows the operating sequence of the VCO sampling switches and their relationship to a locked-on in-band signal.  $C_{2A}$ and $C_{2B}$ should not receive any additional charge since they always sample the input as it crosses the dc bias level.  Should the signal not be locked to the VCO, a positive or negative charge voltage will appear on $C_{2A}$ or $C_{2B}$.  This voltage, when differentially amplified, is applied to the VCO as an error correcting signal to enable the VCO to "lock."

Figure 3 also shows the operating sequence of the "Word" sampling switches and their relationship to a locked-on in-band signal.  As the figure shows, the charge applied to $C_{3A}$ should always be positive, and the charge applied to $C_{3B}$ should always be negative (with respect to the common bias level).

These capacitor potentials are differentially amplified and applied to a dc comparator, which switches at a pre-determined threshold voltage $V_{TH}$.  The comparator output is a logic signal used to control a counter.  This counter switches the FX105A output ON when the comparator output is maintained in the "Word present" state for a minimum number of consecutive signal samples.  The activated output switch reduces the comparator threshold by 50%, introducing threshold hysteresis.  Output chatter with marginal input signal amplitudes is thereby minimised.
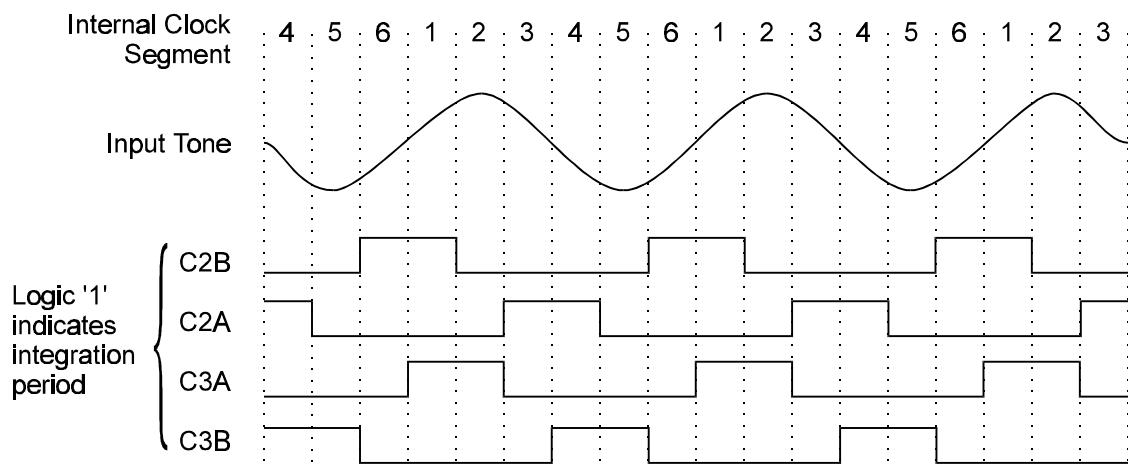


**Figure 3 Sampling Clocks of Commutating Filters**

## 1.6     Application Notes

### 1.6.1    General
The external components shown in Figure 2 are used to adjust the various performance parameters of the FX105A.  The signal-to-noise performance, response time and signal bandwidth are all interrelated factors which should be optimised to meet the requirements of the application.

By selecting component values in accordance with the following formulae, optimum circuit performance is obtained for any given application.

First define the following application parameters:

(a)     The input frequency to be detected ($f_0$).  The free running frequency of the VCO is set to 6 times this frequency by observing the output across $C_1$ or $R_1$.  (The frequency observed at pin 15 ($R_1$) is 6 x $f_0$ and the frequency observed at pins 13 or 14 ($C_{1A}$ or $C_{1B}$) is 3 x $f_0$).
(b)     The FX105A Minimum Usable Bandwidth (MUBW).  This is obtained by taking into account the worst case tolerances ($\Delta f_0$) of the input frequency and the variations in the FX105A VCO frequency due to supply voltage ($\Delta V_{DD}$) and temperature ($\Delta$TEMP) variation of the FX105A and its supporting components.
(c)     The maximum permissible FX105A response time.
(d)     The minimum input signal amplitude.
(e)     The maximum input signal amplitude.

Using this information the appropriate component values can be calculated, and the signal-to-noise performance can be read from a chart.  Do not add large safety margins for response time and minimum signal amplitude: reasonable margins are already included in the formulae.  Excessive margins may result in reduced noise immunity.

### 1.6.2    Method for Calculating External Component Values
The example on the following pages demonstrates the calculation of component values for any given application.  For the purpose of this example, the values below are used:

(a)     $f_0$ = 2800 Hz
(b)     $\Delta$TEMP = 100°C,  $\Delta V_{DD}$ = 1V,   $\Delta f_0$ = 0.5%
(c)     Maximum allowed response time $T_{ON}$ = 50msec
(d)     Minimum input signal amplitude $V_{IN\ MIN}$ = 200 mVrms
(e)     Maximum input signal amplitude $V_{IN\ MAX}$ = 400 mVrms

### 1.6.2.1 Calculate $R_1 C_1$  ($C_{1A} = C_{1B}$)
The components $R_1$, $C_{1A}$ and $C_{1B}$ set the free running frequency of the VCO and therefore the $f_0$ of the FX105A.  As shown below, the frequency of 2800 Hz corresponds to a capacitor value of 220 pF and a resistor value of 385kΩ.  This resistance can be achieved with a 300 kΩ fixed resistor and a 100kΩ potentiometer.  R1 should lie in the range 100kΩ to 680kΩ.

$$R_1 C_{1A} = 1/[2Kf_0] = 1/(2 \times 2.1 \times 2800) = 85\mu sec$$

where K is a constant = 2.1 ± 5%.  Note that above $f_0$ = 1kHz, the value of K increases with $f_0$ up to a maximum of 2.5 at 20kHz.

Therefore        $R_1 \approx 385$kΩ for $C_{1A} = C_{1B}$ = 220pF

### 1.6.2.2 Calculate Minimum Usable Bandwidth (%)
Minimum Usable Bandwidth (MUBW) is the TOTAL (%) bandwidth required for the following:

(a)    Input signal frequency tolerance ($\Delta f_0$)
(b)    FX105A VCO temperature coefficient ($T_C = -100$ ppm/ºC)
(c)    FX105A VCO supply voltage coefficient ($V_C = 2330$ ppm/V)

Add (a), (b) and (c) and express as TOTAL (%) bandwidth, *not* as a ± (%) value.

$$MUBW = \Delta f_0 + |T_c|\Delta TEMP + V_c\Delta V_{DD}$$

$$MUBW = 0.5 + 0.01 \times 100 + 0.233 \times 1 \approx 2\%$$

### 1.6.2.3 Calculate the Recommended Operating Bandwidth
Note again that this is the TOTAL (%) bandwidth:

$$BW = \tfrac{1}{2} [10 + MUBW] = \tfrac{1}{2} (10 + 2) = 6\%$$

### 1.6.2.4 Select $R_2$ for Operating BW

$$R_2 = 4.8\ BW/ [10.35 - BW] = 4.8 \times 6/ (10.35 - 6) \approx 6.8 k\Omega$$

The exact bandwidth given by any value of $R_2$ will vary slightly. In applications where an exact bandwidth is required, $R_2$ should be a variable resistor to permit adjustment.

### 1.6.2.5 Calculate $R_V C_{2A}$ ($C_{2A} = C_{2B}$)  Use nearest preferred values

$$R_V C_{2A} \approx 100/ [3\ f_0\ BW] \approx 100/ (3 \times 2800 \times 6) \approx 2msec$$

Therefore          $R_V \approx 200 k\Omega$ for $C_{2A} = C_{2B} = 10nF$

### 1.6.2.6 Define the Maximum Allowed Response Time
The maximum response time ($T_{ON}$) is the sum of the VCO lock time ($T_{LOCK}$) and the Word integration time ($T_{WORD}$). The FX105A's $T_{ON}$ must not exceed the maximum time allowed for the application, but a value lying near the maximum gives the best S/N performance.

(a)    Calculate $T_{LOCK}$

$$T_{LOCK} = 150/ [f_0\ BW] = 150/ (2800 \times 6) \approx 9msec$$

Note: $T_{LOCK}$ may vary from near zero to the value given, causing corresponding variations in actual $T_{ON}$.

(b)    Calculate Maximum Allowable $T_{WORD}$

$$T_{WORD} = T_{ON_{MAX}} - T_{LOCK} = 50 - 9 = 41\ msec$$

Note: Since the maximum allowed response time ($T_{ON}$) is 50 msec, a maximum Word integration time of 41 msec is available.

### 1.6.2.7 Calculate $R_W C_{3A}$ ($C_{3A}$ = $C_{3B}$) Use nearest preferred values.

$$R_W C_{3A} \approx T_{WORD} / [-3\ln (1 - V_{TH} / V_{IN_{MIN}} ) ]$$

where $V_{TH}$ is the word filter sensitivity, see Section 1.7.1

A signal amplitude of 200 mV and a resistor value $R_W$ of 510kΩ with a 0.1µF capacitor for $C_{3A}$ and $C_{3B}$ will yield a $T_{WORD}$ time of 20msec.  This in turn yields a response time of 9msec + 20msec = 29msec.

### 1.6.2.8 Calculate the Maximum De-response Time

$$T_{OFF} \approx -3 R_W C_{3A} \ln (V_{TH} / V_{IN_{MAX}} )$$

where $V_{TH}$ is the word filter sensitivity, see Section 1.7.1

For improved de-response time, a diode (1N914 or similar) can be placed between pins 5 and 6, as shown in Figure 2.  The formula and figure below show the approximate time the FX105A will take to turn off after an in-band signal has been removed.  The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300 mV$_{rms}$.  Figure 4 is for $V_{DD}$ = 5V; for lower $V_{DD}$ then $K_{DT}$ increases.

$$T_{OFF} \approx K_{DT} R_W C_{3A}$$

So for a maximum signal amplitude of 400mV, a resistor value $R_W$ of 510kΩ with a 0.1µF capacitor for $C_{3A}$ and $C_{3B}$ and a diode between pins 5 and 6, a de-response time of ≈ 182 msec is obtained.
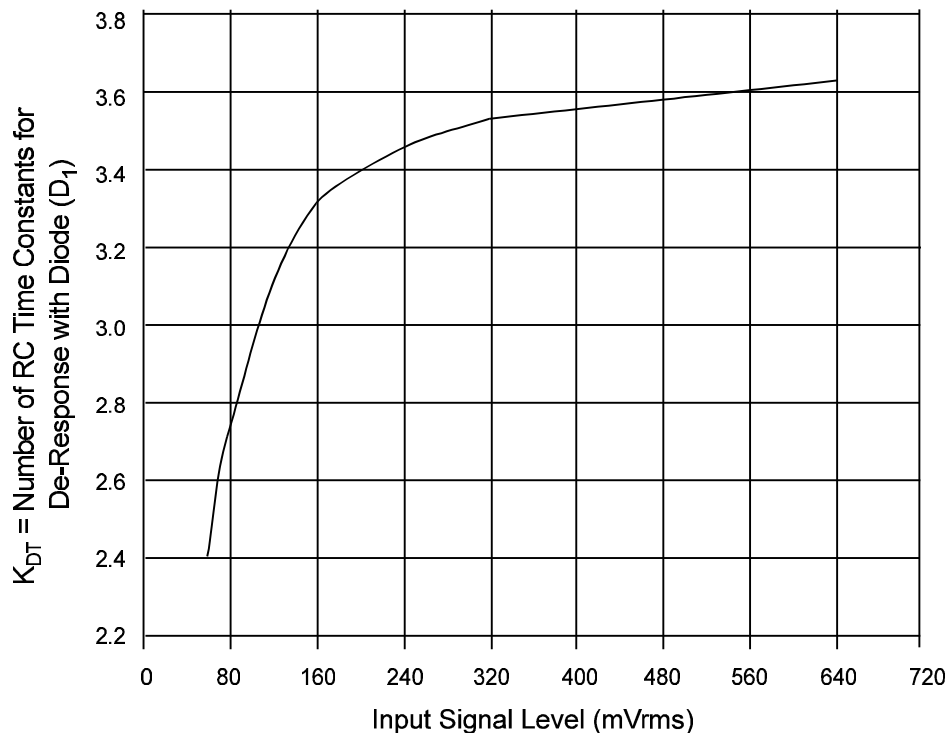


**Figure 4  $K_{DT}$ Factor for $T_{OFF}$ vs. Signal Input Amplitude**

### 1.6.2.9 Calculate Signal to Noise Performance

Worst-case S/N calculations depend on calculation of a value "M" using the formula shown below:

$$M = R_W C_{3A} / [3 R_V C_{2A}]$$

substituting our example values,

$$M = 510 \times 0.1 / (3 \times 200 \times 0.01) = 8.5$$

By substituting this value for M in Figure 5 the minimum required S/N of an in band tone with respect to an adjacent interfering tone can be found. This has to be increased if the required tone amplitude is close to the word filter sensitivity $V_{TH}$.
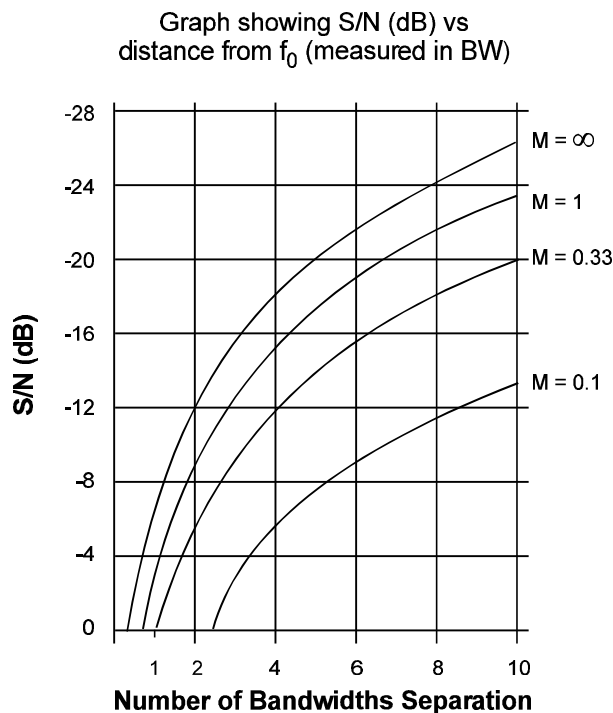
Graph showing S/N (dB) vs
distance from $f_0$ (measured in BW)



**Figure 5  S/N vs. BW Separation**

The following formula expresses the reduction in noise immunity as the input signal approaches the word filter sensitivity $V_{TH}$.

$$\text{required S/N} = 20 \log (V_{IN} / [V_{IN} - V_{TH}]) + \text{S/N}_{\text{Figure 5}}$$

If this S/N is better than required for the application, $R_W C_{3A}$ can be reduced, or the operating bandwidth can be increased to obtain a faster tone detection time.

If the S/N performance is not adequate, the operating bandwidth can be reduced toward the MUBW, or $R_W C_{3A}$ can be increased to improve S/N performance at the expense of a slower response time.

### 1.6.2.10  Calculation of PLL Filter Phase Shift

Capacitor $C_4$ is used to phase shift the input to the VCO commutating filter by 30°, thus shifting the sampling clocks by the same amount. This enables the "Word" sampling filter to sample and integrate at the maxima and minima of the input tone.

$$C_4 = \tan (30°) / [2\pi f_0 R_V] \approx 0.092 / [f_0 R_V] \approx 164pF$$

## 1.7    Performance Specification

### 1.7.1    Electrical Performance

**Absolute Maximum Ratings**
Exceeding these maximum ratings can result in damage to the device.

|  | Min. | Max. | Units |
|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) | -0.3 | 7.0 | V |
| Voltage on any pin to $V_{SS}$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Current into or out of $V_{DD}$ and $V_{SS}$ pins | -30 | +30 | mA |
| Current into or out of any other pin | -20 | +20 | mA |
| Maximum Output Switch Load Current |  | +10 | mA |

| P3/D4  Package | Min. | Max. | Units |
|---|---|---|---|
| Total Allowable Power Dissipation at Tamb = 25°C |  | 800 | mW |
| ... Derating |  | 13 | mW/°C |
| Storage Temperature | -55 | +125 | °C |
| Operating Temperature | -30 | +85 | °C |

**Operating Limits**
Correct operation of the device outside these limits is not implied.

|  | Notes | Min. | Max. | Units |
|---|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) |  | 2.7 | 5.5 | V |
| Operating Temperature |  | -30 | +85 | °C |

## Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD}$ = 3.0V to 5.0V, Tamb = −40°C to +85°C,  Load resistance on decoder output pin = 20kΩ

|  | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **Static Parameters** | | | | | |
| $I_{DD}$ | 2 | | 0.9 | 3.0 | mA |
| Amplifier Input Impedance | | | 200 | | kΩ |
| Digital Output Impedance | | | 500 | | Ω |
| Analogue Output Impedance | | | 1000 | | Ω |
| **Dynamic Parameters** | | | | | |
| **Input Signal** | | | | | |
| Amplitude | 2 | | | 1.0 | Vrms |
| Frequency | | 40 | | 20,000 | Hz |
| Response Threshold | 1 | | 18 | 38 | mVrms |
| Deresponse Threshold | 1 | 5 | 9 | | mVrms |
| BW Range | | 5 | | 10 | %$f_0$ |
| Signal to Noise Performance | | -6 | -9 | | dB |
| ($f_0$/2) Subharmonic Rejection | | | 30 | | dB |
| (5 $f_0$) Harmonic Rejection | | | 20 | | dB |
| **VCO** | | | | | |
| Frequency | 3 | 240 | | 120,000 | Hz |
| Frequency Stability (Δ TEMP) | 3 | | 100 | | ppm/°C |
| Frequency Stability (Δ $V_{DD}$) | 3 | | 2330 | | ppm/V |
| **Amplifier** | | | | | |
| Open Loop Gain | | | 60 | | dB |
| Gain Bandwidth Product | | | 1.0 | | MHz |
| Closed Loop Gain | | | 0 | | dB |
| **Word Commutating Filter** | | | | | |
| Sensitivity  ($V_{TH}$) | 4 | | 12.5 | | mVrms |

**Notes:** 1. With diode ($D_1$) fitted.
2. For $V_{DD}$ = 5V.  Multiply by $V_{DD}$/5V for other supply values.
3. Observing pins 13, 14 or 15 (D4/P3 package) will cause a frequency shift due to additional loading.  If tuning the centre frequency by observing the VCO, design in a buffer amplifier between pin 15 and the probe/calibration point and tune with no input signal.  Otherwise, tune by observing the detect output band edges while sweeping the input signal.
4. Adjust according to equation for $R_2$ in Section 1.6.2.

## 1.7.2    Packaging
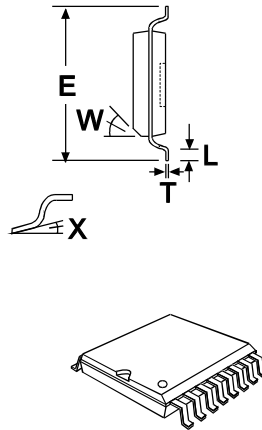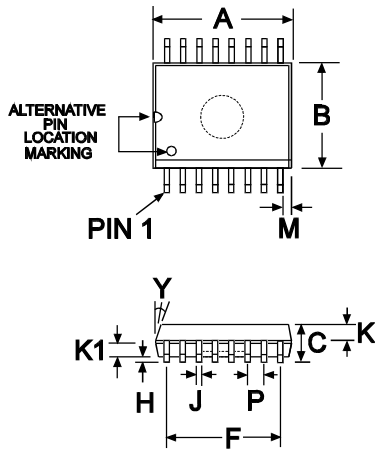


| DIM. | MIN. | TYP. | MAX. |
|------|------|------|------|
| A | 0.395 (10.03) | | 0.413 (10.49) |
| B | 0.291 (7.39) | | 0.299 (7.59) |
| C | 0.093 (2.36) | | 0.105 (2.67) |
| E | 0.394 (10.01) | | 0.419 (10.64) |
| F | | 0.366 (9.29) | |
| H | 0.004 (0.10) | | 0.012 (0.30) |
| J | 0.013 (0.33) | | 0.019 (0.48) |
| K | | 0.041 (1.04) | |
| K1 | | 0.041 (1.04) | |
| L | 0.016 (0.41) | | 0.050 (1.27) |
| M | 0.021 (0.53) | | 0.031 (0.79) |
| P | | 0.050 (1.27) | |
| T | 0.009 (0.23) | | 0.012 (0.30) |
| W | | 45° | |
| X | 0° | | 8° |
| Y | | 7° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**Figure 6  -  SOIC Mechanical Outline:  *Order as part no. FX105AD4***
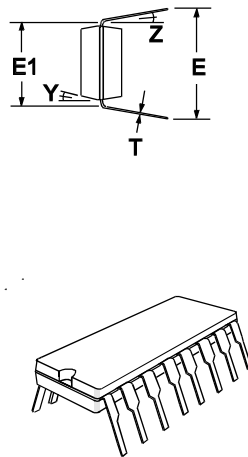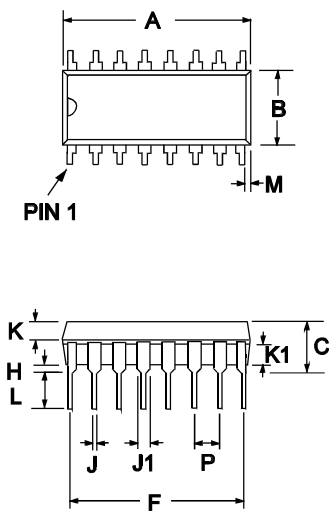


| DIM. | MIN. | TYP. | MAX. |
|------|------|------|------|
| A | 0.740 (18.80) | | 0.810 (20.57) |
| B | 0.240 (6.10) | | 0.260 (6.60) |
| C | 0.135 (3.43) | | 0.175 (4.45) |
| E | 0.300 (7.62) | | 0.390 (9.91). |
| E1 | 0.290 (7.37) | | 0.325 (8.26) |
| F | | 0.70   (17.78) | |
| H | 0.015 (0.38) | | 0.035 (0.89) |
| J | 0.015 (0.38) | | 0.023 (0.58) |
| J1 | 0.040 (1.02) | | 0.065 (1.65) |
| K | 0.056 (1.42) | | 0.064 (1.63) |
| K1 | 0.056 (1.42) | | 0.064 (1.63) |
| L | 0.121 (3.07) | | 0.150 (3.81) |
| M | | 0.028 (0.72) | |
| P | | 0.100 (2.54) | |
| T | 0.008 (0.20) | | 0.015 (0.38) |
| Y | | 7° | |
| Z | | 5° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**Figure 7  -  DIL Mechanical Outline:  *Order as part no. FX105AP3***