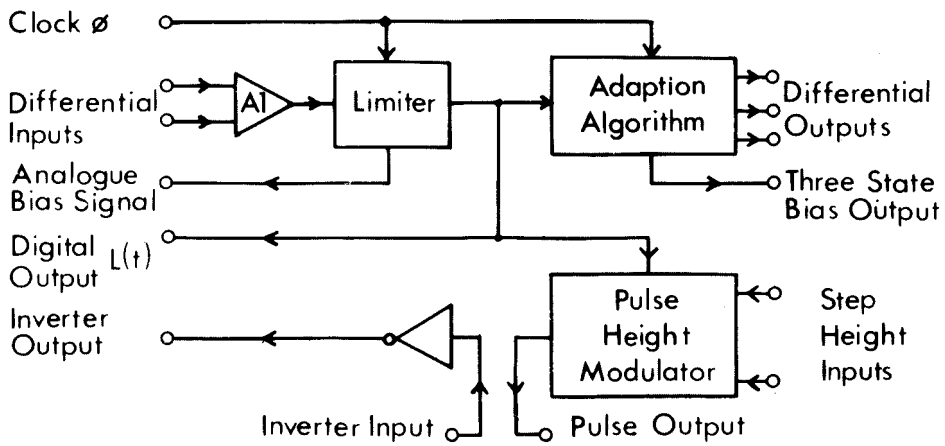
CONSUMER MICROCIRCUITS LTD

FUNCTIONAL SCHEMATIC OF THE FX309



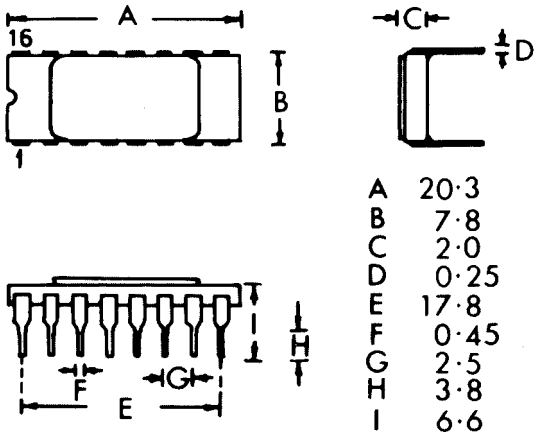
FX-309

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATION. (CVSD)

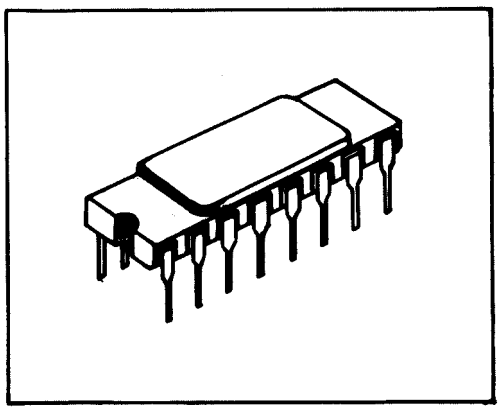
FEATURES

- LOW POWER CMOS PROCESS
- PRE-PROGRAMMED ADAPTIVE 3-BIT ALGORITHM
- PERFECT IDLE CHANNEL NOISE PATTERN
- CLOCK FREQUENCIES UP TO 1MHZ
- FLEXIBLE BIASING
- SINGLE INTEGRATION
- TELECOMMUNICATIONS
- SIGNAL ENCODER/DECODER
- COMPLEX WAVE FORM ANALYSIS
- AUDIO DELAY
- SCRAMBLER

16 Lead Dual In Line Ceramic Package



A	20·3
B	7·8
C	2·0
D	0·25
E	17·8
F	0·45
G	2·5
H	3·8
I	6·6



Dimensions in mm.

MAXIMUM RATINGS

SYMBOL	PARAMETER	NOTES & CONDITIONS	MIN	TYP	MAX	UNITS
VDD	DC Supply Voltage	Recommended Operating Range 4.5V to 8V	−0.3		8	Vdc
Vin	Input Voltage	All inputs	−0.3		8	Vdc
I	DC Current drain per pin				10	mA
T_A	Operating temp. range		−40		85	^oC
T_{stg}	Storage temp. range		−55		125	^oC
P_{max}	Max. Device Dissipation	Ambient temperature 20^{o}C			400	mW

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	PIN No.	NOTES & CONDITIONS	VDD	MIN	TYP	MAX	UNITS
	Input/Output Leakage Current		to VDD −300mV	8	—	±2	±300	nA
I_{DD}	Supply Current Consumption	3,15	Inverter linearly biased	4.5 8	— —	4 15	6 20	mA
		3,15	When in Logic Mode	4.5 8	— —	— —	0.3 1	
V_{IL}	Input Logic Levels	1,4	'0' Level	4.5 8	— —	0 0	1.5 3	V
V_{IH}		1,4	'1' Level	4.5 8	3 5	4.5 8	— —	
V_{OL}	Output Logic Levels	2,16,5	'0' Level	4.5 8	— —	0 0	0.5 0.5	V
V_{OH}		2,16,5	'1' Level	4.5 8	4.45 7.2	4.5 8	— —	
R_{ON}	ON Resistance	2	V_O = OV dc	4.5 8	— —	3K 2K	6K 4K	Ω
		2	V_O = VDD	4.5 8	— —	3K 2K	6K 4K	
		5,8,16	V_O = OV dc	4.5 8	— —	150 100	300 200	
		5,6,16	V_O = VDD	4.5 8	— —	150 100	300 200	
		6,7,9, 10,11	Pin 7 to 6, pin 10 to 9 Pin 10 to 11	4.5 8	— —	450 300	800 600	
		6,7,9 10, 11	Pin 6 to 7, pin 9 to 10 Pin 11 to 10	4.5 8	— —	450 300	800 600	
		14		4.5 8	— —	20K 15K	30K 25K	
		14		4.5 8	— —	20K 15K	30K 25K	

SWITCHING CHARACTERISTICS

SYMBOL	PARAMETER	PIN No.	NOTES AND CONDITIONS	VDD	MIN	TYP.	MAX.	UNITS
t_r	Output Rise Time (C_{LOAD} = 10pF)	2, 5, 6, 7, 8, 9, 11, 16		4.5 8	– –	100 80	300 200	nS
		14		4.5 8	– –	350 350	600 600	
t_f	Output Fall Time (C_{LOAD} = 10pF)	2, 5, 6, 7, 8, 9, 11, 16		4.5 8	– –	100 80	300 200	
		14		4.5 8	– –	350 350	600 600	
t_{PLH}	Propagation Delay Time	2, 5, 6, 7, 8, 9, 11, 16	From inputs or clock	4.5 8	– –	250 200	600 500	
		14	Output Analogue Switch	4.5 8	– –	60 50	100 100	
PW_{CH}	Min. Clock Pulse Width	1		4.5	500	–		

OPERATIONAL AMPLIFIER CHARACTERISTICS

SYMBOL	PARAMETER	PIN No.	NOTES AND CONDITIONS	VDD	MIN.	TYP.	MAX.	UNITS
V_{IO}	Input offset voltage	12WRT 13	(at $\frac{VDD}{2}$)	4.5 8	– –	±100 ±150	±200 ±300	mV
V_{ICR}	Common mode input voltage range W.R.T. $\frac{VDD}{2}$	12, 13	Input Offset Change of 15mV	4.5 8	±0.5 ±1.5	±1.0 ±2.3	– –	V
			Input Offset Change of 30mV	4.5 8	±0.6 ±1.6	±1.1 ±2.4	– –	
t_{PLH}	Propagation Delay Time	12 & 13 to 14		4.5 8	– –	5.5 2.5	8 3	μS
CMRR	Common Mode Rejection Ratio	12,13,14	Input Offset Change of 15mV	4.5 8	36 46	42 49	– –	dB
			Input Offset Change of 30mV	4.5 8	32 40	37 44	– –	
			For small signals	4.5 8	– –	62 67	– –	
A_{OL}	Open Loop Differential Gain	12,13,14		4.5 8	– –	80K 80K	– –	
	Bandwidth (–3dB)	12,13,14		4.5 8	– –	50 50	– –	KHZ

OPERATION

Encoder

The input differential amplifier drives a clocked limiter and this produces the digital output. The sequential signal so produced is analysed by the adaption logic which detects three 'ones' or 'zeros' and produces compand outputs. These, when integrated in duplicated RC networks, produce opposite polarity voltages related to the power of the duplicated RC networks, produce opposite polarity voltages related to the power of the input signal. One of these voltages is switched to the "local decoder" RC via the "pulse height modulator"; the polarity of the switched voltage being defined by the logic output. The output from the local decoder is fed to the non inverting input of the differential amplifier and closely tracks the input signal.

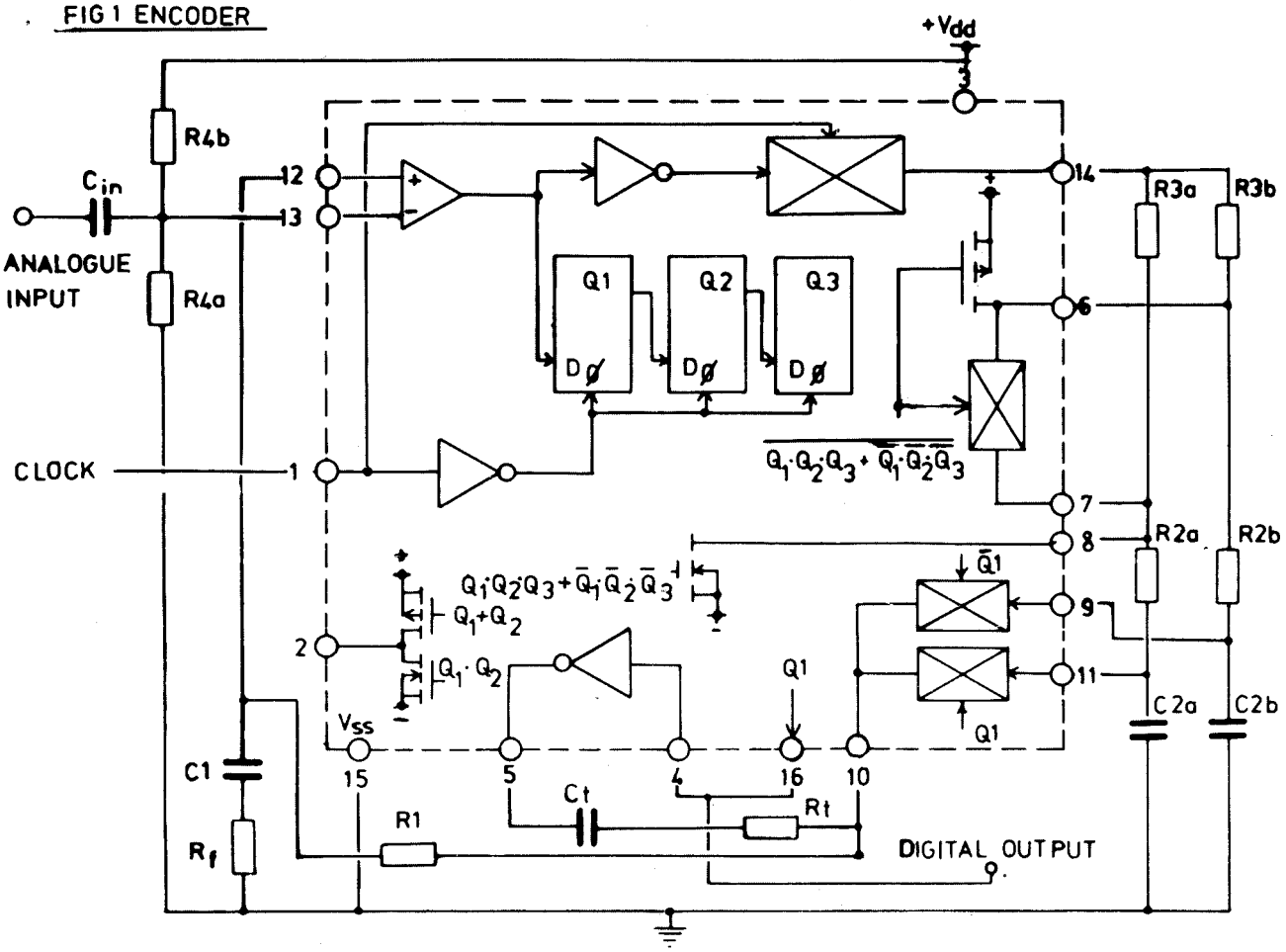
The maximum and minimum difference voltage between the compand capacitors defines the dynamic range of the pulse height and saturated switching ensures this is maximised, the complementary process ensures a highly symmetrical output pulse.

DECODER

When operating as a decoder similar circuitry is used with the feedback loop open circuit and the digital signal fed in via the input amplifier, the logic threshold being defined by the other input of the amplifier.

EXTERNAL COMPONENT CONNECTIONS FOR THE FX-309

FIG 1 ENCODER



FACTORS AFFECTING SELECTION OF COMPONENTS

Cin

Cin feeds the input signal to the comparator. It forms a high pass filter with R4a & R4b. As the two biasing resistors are normally equal, the input time constant, Tin = Cin R4a/2, should be chosen so as not to significantly attenuate the lowest input signal frequency that it is required to encode.

R4a & R4b

These components contribute to the input filtering as described above. They also supply the input bias voltage and are therefore normally made equal. The larger their values, the less the drain on supply current. However this has a greater effect on input leakage and the resultant danger of picking up extraneous signals such as mains hum. When encoding small signals they will therefore normally be less than 10MΩ. The higher the value of these components the smaller the input coupling capacitor required. It will assist the minimizing of pickup if the encoder is driven from a low impedance source.

R3a & R3b

The bias generated at pin 14 and fedback to pin 12 is supplied via these resistors. The bias is necessary to overcome input leakage and offset. Two resistors are used to preserve the natural symmetry of the circuit and thus minimise second harmonic distortion. Their impedances must be high so that the contribution pin 14 makes to the tracking signal at pin 12 is negligible within the band of interest. The input bias voltage from pin 14 is only relevant when the circuit is in the non-compand state since the bias voltage is defined by R2a & R2b when the circuit is companding. The time constants R3a C2a and R3b C2b must be sufficiently large

to attenuate the feedback signal from pin 14 and guarantee that there is no oscillation around the loop from pin 14 to 6 and 8 to 9 and 11 to 10 to 12 and onto 14 again. R3a and R3b are normally made much greater than R2a and R2b since they will limit the maximum achievable step height as described below and in figs. 3 i and ii.

R2a and R2b

These resistors in conjunction with C2a and C2b determine the rate of rise and fall of the step height which is developed across pins 9 and 11, the time constant being given by:-

$$T = \frac{R_1 (R2a + R2b)\, C2a}{\frac{(R2a + R2b)}{2} + 2R_1}$$

If one assumes that the external resistors are much greater than the output impedance of the pins to which they are attached.
If $R_1 >> R2a = R2b$ then a simpler approximation may be used:-

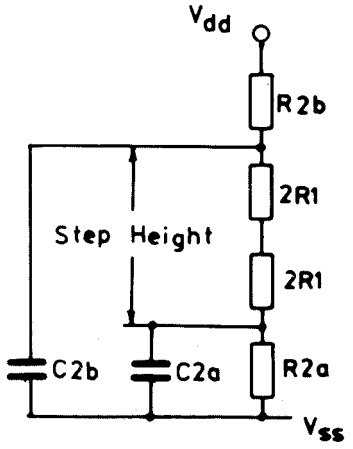
$$T = R2a\ C2a$$

Normally symmetrical rise and fall times are used so pins 7 and 8 are linked. The equivalent circuit of the compand circuitry when the step height is increasing and decreasing as shown in figs. 3(i) and (ii) respectively. The maximum achievable step height is therefore limited by the supply voltage and by the ratio 2R1:R2a. Step height maximum 100% companding is:-

$$H = \frac{2VDD\ R1}{2R1 + R2b}$$

C2a and C2b

These capacitors are used to integrate the compand outputs from pins 6 and 8 and define the rate of rise and fall of the step amplitude at pin 10. Usually for speech a syllabic time constant of around 10mSec is chosen, some specifications call for a time of approximately 4mSec. The actual choice of time depends on the rate of change of the input signal amplitude expected. It would obviously be faster than the values suggested if music was to be encoded and may well be slower in other applications. The decay time may be increased by including a resistor between pins 7 and 8.



Increasing step height
Fig.3(i) (Companding)

R_1 C_1

This is the local decoder, it performs an integration function on the variable step output at pin 10 which is the output of the pulse height modulator. The integrated waveform approximates to input signal. The time constant $R_1 C_1$ should be chosen such that it attenuates components of the output pulse train which are outside the message band. For short time constants the greater the amplitude and frequency of signals that can be tracked but a higher clock frequency is then required to maintain faithful tracking and low quantization noise. Generally since R_1 loads the output of the pulse height modulator the value of R_1 should be chosen so as to be high compared with R2a and R2b.

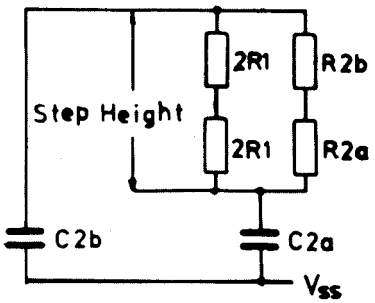


Fig 3(ii) Decreasing step height
(not companding)

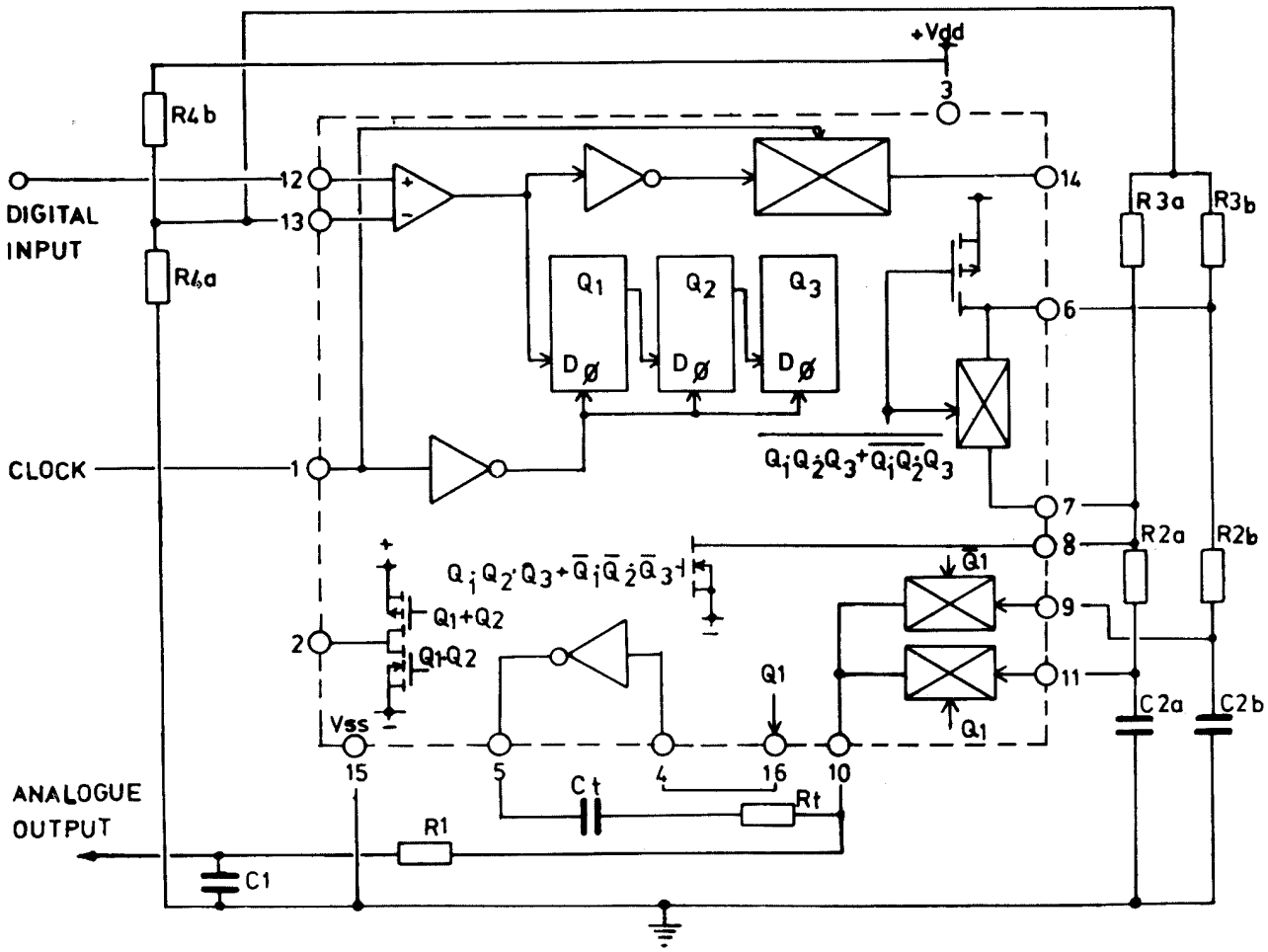
Ct, Rt

These components are combined to enable the minimum step height in the non-compand condition, to be adjusted. They are used to guarantee a perfect 0101 . . . idle channel pattern. The step output at pin 10 is exponentially integrated by R_1, C_1. When no input signals are present, the logic output at pin 16 is A.C. coupled by Ct and attenuated through Rt into the resistors R_2a, R_2b and R_1 via the FX309's internal switches. To maximise dynamic range, the step height is adjusted to a minimum, such that zero idle channel noise is achieved. The minimum step height is given by the following expression:-

$$H_{min} \cong \frac{V_{DD} \cdot R_{2a}}{2Rt} \qquad \text{assuming } R_1 >> R_{2\,a} \text{ and } X_{ct} >> Rt$$

NB. $R_2a = R_2b$

FIG. 2. DECODER



DECODER COMPONENT SELECTION

The decoder component values should be chosen so that the performance of the decoder matches the performance of the encoder as closely as possible. The circuit is therefore very similar, however the loop is no longer closed and it is not necessary to use the system in the self biasing mode since the input digital waveform easily overcomes any input offset voltage.

It should be borne in mind that any mismatch between component values used around the encoding and decoding circuits could lead to distortion. The principle considerations being that asymmetry between the time constants R2a C2a and R2b C2b encode and their corresponding decode time constants will contribute pro-rata to any overall distortion.

RECOMMENDED COMPONENTS FOR FX-309 ENCODER-DECODER.

Resistors (All ¼W 2%)

R1	360k ohm	2%
R2a	12k ohm	1%
R2b	12k ohm	1%
R3a	470k ohm	2%
R3b	470k ohm	2%
R4a	1M ohm	2%
R4b	1M ohm	2%
Rf	1k ohm	2%
Rt	470k ohm	2%

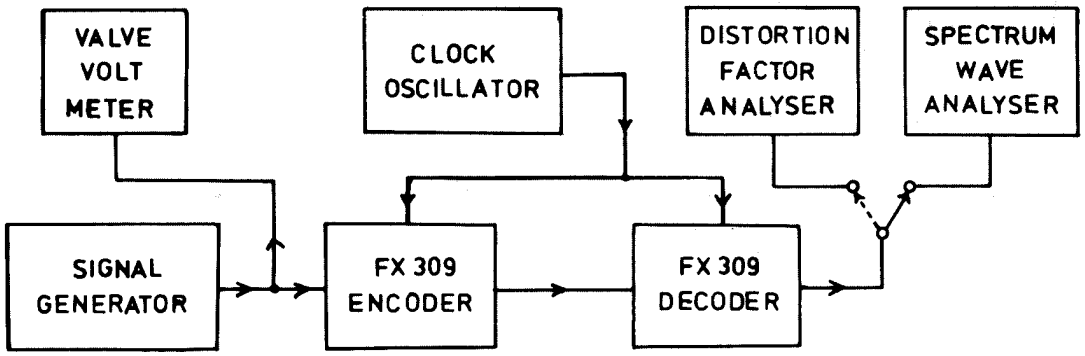
Capacitors (All rated at greater than 8V)

C1	1nF	±	2%	
C2a	0.33μF	±	5%	
C2b	0.33μF	±	5%	
Ct	10nF	±	20%	
Cin	0.047μF	±	20%	
C3	0.1μF	±	20%	(Supply Decoupling)

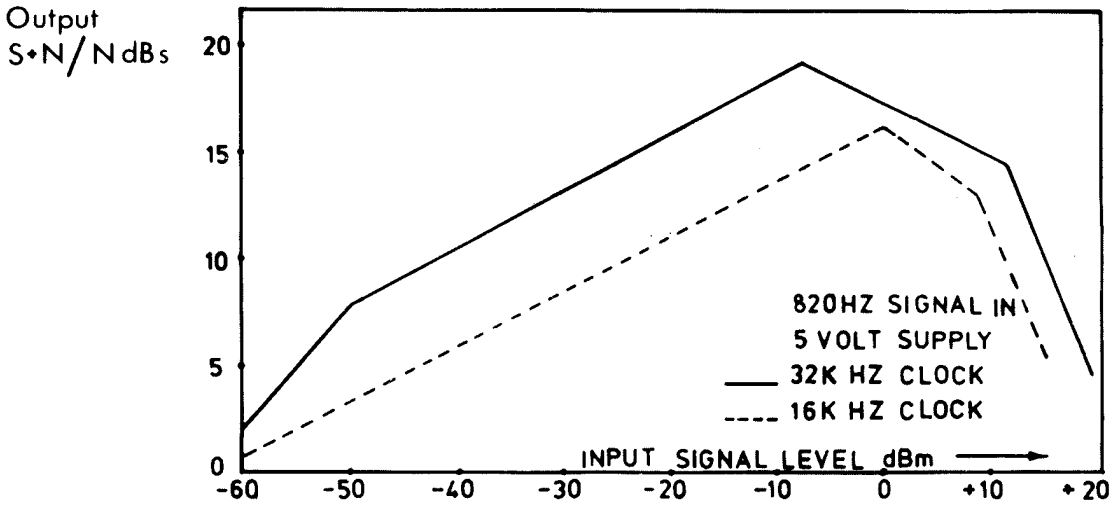
DESCRIPTION OF PIN FUNCTIONS

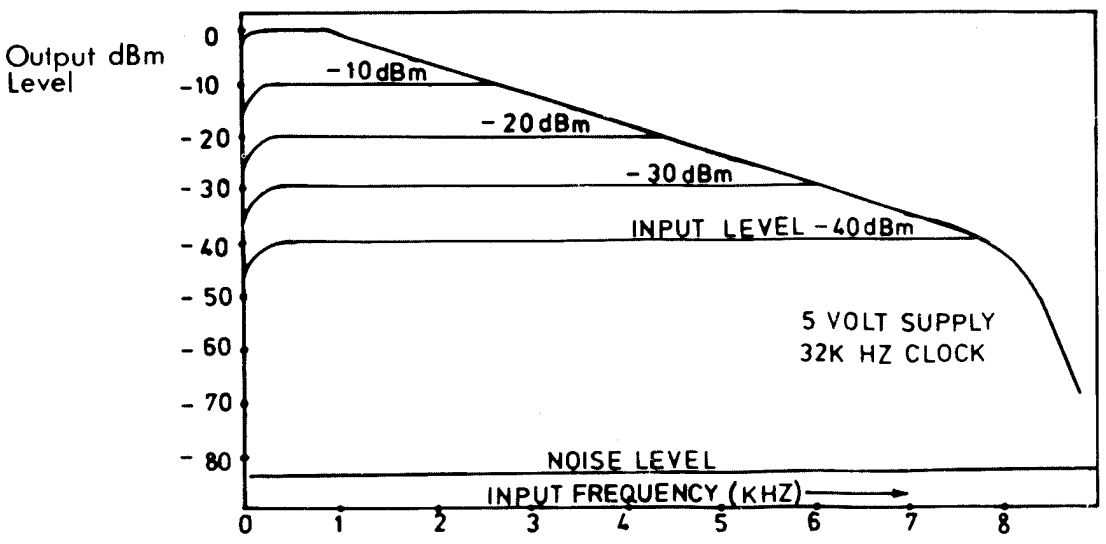
Pin No.	Function
1	**Clock input.** This clocks all internal functions.
2	**Three State Bias Output.** (on, off and open circuit) Provides feedback to bias the op-amp input. When two identical consecutive logic states are detected a corrective output is generated which when integrated over a long time and fed to the input of the op-amp, optimises the input biasing. Thus, it may be used to minimise idle channel noise. When two consecutive one's are detected it sinks current. When two consecutive zero's are detected it sources current.
3	**Positive Supply.**
4	**Inverter Input.**
5	**Inverter Output.** A standard inverter, can be used to provide inversion for any other part of the circuit, directly or via external components. As it is sometimes necessary to provide inversion in order to feed information back to the correct input of the op-amp.
6	**Positive Compand Output.**
7	**Discharge Compand Output.**
8	**Negative Compand Output.** These provide the compand facility, when connected to a few external components. Normally operates with pins 7 and 8 connected. When three identical consecutive logic states are detected, pin 6 sources current and pin 8 sinks current. When integrated, these outputs provide two voltages which can be fed back to the input of the op-amp via the pulse height modulator to provide rapid following of the signal level. When anything other than three identical consecutive logic states are detected pins 6 and 8 are disconnected from the supplies and pin 6 is connected to pin 7 which is normally used to permit the two voltages to equalise at a rate defined by the external components.
9	**Negative Step Height Input.**
10	**Pulse Height Modulator Output** – and is switched to the relevant compand output depending on the last logic state.
11	**Positive Step Height Input.** These switches are used in conjunction with the compand outputs, in order to generate the correct positive or negative going pulse, which when integrated, is fed back to the input of the op-amp when used as an encoder, or to produce the output of the decoder.
12	**Non-Inverting Input.**
13	**Inverting Input.** High gain differential amplifier. The signal to be modulated is applied to either input. It acts as a comparator between the signal and the local decoder outputs (i.e. the integrated form of pin 10 output) to produce a logic output which feeds the comparator and other outputs used for biasing.
14	**Analogue Bias Output.** This is the output of the differential amplifier in series with an analogue switch, which is switched by the clock such that it is closed when the clock is high and open when the clock is low. When integrated this can provide bias for the input of the amplifier.
15	**Negative Supply.**
16	**Digital Output.** This is the delta modulated output which comes directly from the first D - type of the compander. When integrated this will look like the input signal. Thus it may also be used in its integrated form to bias the input.

TEST ARRANGEMENT FOR MEASURING SIGNAL TO NOISE AND THE FREQUENCY RESPONSE



EQUIPMENT USED: SPECTRUM WAVE ANALYSER : HEWLETT PACKARD 3580A
DISTORTION FACTOR METER : MARCONI TF 2331A





CHARACTERISTICS OBTAINED USING THE COMPONENTS AS SHOWN IN FIGS 1 & 2