CML Semiconductor Products
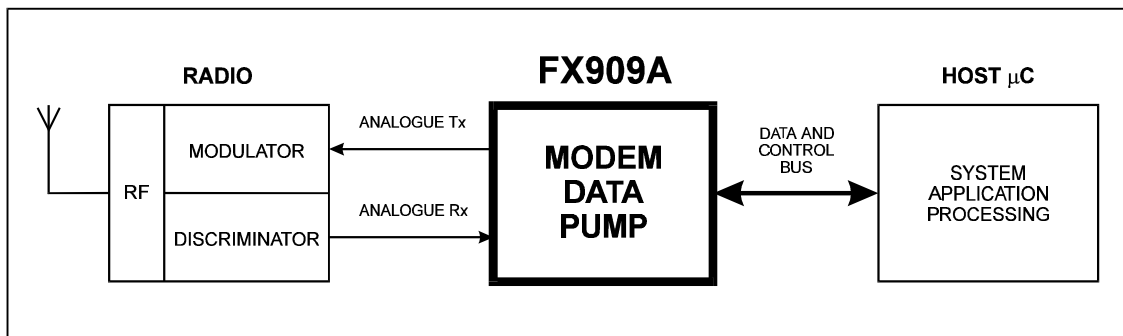
Wireless Modem Data Pump **FX909A**

1.0   Features

- **GMSK Modulation**

- **Rx or Tx up to 19.2k bits/sec**

- **Full Data Packet Framing**

- **Mobitex Compatible**

- **Flexible Operating Modes**

- **Host Processor Interface**

- **Low Power 3.3V/5V Operation**

- **24-Pin Small Form Package Option**

1.1   Brief Description

The FX909A is a CMOS integrated circuit that contains all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance GMSK Wireless Packet Data Modem. It interfaces with the modem host processor and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over the wireless link.

The FX909A assembles application data received from the processor, adds error correction code (FEC), adds error detection code (CRC), time-spreads this data by interleaving (burst-error protection) and scrambles (randomises) the bit pattern. After adding bit and frame sync codewords, it converts the packet into analogue GMSK signals for modulating the radio transmitter.

In receive mode, the FX909A performs the reverse function using the analogue signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the processor. Any residual uncorrected errors in the data will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The FX909A uses data block sizes and FEC/CRC algorithms compatible with the Mobitex Wide Area Network over-air standard. The format used is suitable for other private applications which require the high-speed transfer of data over narrow-band wireless links. The FX909A is programmable to operate at most standard bit-rates from a wide choice of Xtal/clock frequencies.

CONTENTS

1.2   Block Diagram

Figure 1 Block Diagram

1.3   Signal List

Package D2/D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
1	IRQN	O/P	A 'wire-ORable' output for connection to the host μC's Interrupt Request input. This output has a low impedance pull down to V_{SS} when active and is high impedance when inactive.
2	D7	BI	)
3	D6	BI	)
4	D5	BI	)
5	D4	BI	) 8-bit bidirectional 3-state μC interface data
6	D3	BI	) lines.
7	D2	BI	)
8	D1	BI	)
9	D0	BI	)
10	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the host μC.
11	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the host μC.
12	V_{SS}	Power	The negative supply rail (ground).
13	CSN	I/P	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
14	A0	I/P	) Two logic level modem register select
15	A1	I/P	) inputs.
16	XTALN	O/P	The output of the on-chip oscillator.
17	XTAL/CLOCK	I/P	The input to the on-chip oscillator, for external Xtal circuit or clock.
18	DOC 2	O/P	) Connections to the Rx level measurement
19	DOC 1	O/P	) circuitry. A capacitor should be connected) from each pin to V_{SS}.

Package D2/D5/P4	Signal		Description
Pin No.	**Name**	**Type**	
20	TXOP	O/P	The Tx signal output from the modem.
21	V_{BIAS}	O/P	A bias line for the internal circuitry, held at ½ V_{DD}. This pin must be decoupled to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	I/P	The input to the Rx input amplifier.
23	RXFB	O/P	The output of the Rx input amplifier and the input to the Rx filter.
24	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor.

Notes: I/P = Input
O/P = Output
BI = Bidirectional
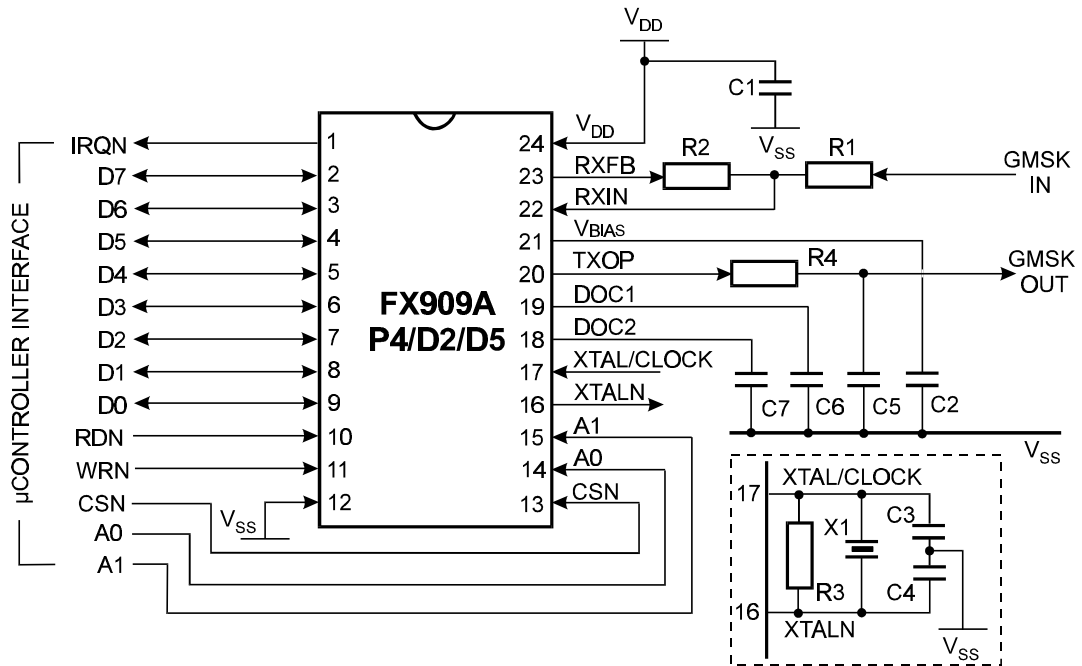
1.4   External Components

Figure 2 Recommended External Components

R1	See section 1.5.1.10	C1	0.1 µF	C5	See section 1.5.1.12
R2	100k ohm	C2	0.1 µF	C6	See note below
R3	1M ohm *	C3	See section 1.5.4.3 *	C7	See note below
R4	See section 1.5.1.12	C4	See section 1.5.4.3 *	X1	See section 1.5.4.3 *

* Refer also to 1.5.1.14

Tolerances: R4 ±5%
                      R2, C5 ±10%
                      all other components ±20%

C6 and C7 values should satisfy the following: C (in Farads) x data rate (bits/second) = 120×10^{-6}

e.g.

Data Rate (kbits/sec)	C6/C7 (nF)
4.0	30
4.8	22
8.0	15
9.6	12
16.0	6.8
19.2	6.8

1.5   General Description

This product has been designed to be compliant with the appropriate sections of the "Mobitex Interface Specification".

1.5.1   Description of Blocks

1.5.1.1   Data Bus Buffers

8 bidirectional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

1.5.1.2   Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs (WRN and RDN), the Chip Select input (CSN) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.
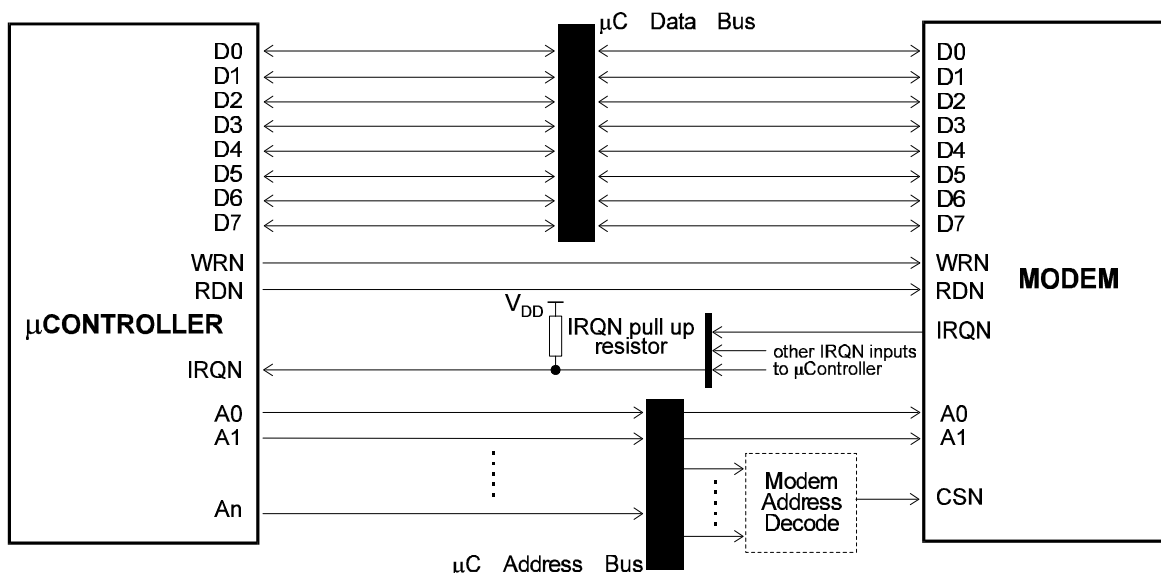
Figure 3 Typical Modem µC Connections

1.5.1.3   Status and Data Quality Registers

8-bit registers which the µC can read to determine the status of the modem and the received data quality.

1.5.1.4   Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

1.5.1.5   Data Buffer

An 18-byte buffer used to hold receive or transmit data to or from the µC.

1.5.1.6   CRC Generator/Checker
A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which are included in transmitted Mobitex data blocks so that the receive modem can detect transmission errors.

1.5.1.7   FEC Generator/Checker
In transmit mode this circuit calculates and adds the Forward Error Correction (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that have occurred in a Mobitex Data Block or in the Frame Head control bytes.

1.5.1.8   Interleave/De-interleave Buffer
This circuit interleaves data bits within a data block before transmission and de-interleaves the received data block so that the FEC system is best able to handle short noise bursts or signal fades.

1.5.1.9   Frame Sync Detect
This circuit, which is only active in receive mode, is used to look for the user specified 16-bit Frame Synchronisation pattern which is transmitted to mark the start of every frame.

1.5.1.10   Rx I/P Amp
This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give $0.2 \times V_{DD}$ pk-pk at the RXFB pin for a received '...11110000...' sequence.

A capacitor may be fitted if ac coupling of the received signal is desired (see section 1.6.4), otherwise the dc level of the received signal should be adjusted so that the signal at the modem's RXFB pin is centred around V_{BIAS} (½ V_{DD}).

1.5.1.11   Tx/Rx Low Pass Filter
This filter, which is used in both transmit and receive modes, is a low pass transitional Gaussian filter having a loss of 3dB at 0.3 times the selected bit rate (BT = 0.3). See Figure 4.

In transmit mode, the bits are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode this filter is used with an increased BT factor (0.56) to reject HF noise, so that the signal is suitable for extraction of the received data.

1.5.1.12   Tx Output Buffer
This is a unity gain amplifier used in transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 2 bit periods to prevent unwanted signals, from the low pass filter, at the output. When the modem is set to power save mode, the buffer is turned off and the TXOP pin connected to V_{BIAS} via a high value resistance. When exiting from power save mode the Tx output is only reconnected to the buffer after 2 bit periods, to prevent unwanted signals, from the low pass filter, at the output.

Note: The RC low pass filter formed by the external components R4 and C5 between the Tx Output Buffer and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The ground connection to the capacitor C5 should be positioned to give maximum attenuation of high frequency noise into the modulator. R4 and C5 should be chosen so that the product of the resistance of R4 (in Ohms) and capacitance of C5 (in Farads) is 0.34/bit rate (bit rate in bits per second). R4 should be not less than 47kΩ and the value used for the external capacitor should take into account parasitic capacitance.

Suitable values being:

	R4	C5
8000 bits/sec	100kΩ	430pF
4800 bits/sec	100kΩ	710pF

The signal at the TXOP pin is centred around V_{BIAS} and is approx 0.2 x V_{DD} pk-pk, going positive for a logic '1' and negative for a logic '0', if the modem is not inverting the Tx data.

A capacitor may be fitted if ac coupling of the input to the frequency modulator is desired, see section 1.6.4.

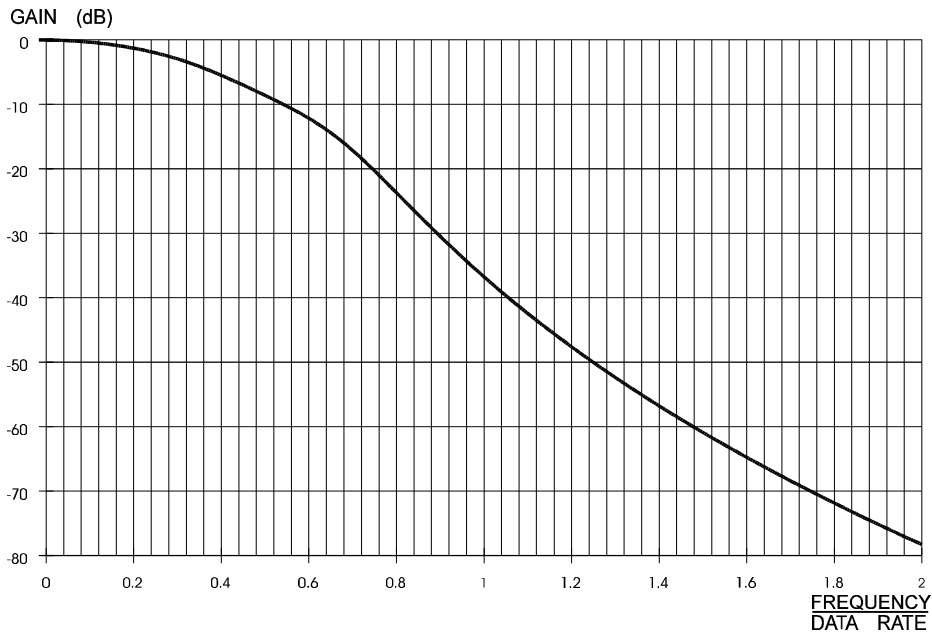The 'eye' diagram of the transmitted signal (after the external R4/C5 network) is shown in Figure 5.

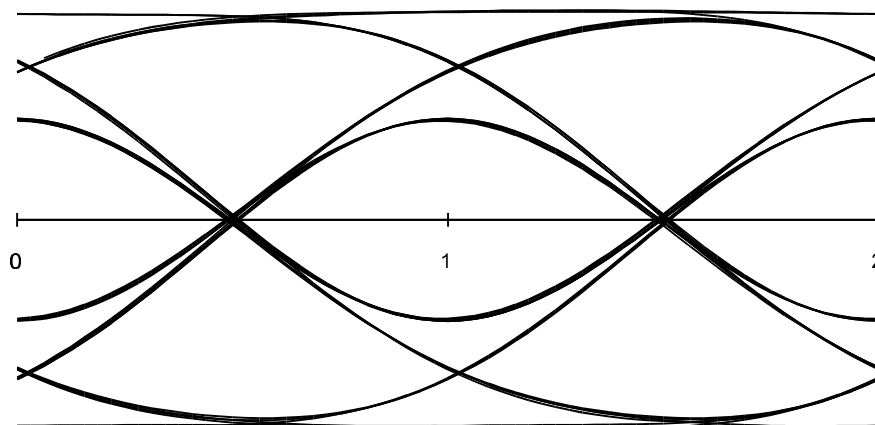**Figure 4 Typical Tx Filter Frequency Response (after the external RC filter)**

Figure 5 Transmitted Signal Eye Diagram (after the external RC filter)

1.5.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, extract a bit rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

1.5.1.14 Clock Oscillator and Dividers

This circuit derives the transmit bit rate (and the nominal receive bit rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the XTALN pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

1.5.1.15 Scramble/De-scramble

This block may be used to scramble/de-scramble the transmitted/received data blocks. It does this by modulating the data with a 511-bit pseudorandom sequence, as described in section 1.5.5.4. Scrambling smooths the transmitted spectrum, especially when repetitive sequences are to be transmitted.

1.5.2   Modem - µC Interaction

In general, data is transmitted over air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted data blocks. The Frame Head includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, Interleaving and Scrambling. Details of the message formats handled by this modem are given in section 1.5.3.

To reduce the processing load on the host µC, this modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) in searching for and synchronising onto the Frame Head. In normal operation the modem will only require servicing by the µC once per received or transmitted data block.

Thus, to transmit a block, the host µC has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with Forward Error Correction coding, interleave then scramble the bits before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct them (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data, to allow the transmission of special Bit and Frame Synchronisation sequences or test patterns.

1.5.3   Data Formats

General Purpose Formats
In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be sent as:

TQB (bit and frame sync) + TQB (addresses) + (n x TDB) + TSB

And received as:

SFS + RSB + RSB + RSB + RSB + (n x RDB)

Note that it is important to have established frame synchronisation before receiving data to enable the receiving device to decode synchronously. Also the user may add, by way of algorithms performed on the controlling device, additional data correction with the bytes in the data block task.

Mobitex Frame Structure
The Mobitex format for transmitted data is in the form of a Frame Head immediately followed by a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes:

   2 bytes of bit sync:
        1100110011001100 from base,
        0011001100110011 from mobile
        bits are transmitted from left to right

   2 bytes of frame sync:
        System specific.

   2 bytes of control data.

   1 byte of FEC code, 4 bits for each of the control bytes:
        bits 7-4 (leftmost) operate on the first control byte.
        bits 3-0 (rightmost) operate on the second control byte.

   Each byte in the Frame Head is transmitted bit 7 (MSB) first to bit 0 (LSB) last.

The Data Block consists of:

   18 bytes of data.

   2 bytes of CRC calculated from the 18 data bytes.

   4 bits of FEC code for each of the data and CRC bytes

   The resulting 240 bits are interleaved and scrambled before transmission.

Figure 6 shows how the over air signal is built up from Frame Sync and Bit Sync patterns, Control bytes and Data Blocks.

The binary data transferred between the modem and the host μC is that shown enclosed by the thick dashed rectangles near the top of the diagram.
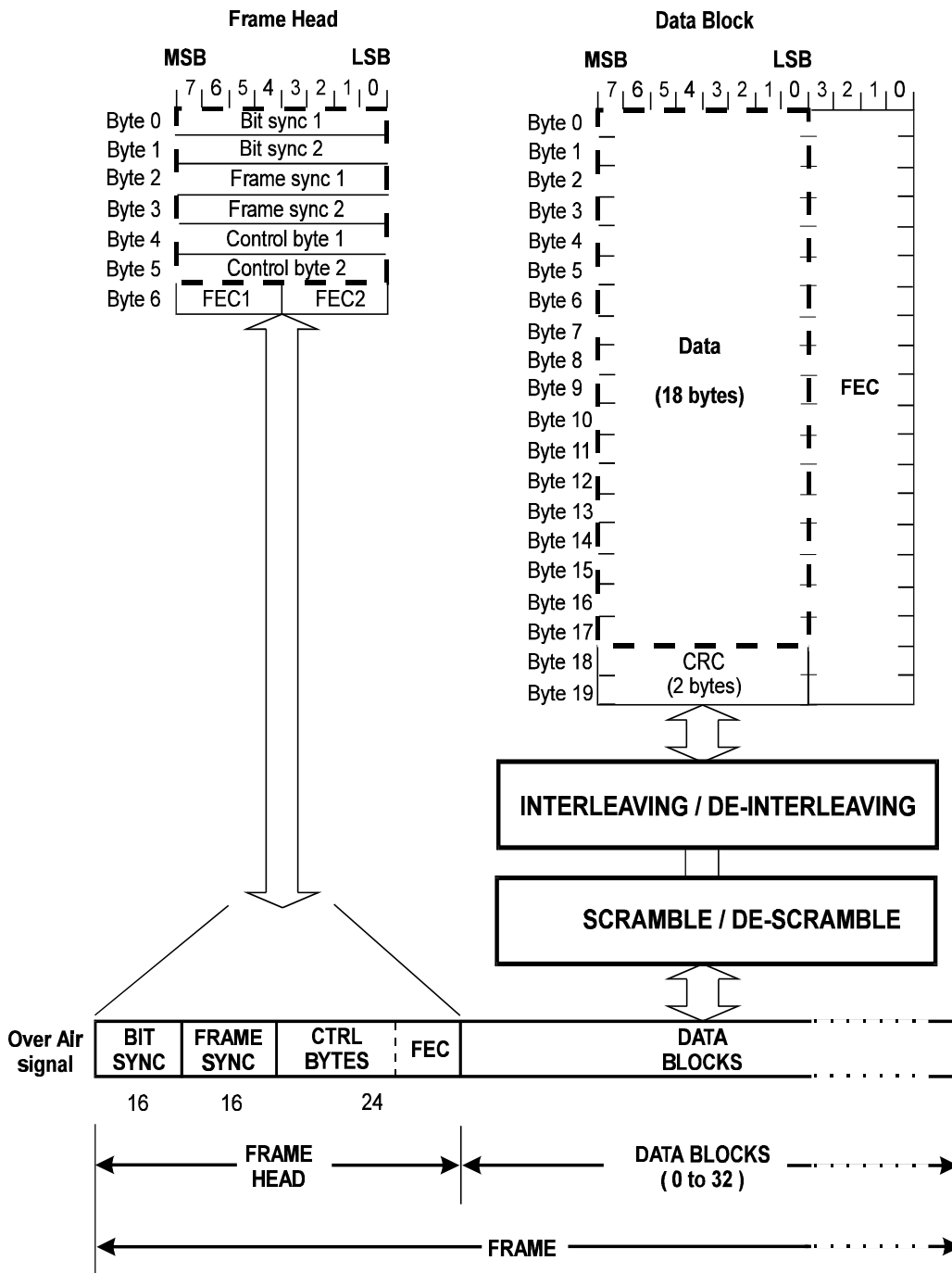

Figure 6 Mobitex Over Air Signal Format

1.5.4   The Programmer's View

The modem appears to the programmer as 4 write only 8-bit registers shadowed by 3 read only registers, individual registers being selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

1.5.4.1   Data Buffer
This is an 18-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality and control information) between the modem and the host μC.

It appears to the μC as a single 8-bit register; the modem ensuring that sequential μC reads or writes to the buffer are routed to the correct locations within the buffer.

The μC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode (except when loading Frame Sync detection bytes while in Rx mode).

1.5.4.2   Command Register
Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQBC bits.
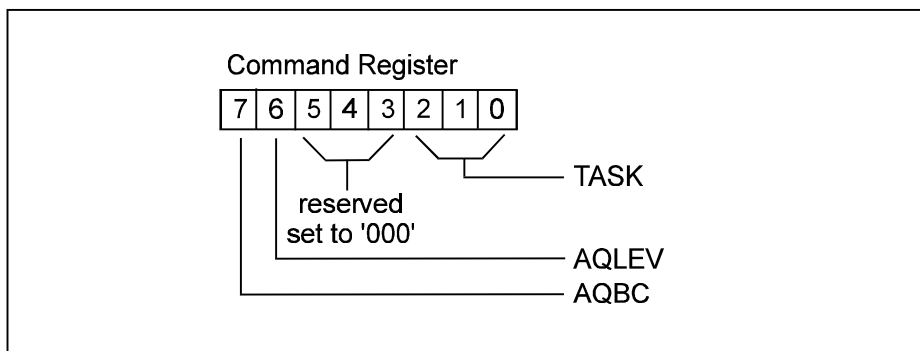
When it has no action to perform (but is not 'powersaved'), the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract bits from the received signal, supplying them to the de-interleave buffer, but will otherwise ignore the received data.

Command Register B7: AQBC - Acquire Bit Clock
This bit has no effect in transmit mode.

In receive mode, whenever a byte with the AQBC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve bit timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQBC bit set to '1'.

The AQBC bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the AQBC bit '0' if it is known that clock synchronisation does not need to be re-established. More details of the bit clock acquisition sequence are given in section 1.6.3.

Command Register B6: AQLEV - Acquire Receive Signal Levels
This bit has no effect in transmit mode.

In receive mode, whenever a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, hence improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels. More details of the level measurement acquisition sequence are given in section 1.6.3.

The error rate is highest immediately after a AQBC and AQLEV sequence is triggered and rapidly reduces to its static value soon after. These erroneous bits could incorrectly trigger the frame sync detection circuits and so it is suggested that a SFH or SFS task is set 12 bits after setting either of the AQLEV or AQBC sequences.

Command Register B5, B4, B3
These bits should be set to '0'.

Command Register B2, B1, B0: TASK - Task
Operations such as transmitting a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL, RESET and TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µC should wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE (Buffer Free) bit of the Status Register to '0'.

> Take the data from the Data Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

> Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

In this way the µC can write a task and the associated data to the modem while the modem is still transmitting the data from the previous task. See Figure 7.

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

> Set the BFREE bit of the Status Register to '0'.

> Wait until enough received bits are in the De-interleave Buffer.

> Decode them as needed, and transfer any resulting data to the Data Buffer

> Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the IRQN output to go low if the IRQNEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µC can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-interleave Buffer. See Figure 8.

The above is not true for loading the Frame Sync detection bytes (LFSB): the bytes to be compared with the incoming data must be loaded prior to the task bits being written.

Detailed timings for the various tasks are given in Figures 9 and 10.
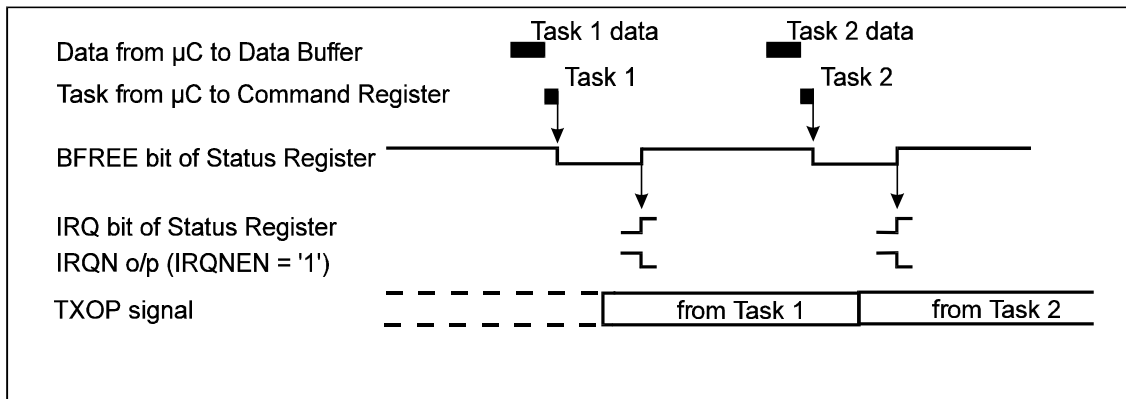
Figure 7 The Transmit Process
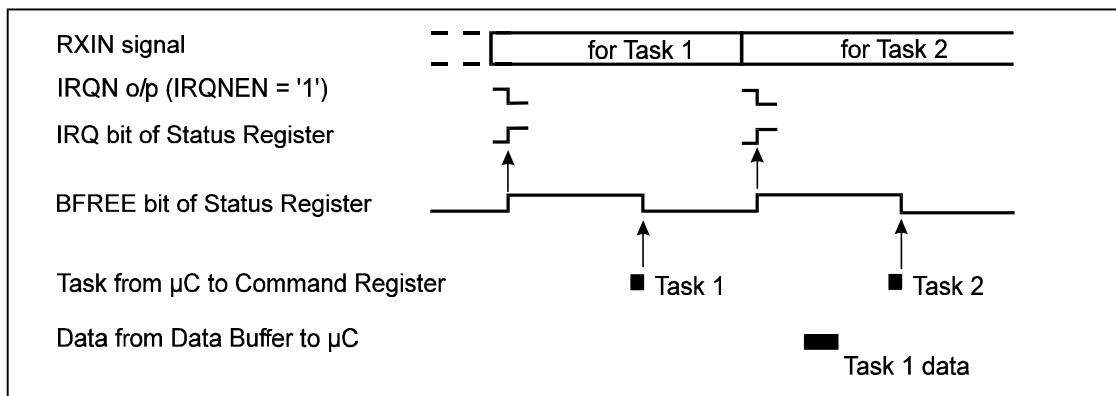
Figure 8 The Receive Process

Mobitex modem tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFH	Search for Frame Head	T7H	Transmit 7 byte Frame Head
0	1	0	R3H	Read 3 byte Frame Head		Reserved
0	1	1	RDB	Read Data Block	TDB	Transmit Data Block
1	0	0	SFS	Search for Frame Sync	TQB	Transmit 4 Bytes
1	0	1	RSB	Read Single Byte	TSB	Transmit Single Byte
1	1	0	LFSB	Load Frame Sync Bytes	TSO	Transmit Scrambler Output
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

NULL - No effect
This task is provided so that a AQBC or AQLEV command can be initiated without loading a new task.

SFH - Search for Frame Head
Causes the modem to search the received signal for a Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data (see Figure 6 - Mobitex Over Air Signal). The search will continue until a Frame Head has been found, or until the RESET task is loaded.

The search is carried out by first attempting to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error). When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes, these bytes will be checked, and corrected if necessary, using the FEC bits. The two Frame Head Data bytes are then placed into the Data Buffer.

The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µC may read the 2 Frame Head Data bytes from the Data Buffer and write the next task to the Command Register. If the FEC indicates uncorrectable errors the modem will set the CRCFEC bit in the Status Register to a logic '1'. The MOBAN bit (Mobile or Base) in the Status Register will be set according to the polarity of the 3 bits preceding the Frame Sync pattern.

R3H - Read 3-byte Frame Head
This task, which would normally follow an SFS task, will place the next 3 bytes directly into the Data Buffer. It also causes the modem to check the 3 bytes as Frame Head control data bytes and will set the CRCFEC bit to a logic '1' (high) only if the FEC bits indicate uncorrectable errors. Note: This task will not correct any errors and, due to the Mobitex FEC specification, will not detect all possible uncorrectable error patterns The BFREE and IRQ bits of the Status Register will be set to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register.

The CRCFEC bit in the Status Register will be set according to the validity of the received FEC bits.

RDB - Read Data Block
This task causes the modem to read the next 240 bits as a Mobitex Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 18 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: in receive mode the CRC checksum circuits are initialised on completion of any task other than NULL.

SFS - Search for Frame Sync
This task, which is intended for special test and channel monitoring purposes, performs the first part only of a SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the Frame Synchronisation pattern with up to any 1 bit in error.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' and update the MOBAN bit. The µC may then write the next task to the Command Register.

RSB - Read Single Byte
This task causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task.

LFSB - Load Frame Sync Bytes
This task takes 2 bytes from the Data Buffer and updates the Frame Sync detect bytes. The MSB of byte '0' is compared to the first bit of a received Frame Sync pattern and the LSB of byte '1' is compared to the last bit of a received Frame Sync pattern. This task does not enable Frame Sync detection.

Unlike other Rx tasks, the data buffer must be loaded before the task is issued and the task must only be issued 'between' received messages, i.e. before the first task for receiving a message and after the last data is read out of the data buffer.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task to the modem.

T7H - Transmit 7-byte Frame Head
This task takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes '4' and '5' then transmits the result as a complete Mobitex Frame Head.

Bytes '0' and '1' form the bit sync pattern, bytes '2' and '3' form the frame sync pattern and bytes '4' and '5' are the frame head control bytes. Bit 7 of byte '0' of the Data Buffer is sent first, bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TQB - Transmit 4 Bytes
This task takes 4 bytes of data from the Data Buffer and transmits them, bit 7 first.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TDB - Transmit Data Block
This task takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL.

TSB - Transmit Single Byte
This task takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first.

Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TSO - Transmit Scrambler Output
This task, intended for channel set-up, enables the scrambler and transmits its output.

When the modem has started the task the Status Register bits will not be changed and hence an IRQ will not be raised. The µC may write the next task and its data to the modem at any time and the scrambler output will stop when the new task has produced its first data.

RESET - Stop any current action
This task takes effect immediately, and terminates any current action (task, AQBC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied to set the modem into a known state.

Note that due to delays in the internal switched capacitor filter, it will take approximately 3 bit times for any change to become apparent at the TXOP pin.

Task Timings
The device should not be given a new task for at least 2 bit times after the following:

> Changing from powersave state to normal operation.
> Changing the Tx/Rx bit.
> Resetting or after power is applied to the device.

This is to ensure that the internal operation of the device is initialised correctly for the new task. Note that this only applies to the Command Register, the other registers may be accessed as normal.
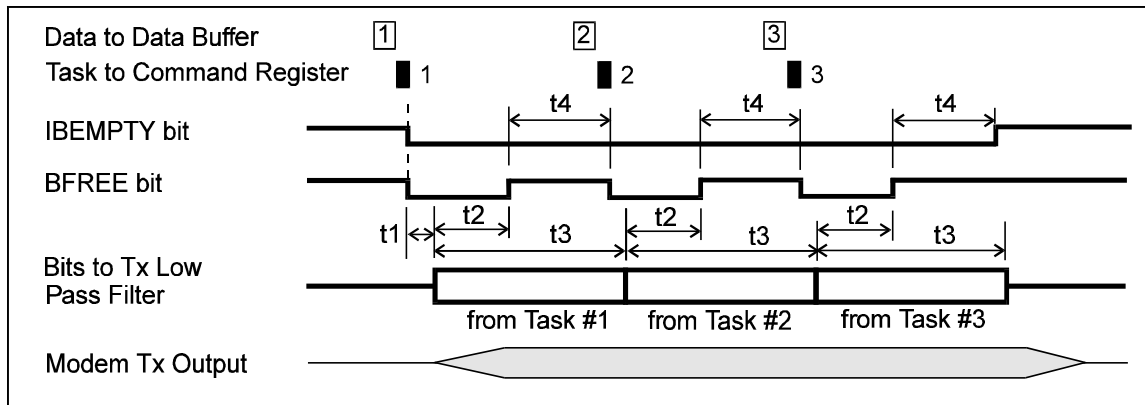
Figure 9 Transmit Mode Timing Diagram

		Task	Typical time (bit-times)
t1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t2	Time from application of first bit of task to Tx Low Pass filter until BFREE goes to a logic '1' (high).	T7H	36
		TQB	24
		TDB	20
		TSB	1
t3	Time to transmit all bits of task	T7H	56
		TQB	32
		TDB	240
		TSB	8
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T7H	18
		TQB	6
		TDB	218
		TSB	6
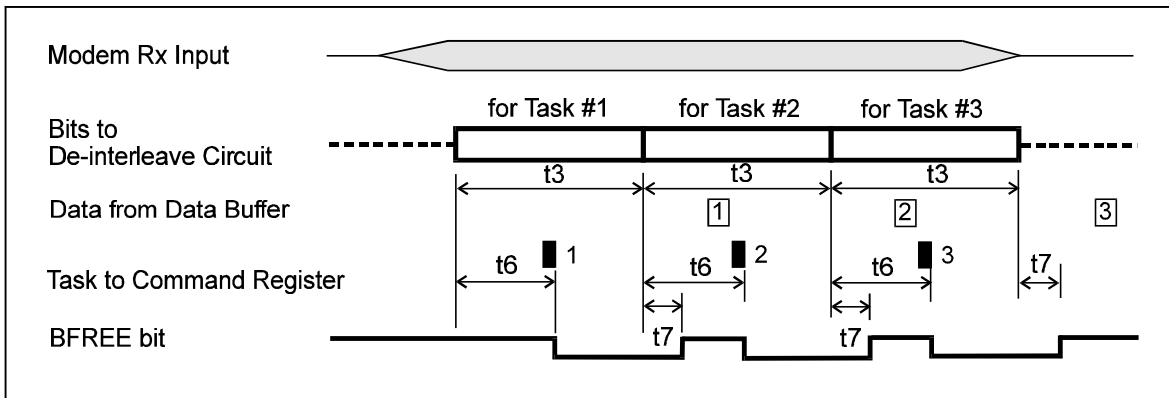
Figure 10 Receive Mode Timing Diagram

		Task	Typical time (bit-times)
t3	Time to receive all bits of task	SFH	56
		R3H	24
		RDB	240
		RSB	8
t6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem.	SFH	14
		R3H	18
		RDB	218
		RSB	6
t7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1' (high)	Any	1

Tx/Rx Low Pass Filter Delay
The previous task timing figures are based on the signal at the input to the Tx Low Pass filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 2 bit times in both transmit and receive modes due to the Tx/Rx Low Pass filter, as illustrated in Figure 11.
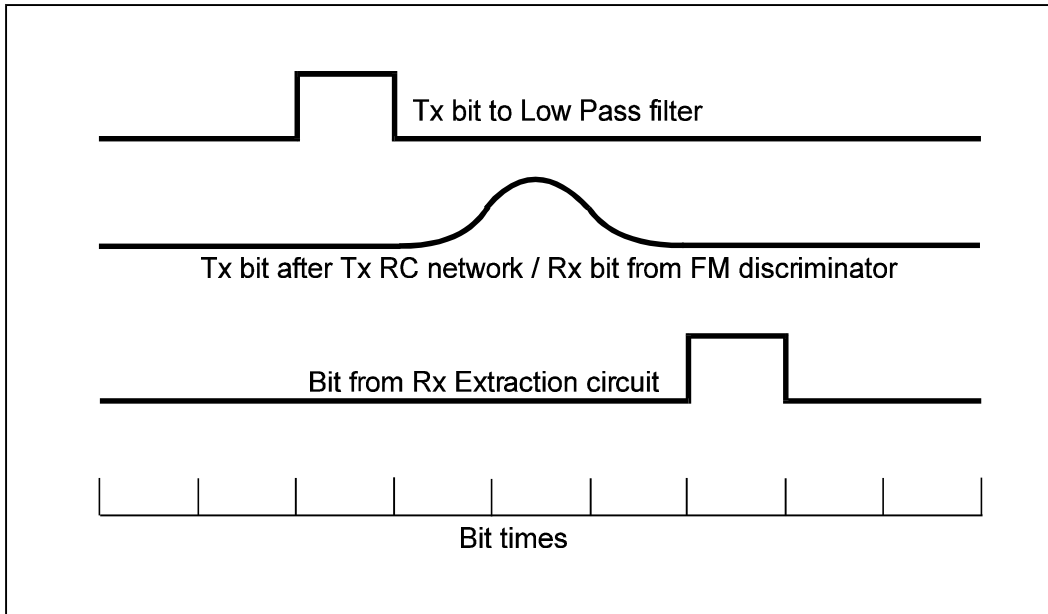
Figure 11 Low Pass Filter Delay

1.5.4.3   Control Register
This 8-bit write only register controls the modem's bit rate, the response times of the receive clock extraction and signal level measurement circuits and the internal analogue filters.
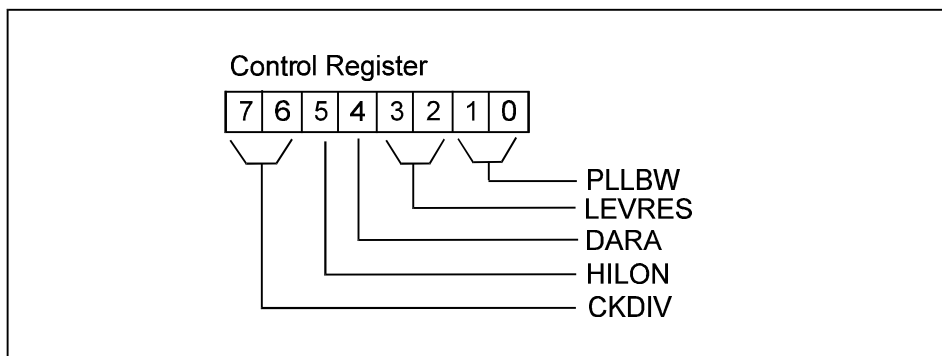
Control Register B7, B6: CKDIV - Clock Division Ratio and
B5: HILON - Xtal Range Selection

These bits control a frequency divider driven from the clock signal present at the XTALN pin, and hence determine the nominal bit rate. The table below shows how bit rates of 4000/8000/16000 or 4800/9600/19200 bits/sec may be obtained from common Xtal frequencies:

B5		Xtal/Clock Frequency (MHz)					
1		8.192	9.8304	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
	0	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)	1.024	1.2288

B7	B6	Division Ratio: Xtal Frequency / Data Rate		Data Rate (bits per second)					
0	0	256	128			16000	19200	8000	9600
0	1	512	256	16000	19200	8000	9600	4000	4800
1	0	1024	512	8000	9600	4000	4800		
1	1	2048	1024	4000	4800				

Note: Device operation is not guaranteed below 4000 or above 19200 bits/sec.

The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide; C3 = C4 = 33pF for X1 < 5MHz, and C3 = C4 = 18pF for X1 > 5MHz.

Control Register B4: DARA - Data Rate

This bit operates in both transmit and receive modes, optimising the modem's internal signal filtering according to the relevent bit rate.

If the bit rate used is above 10k bits/sec this bit should be set to '1' else it should be set to '0'.

Control Register B3, B2: LEVRES - Level Measurement Response Time

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' response time of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

B3	B2		
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detect
1	1	Lossy Peak Detect	Track input signal using lossy peak detection

For Mobitex systems, and most general purpose applications using the modem, these bits should normally be set to 'Peak Averaging', except when the μC detects a receive signal fade, when 'Hold' should be selected.

The 'Lossy Peak Detect' setting is intended for systems where the µC cannot detect signal fades or the start of a received message, as it allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note that, since the measured levels are stored on the external capacitors C6 and C7, they will decay gradually towards V_{BIAS} when the 'Hold' setting is chosen, the discharge time-constant being approximately 2000 bit times. More details of the level measurement system are given in section 1.6.3.

Control Register B1, B0: PLLBW
These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQBC command.

B1	B0	PLL Bandwidth	Suggested use
0	0	Hold	Signal fades
0	1	Narrow	± 20ppm or better Xtals
1	0	Medium	Wide tolerance Xtals or long preamble acquisition
1	1	Wide	Quick acquisition

The 'hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the transmit and receive modem bit rate tolerances should be chosen.

The wide and medium bandwidth settings are intended for systems where the µC cannot detect signal fades or the start of a received message, as they allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note: More details of the clock extraction system are given in section 1.6.3.

1.5.4.4   Mode Register
The contents of this 8-bit write only register control the basic operating modes of the modem:
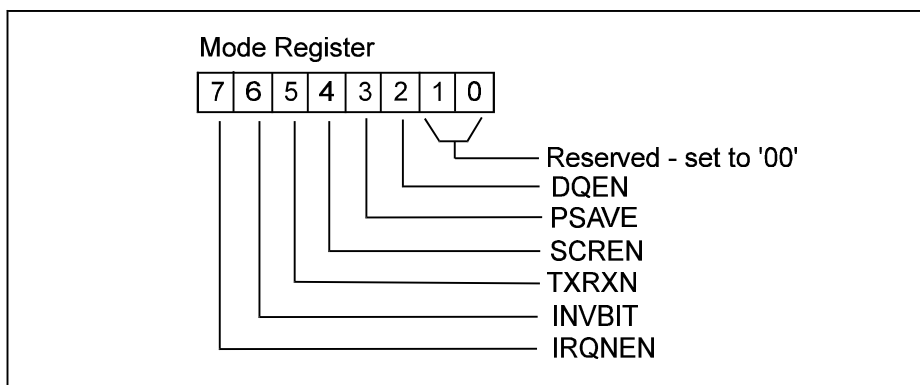
Mode Register B7: IRQNEN - IRQN Output Enable
When this bit is set to '1', the IRQN chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

Mode Register B6: INVBIT - Invert Bits
This bit controls inversion of transmitted and received bit voltages. When set to '1' all data is inverted in the Tx and Rx data paths so a transmitted '1' is a voltage below V_{BIAS} at the TXOP pin and a received '0' is a voltage above V_{BIAS} at the RXIN pin. Data will be inverted immediately after this bit is set to '1'.

Mode Register B5: TXRXN - Tx/Rx Mode
Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. When changing from Rx to Tx there must be a 2-bit pause before setting a new task to allow the filter to stabilise. (See also PSAVE bit).

Note that changing between receive and transmit modes will cancel any current task

Mode Register B4: SCREN - Scramble Enable
The scrambler only takes effect during the transmission or reception of a Mobitex Data Block and during a TSO task. Setting this bit to '1' enables scrambling, clearing it to '0' disables scrambling.

The scrambler is only operative, if enabled by this control bit, during TSO, RDB or TDB, it is held in a reset state at all other times.

This bit should not be changed while the modem is decoding or transmitting a Mobitex Data Block.

Mode Register B3: PSAVE - Powersave
When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx bit and Clock extraction circuits and the Tx o/p buffer will be disabled, and the TXOP pin will be connected to V_{BIAS} through a high value resistance. The Xtal Clock oscillator and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry. Note that the internal filters will take about 2 bit times to settle after the PSAVE bit is taken from '1' to '0'.

Mode Register B2: DQEN - Data Quality IRQ Enable
In receive mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new Data Quality reading is ready. (The DQRDY bit of the Status Register will also be set to '1' at the same time.)

In transmit mode this bit has no effect.

Mode Register B1, B0
These bits should be set to '0'.

1.5.4.5   Status Register
This register may be read by the µC to determine the current state of the modem.
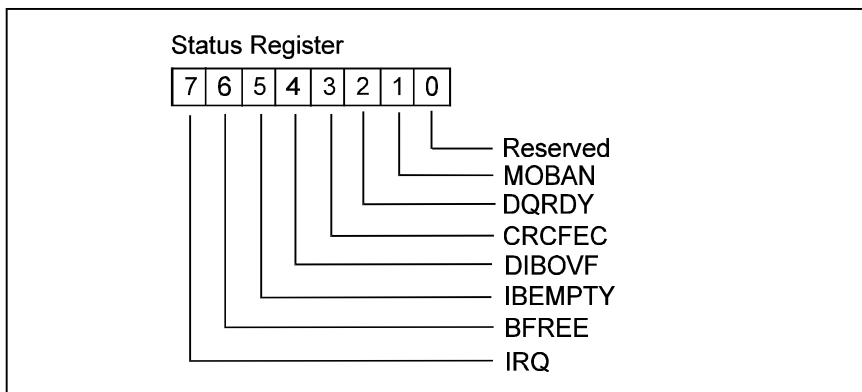
Status Register B7: IRQ - Interrupt Request
This bit is set to '1' by:

> The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register PSAVE or TXRXN bits.

> *or*   The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register PSAVE or TXRXN bits.

> *or*   The Status Register DQRDY bit going from '0' to '1' (If DQEN = '1').

> *or*   The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip IRQN output will be pulled low (to Vss) whenever the IRQ bit is '1'.

Status Register B6: BFREE - Data Buffer Free
This bit reflects the availability of the Data Buffer and is cleared to '0' whenever a task other than NULL, RESET or TSO is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1', but without setting the IRQ bit, by a RESET task or when the Mode Register PSAVE or TXRXN bits are changed.

Status Register B5: IBEMPTY - Interleave Buffer Empty
In transmit mode, this bit will be set to '1', also setting the IRQ bit, when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TXRXN or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' by writing a task other than NULL, RESET or TSO to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level voltage (V_{BIAS}) will be applied to the Tx low pass filter.

In receive mode this bit will be '0'.

Status Register B4: DIBOVF - De-Interleave Buffer Overflow
In receive mode this bit will be set to '1' (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' by reading the Status Register or by writing a RESET task to the Command Register or by changing the PSAVE or TXRXN bits of the Mode Register.

In transmit mode this bit will be '0'.

Status Register B3: CRCFEC - CRC or FEC Error
In receive mode this bit will be updated at the end of a Mobitex Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A '0' indicates that the CRC was received correctly or the FEC did not find uncorrectable errors, a '1' indicates that errors are present.

The bit is cleared to '0' by a RESET task or by changing the PSAVE or TXRXN bits of the Mode Register.

In transmit mode this bit will be '0'.

Status Register B2: DQRDY - Data Quality Reading Ready
In receive mode, this bit is set to '1' whenever a Data Quality reading has been completed. See section 1.5.4.6.

The bit is cleared to '0' by a read of the Data Quality Register.

Immediately after a RESET task, or a change in the PSAVE or TXRXN bits to '0', the DQRDY bit may be set and generate an interrupt. The value in the Data Quality Register will not be valid in this case.

Status Register B1: MOBAN - Mobile or Base Bit Sync Received
In receive mode this bit is updated at the end of the SFS and SFH tasks. This bit is set to '1' whenever the 3 bits immediately preceding a detected Frame sync are '011' (received left to right), with up to any one bit in error. The bit is set to '0' if the bit pattern is '100', again with up to any one bit in error. Thus, if this bit is set to '1' then the received message is likely to have originated from a Mobile and if it is set to '0' from a Base Station. See section 1.5.3.

In transmit mode this bit is a logic '0'.

Status Register B0
This bit will always be set to '0'.

1.5.4.6   Data Quality Register

This is intended to indicate the quality of the receive signal during a Mobitex Data Block or 30 single bytes. In receive mode, the modem measures the 'quality' of the received signal by comparing the actual received zero crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the DQRDY bit in the Status Register is updated. Note: An interrupt will only occur at this time if the DQEN bit = '1'.

To provide synchronisation with Data Blocks, and hence ensure the Data Quality Register is updated in preparation to be read when the RDB task finishes, the measurement process is reset at the end of tasks SFH, SFS, RDB and R3H.

In transmit mode all bits of the Data Quality Register will be '0'.

Figure 12 shows how the value (0-240) read from the Data Quality Register varies with received signal to noise ratio.
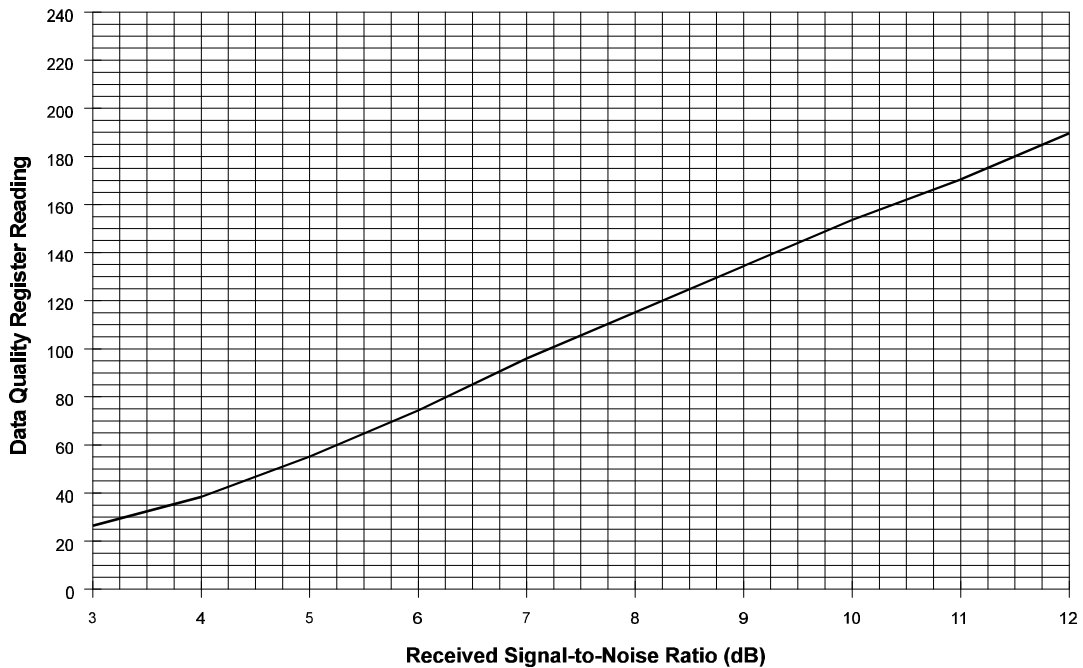
Figure 12 Typical Data Quality Reading (after 240 bits) vs S/N, (noise in bit rate bandwidth)

1.5.5   CRC, FEC, Interleaving and Scrambling Information

1.5.5.1   CRC

This is a 16-bit CRC code used in the Mobitex Data Block. In transmit it is calculated by the modem from the 18 data bytes using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

i.e.   CRC - CCITT X.25.

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC register is initialised to all '1s' and the CRC is calculated octet by octet starting with the least significant bit of 'byte 0'. The CRC calculated is bit-wise inverted and appended to the data bytes with the most significant bit transmitted earliest.

In receive mode, a 16-bit CRC code is generated from the 18 data bytes of each Mobitex Data Block as above and the bit-wise inverted value is compared with the received CRC bytes. If a mis-match is present, then an error has been detected.

1.5.5.2   FEC

In transmit mode, during T7H and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte. The FEC is defined by the following H matrix:

```
        7_____0    3___0

        11101100      1000
   H =  11010011      0100
        10111010      0010
        01110101      0001
```

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

In checking the FEC, the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble is all zero then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occurred.

This code can correct any single error that has occurred in each 12-bit (8 data + 4 FEC) section of the message.

Example:
If the byte to be coded is '00101100' then the FEC is derived as follows:

H matrix row:	1	2	3	4
A	11101100	11010011	10111010	01110101
B	00101100	00101100	00101100	00101100
A AND B	00101100	00000000	00101000	00100100
Even Parity:	1	0	0	0

where A is bits 7 - 0 of one row of the H matrix and B is the byte to be coded. The even parity bits apply to the result of 'A AND B'.

So the word formed will be: '00101100 1000' sent left to right

When the same process is carried out on these 12 bits as above, using all 12 bits of each H matrix row, the resulting 4 parity bits will be '0000'.

1.5.5.3   Interleaving
The 240 bits of a Mobitex Data Block are interleaved by the modem before transmission to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex Frame Head.

Considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 ('0' = bit 7 of byte 0, '11' = bit 0 of FEC for byte 0, ... ,'239' = bit 0 of FEC for byte 19 - see Figure 6), then they will be transmitted as shown in Figure 13.

The modem performs the inverse operation (de-interleaving) in receive mode on Mobitex Data Blocks.
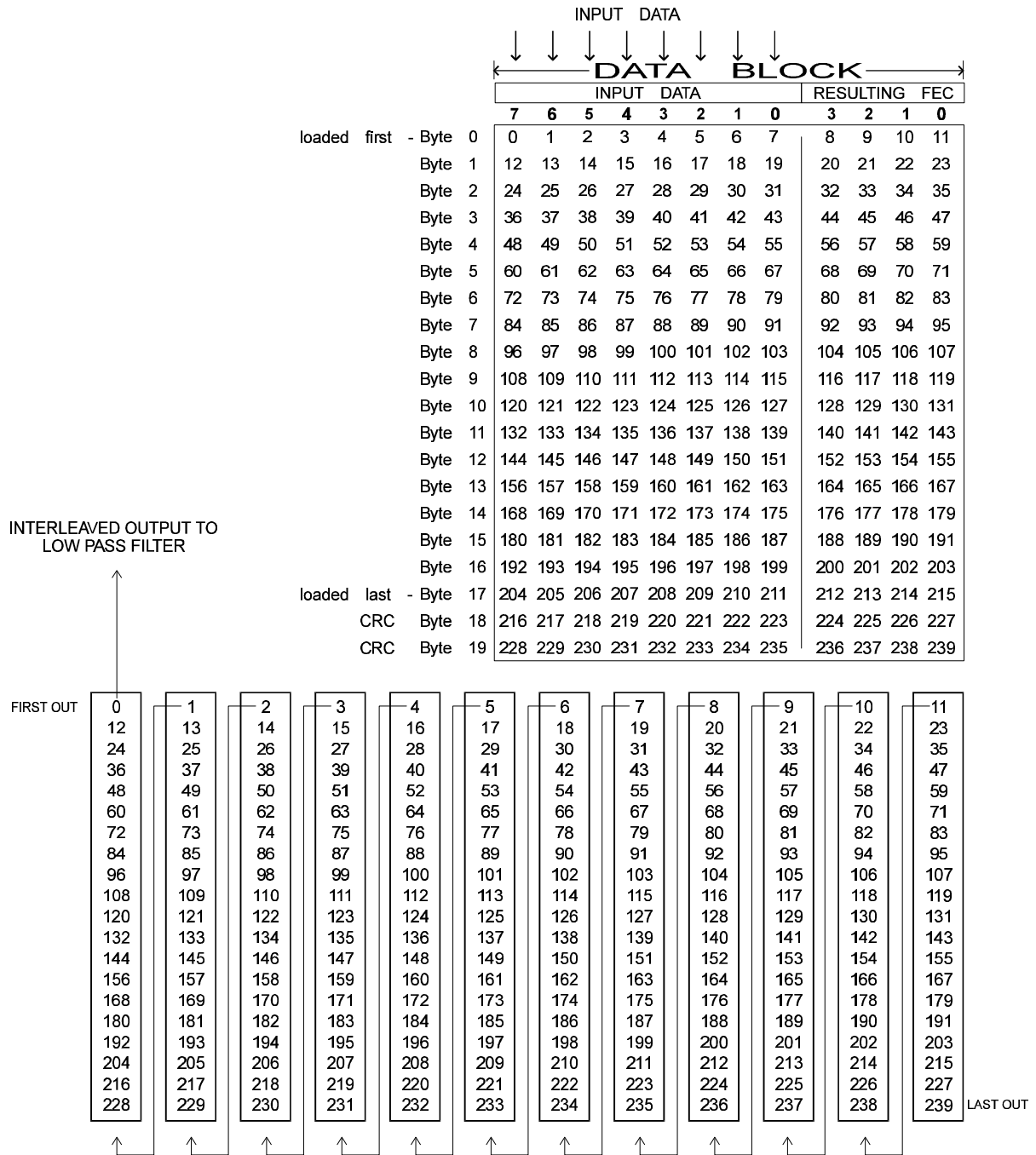
INPUT DATA → DATA BLOCK

		INPUT DATA								RESULTING FEC			
		7	6	5	4	3	2	1	0	3	2	1	0
loaded first - Byte 0		0	1	2	3	4	5	6	7	8	9	10	11
Byte 1		12	13	14	15	16	17	18	19	20	21	22	23
Byte 2		24	25	26	27	28	29	30	31	32	33	34	35
Byte 3		36	37	38	39	40	41	42	43	44	45	46	47
Byte 4		48	49	50	51	52	53	54	55	56	57	58	59
Byte 5		60	61	62	63	64	65	66	67	68	69	70	71
Byte 6		72	73	74	75	76	77	78	79	80	81	82	83
Byte 7		84	85	86	87	88	89	90	91	92	93	94	95
Byte 8		96	97	98	99	100	101	102	103	104	105	106	107
Byte 9		108	109	110	111	112	113	114	115	116	117	118	119
Byte 10		120	121	122	123	124	125	126	127	128	129	130	131
Byte 11		132	133	134	135	136	137	138	139	140	141	142	143
Byte 12		144	145	146	147	148	149	150	151	152	153	154	155
Byte 13		156	157	158	159	160	161	162	163	164	165	166	167
Byte 14		168	169	170	171	172	173	174	175	176	177	178	179
Byte 15		180	181	182	183	184	185	186	187	188	189	190	191
Byte 16		192	193	194	195	196	197	198	199	200	201	202	203
loaded last - Byte 17		204	205	206	207	208	209	210	211	212	213	214	215
CRC Byte 18		216	217	218	219	220	221	222	223	224	225	226	227
CRC Byte 19		228	229	230	231	232	233	234	235	236	237	238	239

INTERLEAVED OUTPUT TO LOW PASS FILTER

FIRST OUT

0	1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59
60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83
84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107
108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131
132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155
156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179
180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203
204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227
228	229	230	231	232	233	234	235	236	237	238	239

LAST OUT

Figure 13 Interleaving - Input/Output

1.5.5.4 Scrambling

All formatted bits of a Mobitex Data Block are passed through a 9-bit scrambler. This scrambler is initialised at the beginning of the first Data Block in every Frame. The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages XOR'ed and fed back to the input of the first stage. The scrambler is disabled during all other tasks, apart for TSO.

1.6   Application Notes

1.6.1   Transmit Frame Example
If the device is required to send a Mobitex Frame the following control signals and data should be issued to the modem, assuming the device is not starting from a powersave state, TXRXN is set to '1' and that SCREN, DARA, CKDIV, and DQEN have been set as required after power was applied to the device:

1. 6 bytes forming the Frame Head are loaded into the Data Buffer, followed by a 2-bit pause to let the filter stabilise, followed by setting T7H task.
2. Device interrupts host μC with IRQN when the 6th byte is read from the Data Buffer.
3. Status Register is read and 18 bytes are loaded, followed by setting TDB task.
4. Device interrupts host μC with IRQN when 18th byte is read from the Data Buffer.
5. Status Register is read, host may load data and set next task as required:

> GOTO '1'   if the last Data Block for this Frame has been transmitted
> and another Frame is to be immediately transmitted
> GOTO '3'   if another Data Block in this Frame is to be transmitted
> GOTO '6'   if no more data is to be immediately sent

6. 1 byte representing the 'hang byte' is loaded into the Data Buffer, followed by setting the TSB task.

If the 'hang byte' has been transmitted and no more data is to be sent then a new task need not be written and the μC can wait for the IBEMPTY interrupt when, after a few bits to allow for the Tx filter delay, it can shut down the Tx RF circuits.

A top level flowchart of the transmit process is shown in Figure 14.

Hang Byte
The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be smeared across 3 bit times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8-bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex frame are:

$$T7H + (n \times TDB) + TSB$$

When receiving this data, the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.
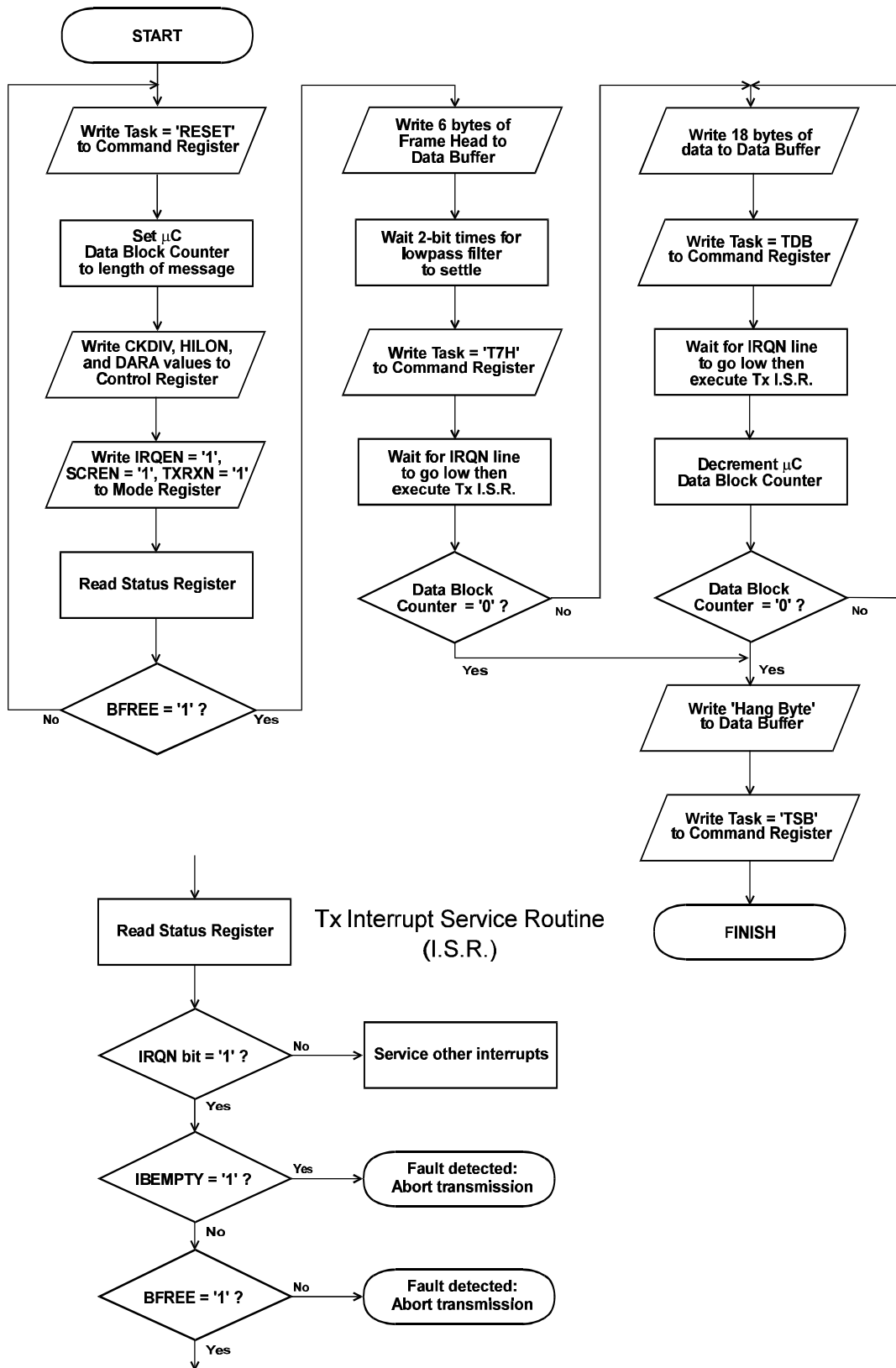
Figure 14 Transmit Process

1.6.2   Receive Frame Example

If the device is required to decode a Mobitex Frame the following control signals should be issued to the modem, assuming the device is initially not in powersave, PLLBW, LEVRES, SCREN are set as required, TXRXN bit is set to '0', the Frame Sync bytes have not been set and the carrier has been detected, or a Frame Head is imminently expected:

1. 2 Frame Sync bytes are loaded.
2. 2 bits after the carrier has been detected, a LFSB task is loaded, along with setting the AQLEV and AQBC bits, to initiate the level acquisition and bit clock extraction sequences.
3. Device interrupts host µC with IRQN when 2nd byte is read from Data Buffer.
4. Status Register is read, 12 bits later task is set to SFH to search for a Mobitex Frame Head.
5. Device will interrupt host µC with IRQN when valid Frame Sync is detected and header bytes decoded.
6. Host µC reads Status Register, checks MOBAN and CRCFEC bit and reads out 2 Frame Head control bytes.
7. Host µC sets the task to RDB to receive a Mobitex Data Block.
8. Device will interrupt host µC with IRQN when the Data Block has been received and the CRC has been calculated.
9. Host µC reads Status Register, checks CRC validity and reads 18 Data Block bytes. The Data Quality Register can also be read to obtain the received S/N level.
10. Host µC sets task if more information is expected:

> GOTO '4'   if last Data Block and another Frame Head imminently expected.
> GOTO '7'   if another Mobitex Data Block expected.

If the last Data Block has been decoded and no more information is expected then the task bits need not be set as the device will automatically select the idle state.

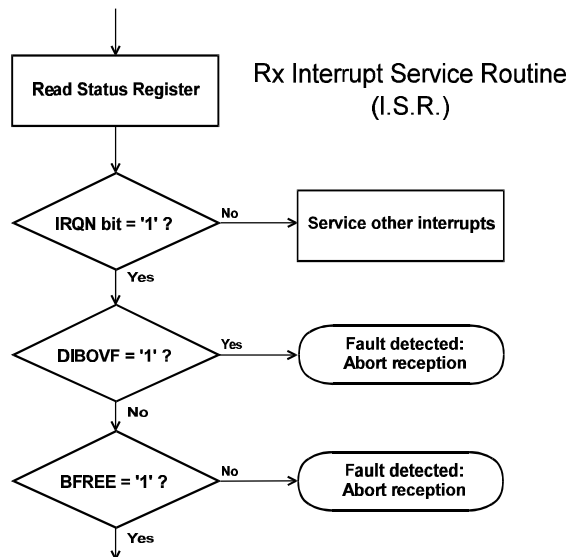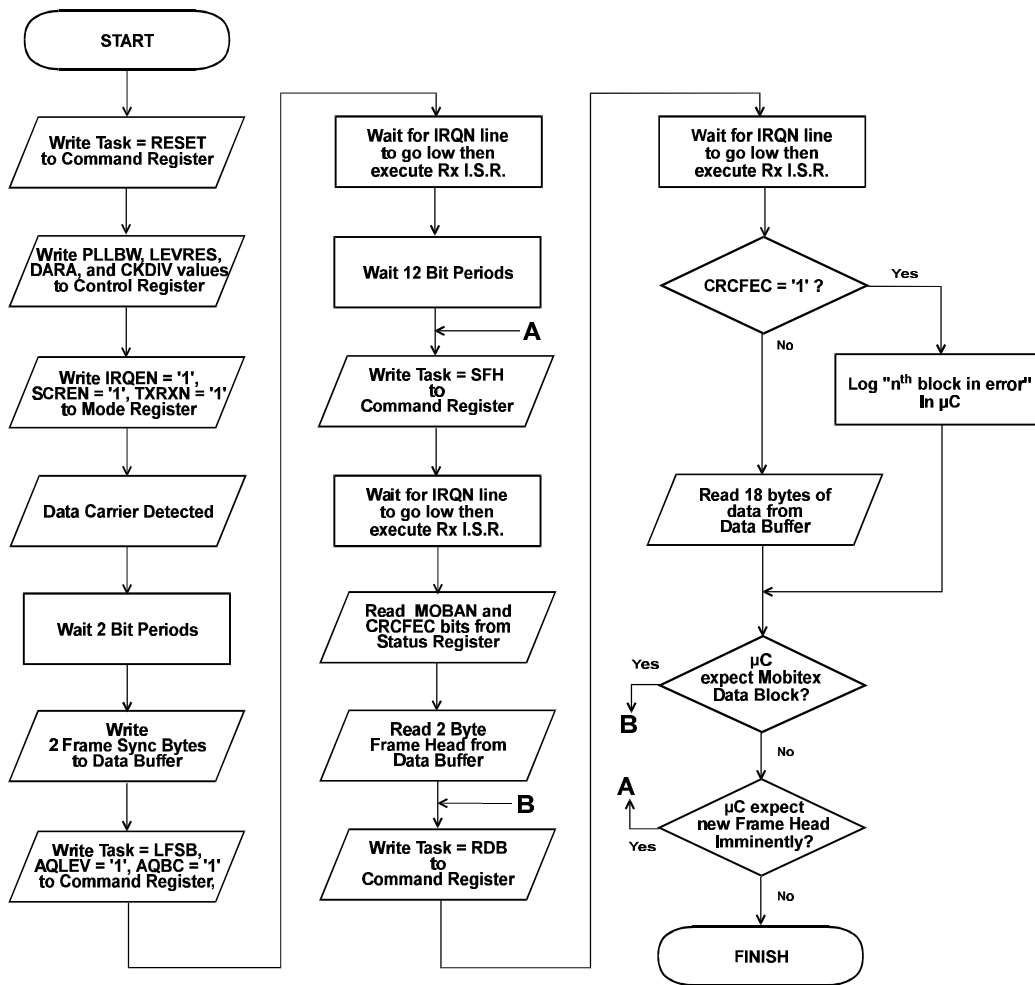A top level flowchart of the receive process is shown in Figure 15.

START

Write Task = RESET
to Command Register

Write PLLBW, LEVRES,
DARA, and CKDIV values
to Control Register

Write IRQEN = '1',
SCREN = '1', TXRXN = '1'
to Mode Register

Data Carrier Detected

Wait 2 Bit Periods

Write
2 Frame Sync Bytes
to Data Buffer

Write Task = LFSB,
AQLEV = '1', AQBC = '1'
to Command Register,

Wait for IRQN line
to go low then
execute Rx I.S.R.

Wait 12 Bit Periods

A

Write Task = SFH
to
Command Register

Wait for IRQN line
to go low then
execute Rx I.S.R.

Read MOBAN and
CRCFEC bits from
Status Register

Read 2 Byte
Frame Head from
Data Buffer

B

Write Task = RDB
to
Command Register

Wait for IRQN line
to go low then
execute Rx I.S.R.

CRCFEC = '1' ?   Yes

No

Log "n^{th} block in error"
In µC

Read 18 bytes of
data from
Data Buffer

Yes

µC
expect Mobitex
Data Block?

B

No

A

µC expect
new Frame Head
Imminently?   Yes

No

FINISH

Read Status Register

**Rx Interrupt Service Routine
(I.S.R.)**

IRQN bit = '1' ?   No   →   Service other interrupts

Yes

DIBOVF = '1' ?   Yes   →   Fault detected:
Abort reception

No

BFREE = '1' ?   No   →   Fault detected:
Abort reception

Yes

Figure 15 Receive Process

1.6.3 Clock Extraction and Level Measurement Systems

The modem needs to make accurate measurements of the received signal amplitude, dc offset and bit timing to achieve reasonable error rates. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time.

However, in most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts. Also, the received baseband signal out of the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and hence their 'carrier' frequencies.

To cater for this situation, AQBC and AQLEV (Acquire Bit Clock and Level) commands are provided which, when triggered, causes the modem to follow an automatic sequence designed to perform these measurements as quickly as possible.

The AQLEV sequence always starts with a measurement of the average signal voltage over a period of 1 bit time. The sequence continues by measuring the positive going and negative going peaks of the signal. The attack and decay times used in this 'Lossy Peak Detect' mode are such that a sufficiently accurate measurement can be made within 16 bits of a ' 1100 ...' pattern (i.e. the bit sync sequence) to allow the bit clock extraction circuits to operate.

If SFH or SFS is set within 28 bit times of AQLEV the device will switch to the Residual setting when Frame Sync is found. If a SFH or SFS task is not set then the Residual setting will be active 30 bits after AQLEV was set. The Residual setting is that programmed in the LEVRES bits and is either 'Lossy Peak Detect', 'Peak Detect', 'Peak Averaging' or 'Hold'. Note: For normal operation the LEVRES bits would only be set to 'hold' for the duration of a fade.

If SFH or SFS is set within 14 bit times of AQBC the device will switch to the Medium setting when Frame Sync is found. If a SFH or SFS task is not set then the Medium setting will be active 16 bits after AQBC was set. The PLLBW will change to the Residual setting 30 bits later.

The complete AQBC and AQLEV sequence is illustrated below, for the situation where the µC can detect the received carrier so that it knows when to issue the AQBC and AQLEV commands. Note that due to the delay through the Rx low pass filter, the AQBC and AQLEV sequences should not be started until about 2 bit times after the received carrier has been detected at the discriminator output. See Figure 16.

In a system where the host µC is not able to detect the received carrier, the AQBC and AQLEV sequences may be started at any time - possibly when no carrier is being received. However, in this case the clock and level acquisition will take longer since the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a dc offset. In this type of system, the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended - preferably by extending the Bit Sync sequence to 32 or even 48 bits.

Note that the clock extraction circuits work by detecting the timing of edges, i.e. a change from '0' to '1' or '1' to '0'. They will eventually fail if '1' or '0' is transmitted continuously. Similarly, the level measuring circuits require '00' and '11' bit pairs to be received at reasonably frequent intervals.

AQLEV Sequence

SFH or SFS is set up to 28 bits after AQLEV;
Frame Sync is being searched for:
   1 bit of clamp.
   Lossy Peak detect until Frame Sync is detected.
   Residual setting.

SFH or SFS is not set; Frame Sync is not being
searched for:
   1 bit of clamp.
   30 bits of Lossy Peak Detect.
   Residual setting.

AQBC Sequence

SFH or SFS is set up to 14 bits after AQBC;
Frame Sync is being searched for:
   'Wide' setting until Frame Sync detected.
   30 bits of 'Medium' setting.
   Residual setting.

SFH or SFS is not set; Frame Sync is not being
searched for:
   16 bits of 'Wide' setting.
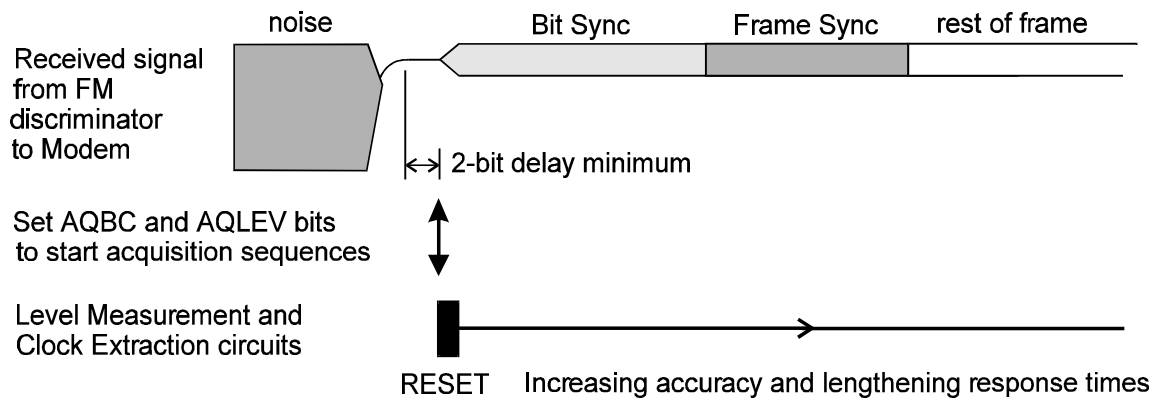   30 bits of 'Medium' setting.
   Residual setting.

Figure 16 Bit Clock and Level Acquisition Example

1.6.4   AC Coupling

For a practical circuit, ac coupling from the modem's transmit output to the Frequency Modulator and between the receiver's Frequency Discriminator and the receive input of the modem may be desired. There are, however, two problems.

Firstly, ac coupling of the signal degrades the Bit Error Rate performance of the modem. See Figure 17.
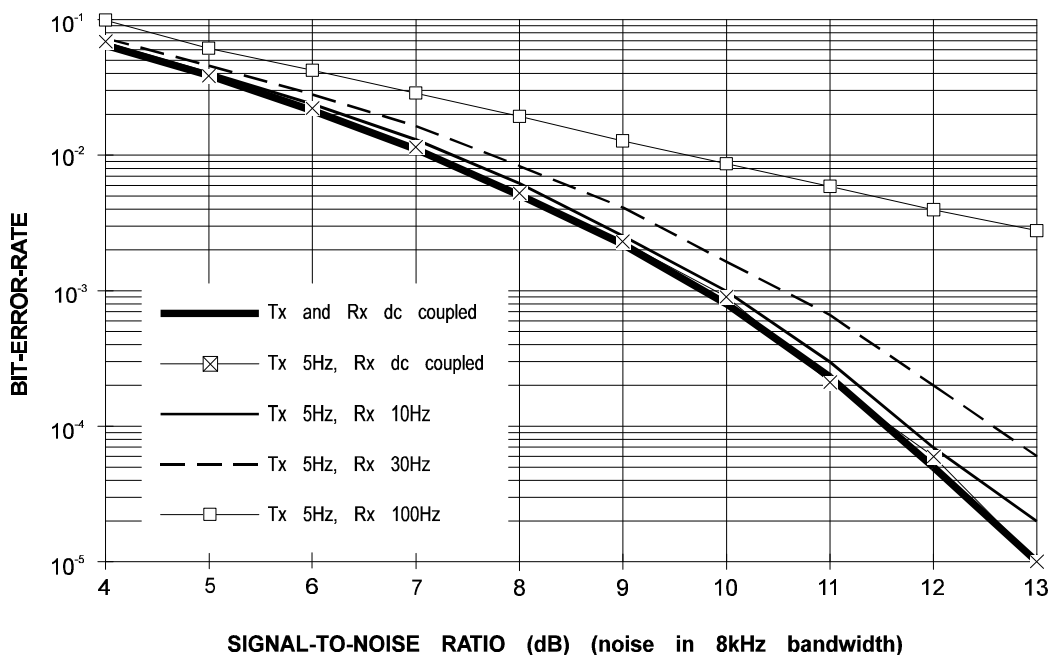
Figure 17 Typical Bit Error Rates (at 8kbits/sec, without FEC, for different degrees of ac coupling)

Secondly, any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated below, the time for this step to decay to 37% of its original value is 'RC' where

RC = $1/(2 \times \pi \times$ the 3dB cut-off frequency of the RC network)

and is 8 msec - or 64 bit times at 8kbits/sec for a 20Hz network. See Figure 18.
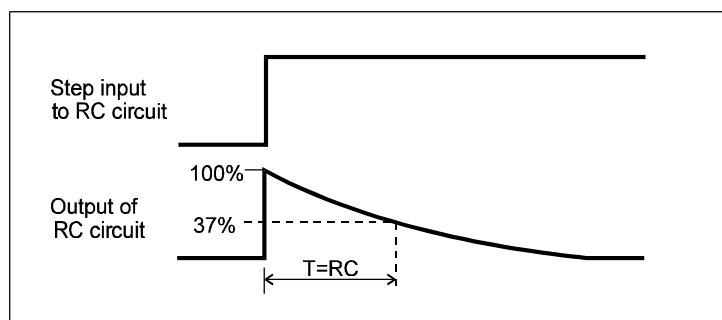

Figure 18 Decay Time - AC Coupling

For these reasons the maximum 3dB cut-off frequencies would seem to be around 5Hz in the Tx path and 20Hz in the Rx path at 8kbits/sec.

1.6.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Bit rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 8000 bits/sec can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2kHz peak for a repetitive ' 1100... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 1500Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye pattern, using the output of the frequency discriminator, gives a good indication of the overall transmitter/receiver performance.
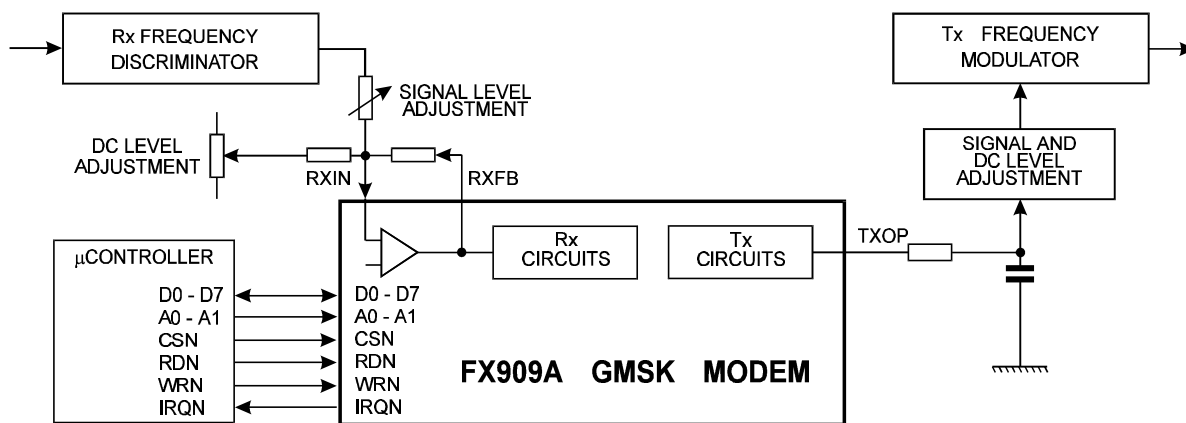

Figure 19 Typical System Installation

1.7   Performance Specification

1.7.1   Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

D5 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C
Xtal Frequency		1.0	10.0	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.096MHz, Bit Rate = 8k bits/sec, Noise Bandwidth = Bit Rate,
V_{DD} = 3.3V to 5.0V, Tamb = - 40°C to +85°C.

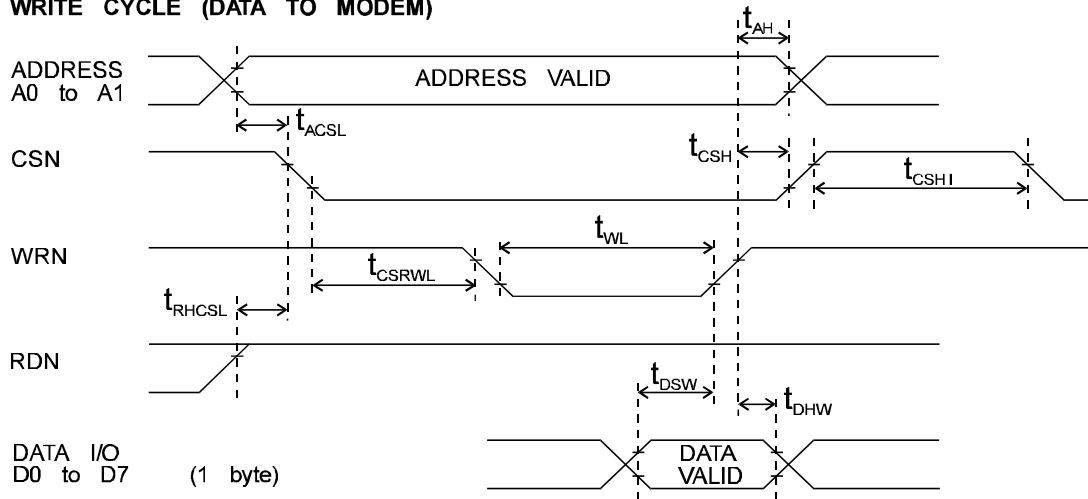|		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD} (not powersaved)	(V_{DD} = 3.3V)	1		2.2	3.3	mA
I_{DD} (powersaved)	(V_{DD} = 3.3V)	1		0.4	0.6	mA
I_{DD} (not powersaved)	(V_{DD} = 5.0V)	1		3	4.5	mA
I_{DD} (powersaved)	(V_{DD} = 5.0V)	1		0.9	1.4	mA
AC Parameters						
Tx Output						
TXOP Impedance (not powersaved)		2		1.0	2.5	kΩ
TXOP Impedance (powersaved)		2		300		kΩ
Signal Level		3	0.9	1.0	1.1	V pk-pk
Tx Data Delay		4		4	6	bits
Rx Input						
RXIN Impedance (at 100Hz)			10.0			MΩ
RXIN Amp Voltage Gain (I/P = 1mVrms at 100Hz)				500		V/V
Input Signal Level		5	0.7	1.0	1.3	V pk-pk
Rx Data Delay		6		3.5		bits
Xtal/Clock Input						
'High' Pulse Width		7	40			ns
'Low' Pulse Width		7	40			ns
Input Impedance (at 100Hz)			10.0			MΩ
Gain (I/P = 1mVrms at 100Hz)			20			dB
µC Interface						
Input Logic "1" Level		8, 9	70%			V_{DD}
Input Logic "0" Level		8, 9			30%	V_{DD}
Input Leakage Current (Vin = 0 to V_{DD})		8, 9	−5.0		+5.0	µA
Input Capacitance		8, 9		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)		9	90%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)		9,10			10%	V_{DD}
'Off' State Leakage Current (Vout = V_{DD})		10			10	µA

Notes:
1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.
3. For "1111000011110000.." bit sequence, at V_{DD} = 5.0V and Tamb = 25°C (output level is proportional to V_{DD}).
4. Measured between issuing first task after idle and the centre of the first bit at TXOP (See Figure 7, 'The Transmit Process').
5. For optimum performance, measured at RXFB pin, for a "...11110000..." bit sequence, at V_{DD} = 5.0V and Tamb = 25°C.
6. Measured between centre of last bit of an Rx single byte or Frame Sync at RXIN and an IRQ interrupt to the host µC.
7. Timing for an external input to the CLOCK/XTAL pin.
8. WRN, RDN, CSN, A0 and A1 pins.
9. D0 - D7 pins.
10. IRQN pin.

1.7.1   Electrical Performance (continued)

Timing Diagrams

WRITE CYCLE (DATA TO MODEM)
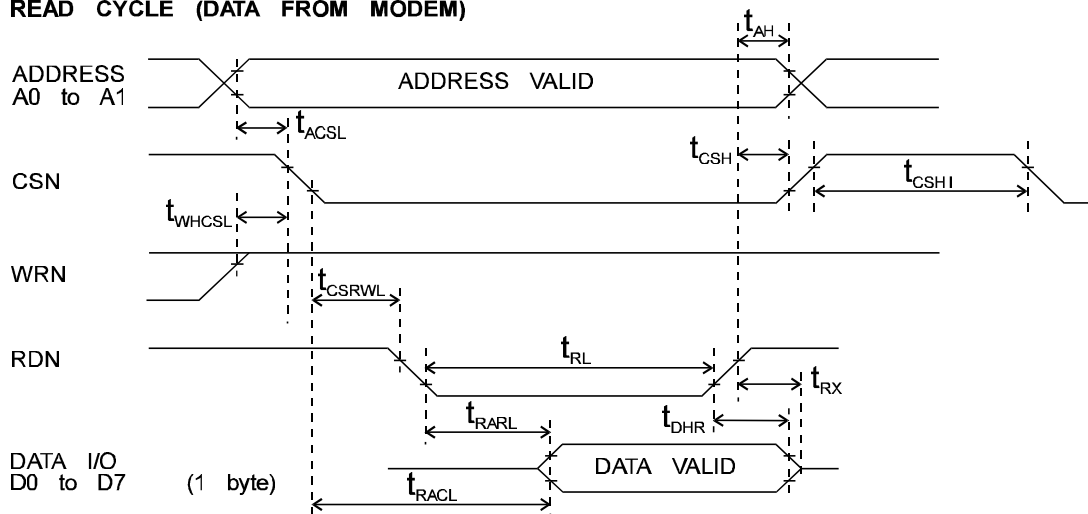

READ CYCLE (DATA FROM MODEM)

Figure 20 μC Parallel Interface Timings

For the following conditions unless otherwise specified:

Xtal Frequency = 4.096MHz, V_{DD} = 3.3V to 5.0V, Tamb = - 40°C to +85°C.

		Notes	Min.	Typ.	Max.	Units
μC Parallel Interface Timings (ref. Figure 20)						
t_{ACSL}	Address valid to CSN low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	CSN hold time		0			ns
t_{CSHI}	CSN high time	12	6			clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	RDN high to CSN low time (write)		0			ns
t_{RACL}	Read access time from CSN low	11			175	ns
t_{RARL}	Read access time from RDN low	11			145	ns
t_{RL}	RDN low time		200			ns
t_{RX}	RDN high to D0-D7 3-state time				50	ns
t_{WHCSL}	WRN high to CSN low time (read)		0			ns
t_{WL}	WRN low time		200			ns

Notes: 11. With 30pF max to V_{SS} on D0 - D7 pins.
              12. Xtal/Clock cycles at the XTAL/CLOCK pin.
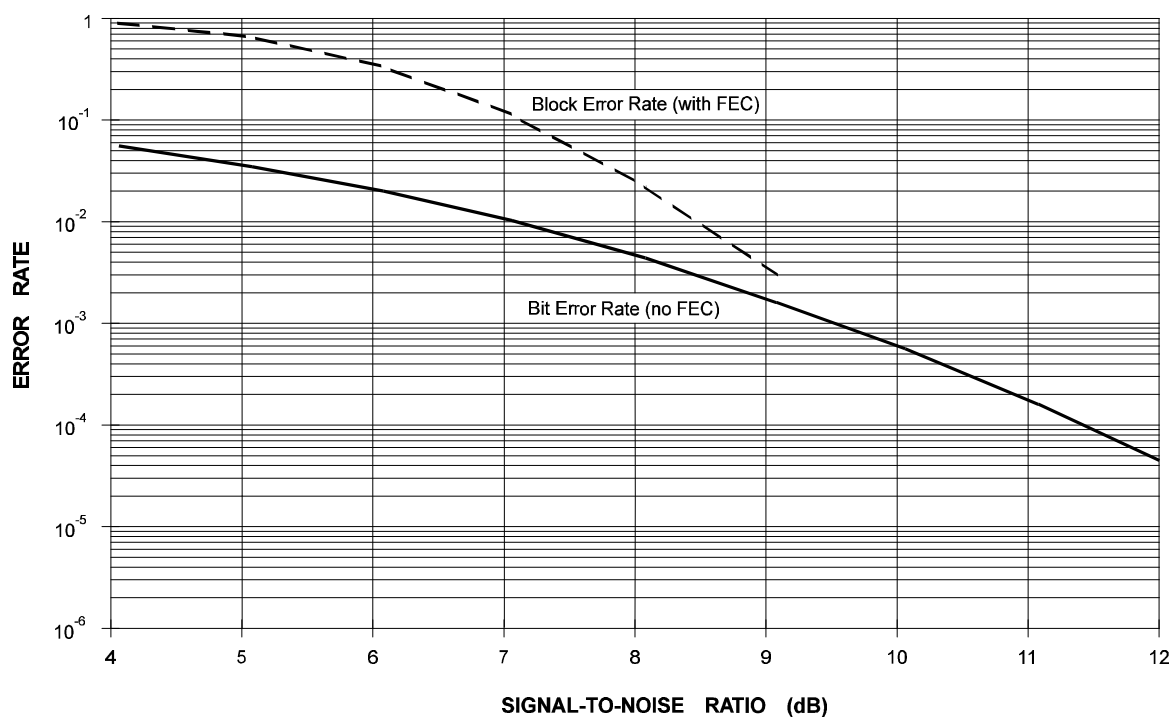
N.B. A block is deemed to be in error if the CRC fails.

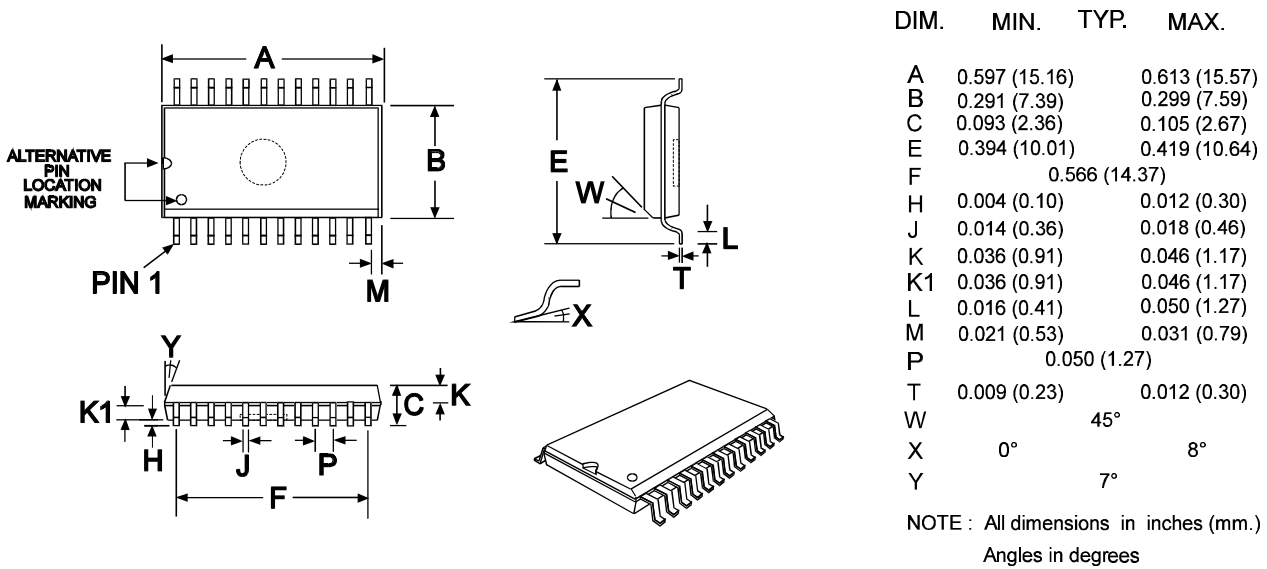**Figure 21 Typical Bit Error Rate (noise in bit rate bandwidth)**

1.7.2 Packaging

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)

Angles in degrees

Figure 22 D2 Mechanical Outline: *Order as part no. FX909AD2*

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)

Angles in degrees
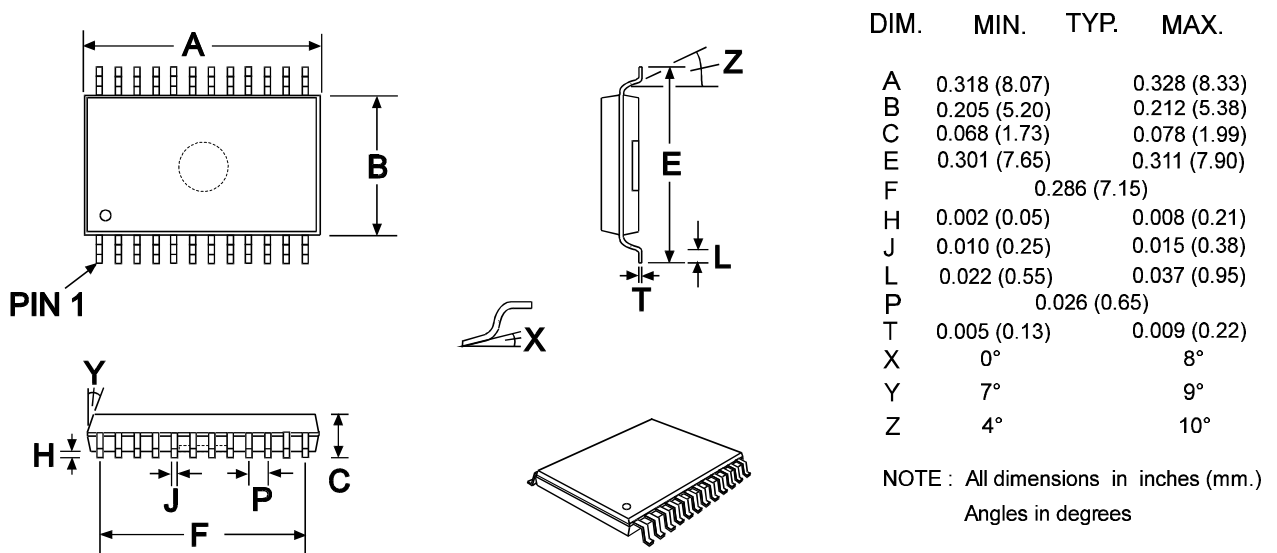
Figure 23 D5 Mechanical Outline: *Order as part no. FX909AD5*

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.552 (14.02)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.150 (3.81)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE : All dimensions in inches (mm.)
Angles in degrees
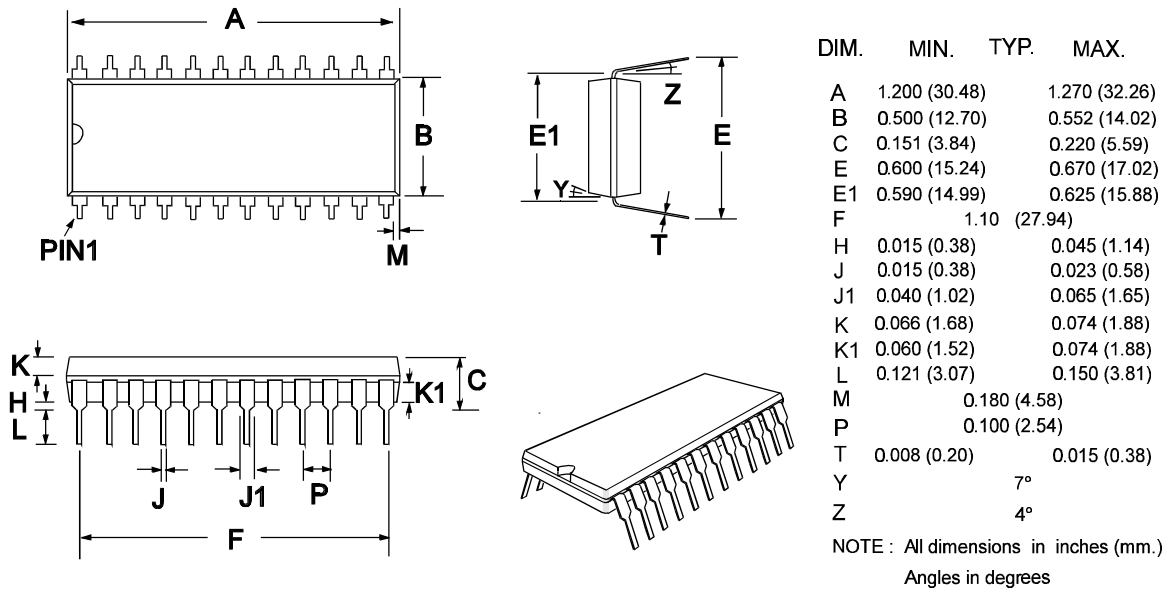
Figure 24 P4 Mechanical Outline: *Order as part no. FX909AP4*