RF133

RF/IF Transceiver For GSM Applications

The RF133 RF/IF Transceiver is a highly integrated, monolithic device optimized for use in GSM and other TDMA single-band or multi-band applications.

The receive path of the device consists of three Intermediate Frequency (IF) amplifiers with selectable gain, an I/Q demodulator, baseband filters, DC offset compensation circuitry, and selectable gain baseband amplifiers.

The transmit path of the device consists of an I/Q modulator and a frequency translation loop designed to perform frequency up-conversion with high output spectral purity. The translation loop consists of a phase/frequency detector, a charge-pump, a mixer, and buffers for the required isolation between the RF input, Local Oscillator (LO), and IF inputs.

The device package and pin configuration are shown in Figure 1. A block diagram of the RF133 is shown in Figure 2. The signal pin assignments and functional pin descriptions are found in Table 1.

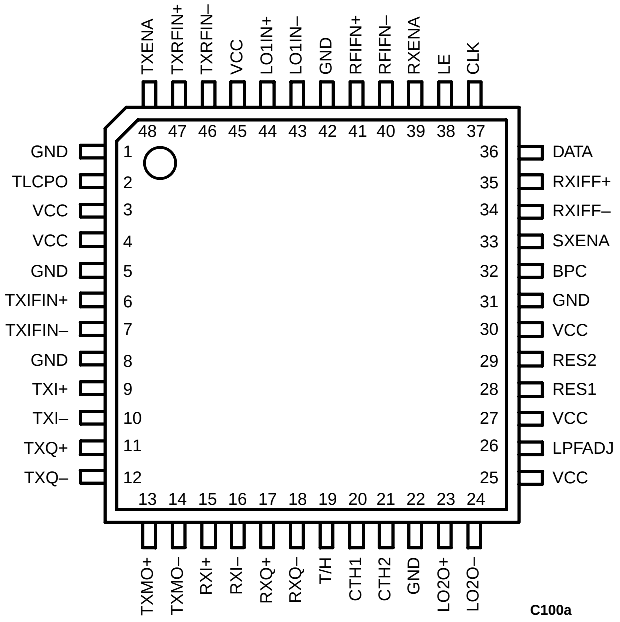


Figure 1. RF133 Pin Configuration – 48-pin TQFP

Features

- Quadrature demodulator for downconversion
- 80 dB IF gain range and 30 dB baseband gain range
- Integrated receive baseband filters with tunable bandwidth
- Integrated transmit path with high phase accuracy
- Reduced filtering requirements for the transmit path
- Broad RF and IF range for multi-band operation
- Integrated selectable local oscillator dividers/phase shifters and selectable high/low-side injection for frequency plan flexibility
- On-chip second local oscillator
- Separate enable lines for transmit, receive, and synthesizer modes for power management
- 48-pin Thin Quad Flat Pack (TQFP) package (7mm x 7mm)

Applications

- GSM900/DCS1800/PCS1900 digital cellular telephony
- Multi-mode, multi-band terminals

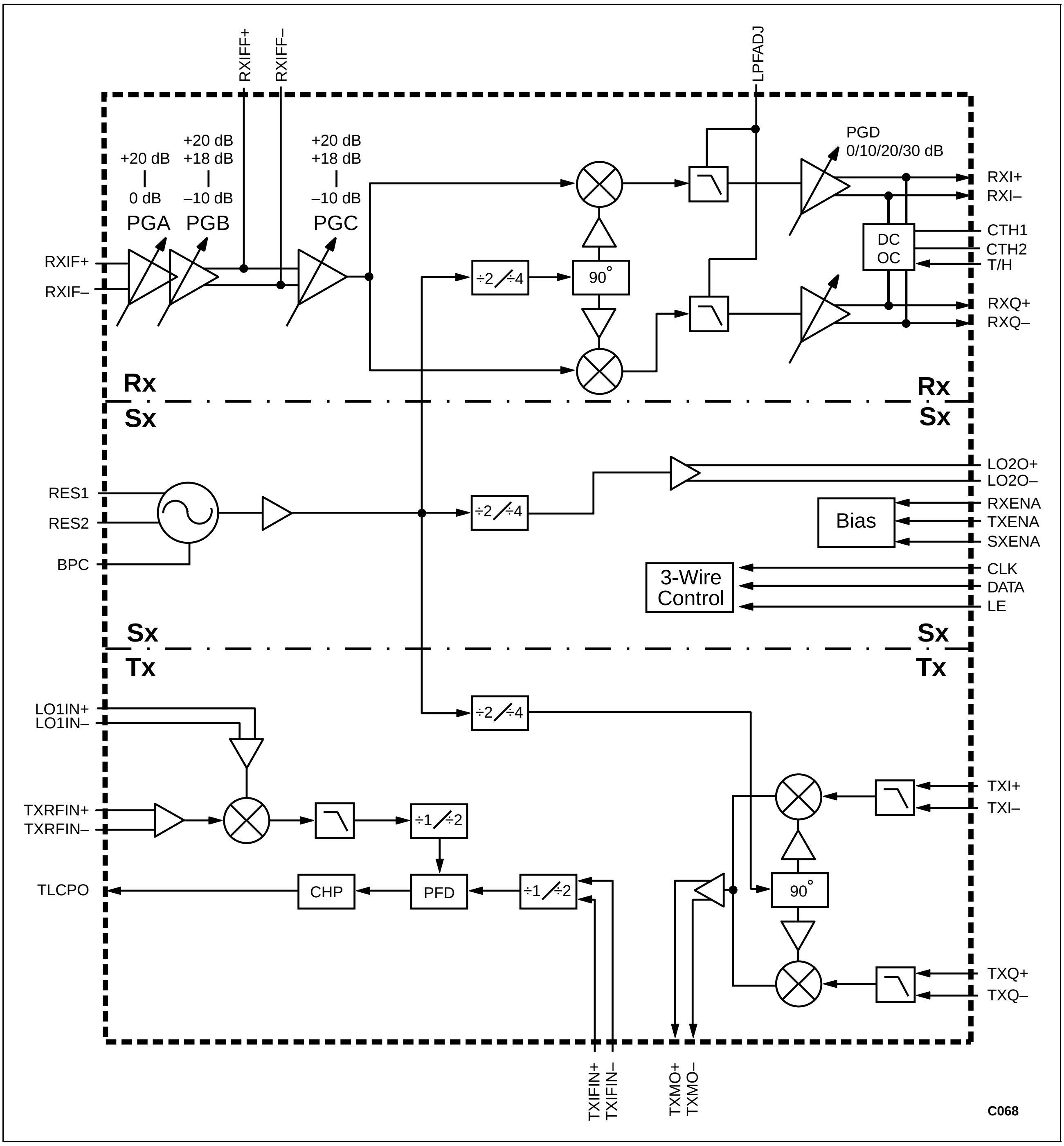


Figure 2. RF133 Block Diagram

Table 1. RF133 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground (Tx phase detector/charge pump)	25	VCC	Supply (2nd LO output buffers)
2	TLCPO	Translation loop charge pump output	26	LPFADJ	Adjustment pin for baseband low pass filter corner frequency
3	VCC	Supply (phase detector and charge pump)	27	VCC	Supply (2nd LO)
4	VCC	Supply (Tx modulator, Rx baseband sections)	28	RES1	Resonator pin
5	GND	Ground (Tx modulator, Rx baseband sections)	29	RES2	Resonator pin
6	TXIFIN+	Tx IF input	30	VCC	Supply (2nd LO)
7	TXIFIN–	Tx IF input	31	GND	Ground (2nd LO)
8	GND	Ground	32	BPC	Bypass capacitor
9	TXI+	Tx modulator input	33	SXENA	Synthesizer enable
10	TXI–	Tx modulator input	34	RXIFF–	Rx IF filter pin
11	TXQ+	Tx modulator input	35	RXIFF+	Rx IF filter pin
12	TXQ–	Tx modulator input	36	DATA	Data input
13	TXMO+	Tx modulator output	37	CLK	Clock input
14	TXMO–	Tx modulator output	38	LE	Latch enable input
15	RXI+	Rx baseband output	39	RXENA	Receiver enable
16	RXI–	Rx baseband output	40	RXIFIN–	Rx IF input
17	RXQ+	Rx baseband output	41	RXIFIN+	Rx IF input
18	RXQ–	Rx baseband output	42	GND	Ground (Tx mixer, Rx IF sections)
19	T/H	Track and hold signal	43	LO1IN–	1st local oscillator input
20	CTH1	Capacitor for track and hold	44	LO1IN+	1st local oscillator input
21	CTH2	Capacitor for track and hold	45	VCC	Supply (Tx mixer, Rx IF sections)
22	GND	Ground (2nd LO output buffers)	46	TXRFIN–	Transmit RF input
23	LO2O+	2nd local oscillator output	47	TXRFIN+	Transmit RF input
24	LO2O–	2nd local oscillator output	48	TXENA	Transmit enable

Technical Description

The RF 133 RF/IF transceiver unit is comprised of a receive path, a transmit path, and a synthesizer section as shown in Figure 2. The receive path consists of a selectable gain IF chain, a quadrature demodulator, and baseband amplifier circuitry with I and Q outputs. The transmit path is essentially an I/Q modulator with a translation loop for frequency up-conversion. An on-chip oscillator and frequency dividers make up the synthesizer section. Each section of the RF 133 is separately enabled via the enable signals: TXENA, RXENA, and SXENA.

To control different modes of operation, a serial 21-bit word (bits S1 to S21) is written to the on-chip registers. This 21-bit word is programmed using the three-wire input signals, CLK, DATA, and LE. To ensure that the data remains latched, either one of the signals TXENA, RXENA, or SXENA must stay enabled. The operating mode that draws the least current (12 mA) is the synthesizer mode (i.e., the mode that results when only SXENA is enabled) (refer to Table 5). In the sleep mode, the device typically draws less than 1 μA of current.

The block diagram in Figure 3 shows a complete RF/IF dual-band transceiver chipset using the RF133.

Receive Path

Selectable Gain IF Chain and Quadrature Mixer. The receive path of the RF133 is composed of an IF section and a baseband section. The IF section consists of three programmable gain amplifiers: PGA, PGB, and PGC.

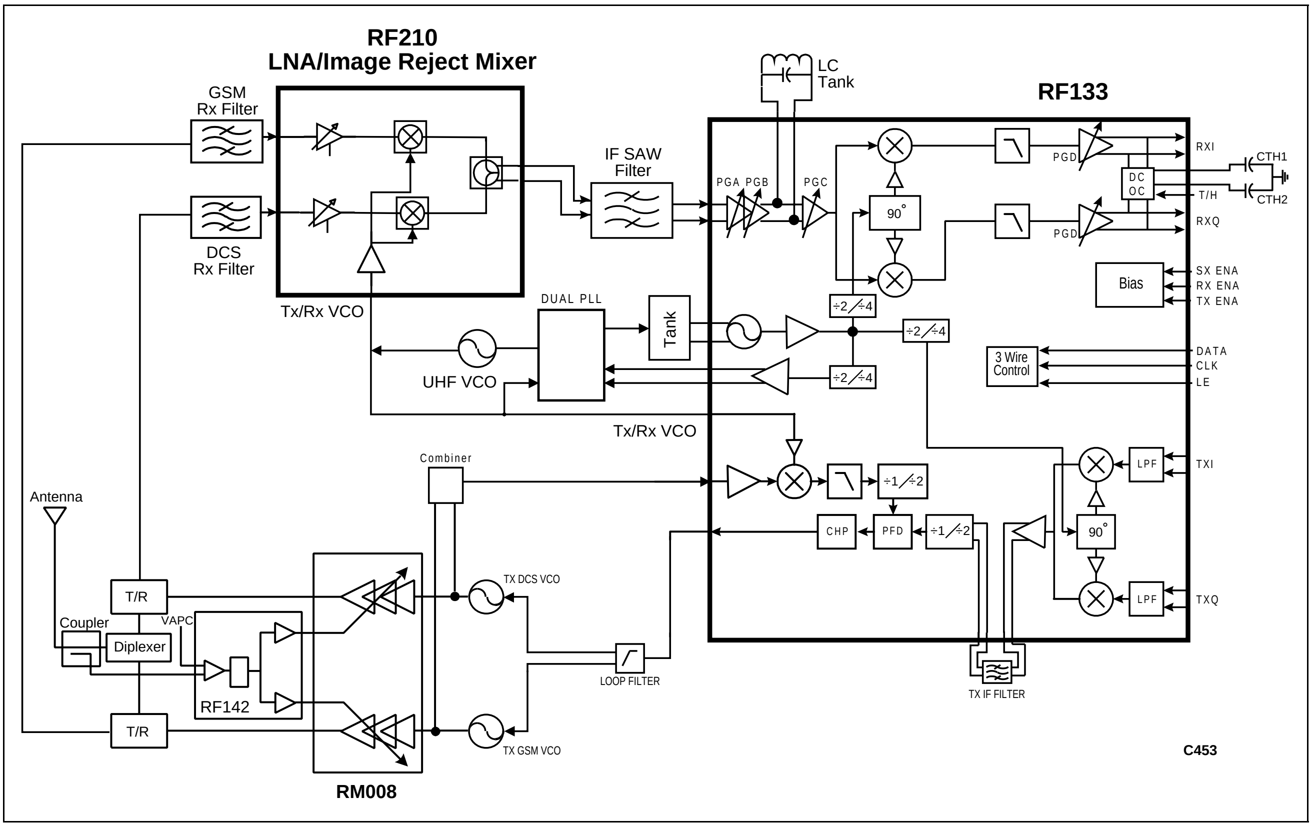


Figure 3. Dual-Band Transceiver Chipset Using The RF133

PGA has two gain settings, either 0 dB or 20 dB, whereas both PGB and PGC have a gain range of -10 dB to 20 dB programmable in 2 dB steps. The output of PGC is fed to a quadrature mixer. The quadrature mixer has a fixed conversion gain of 10 dB and its LO inputs are taken from the outputs of a quadrature divider (divide by 2 or 4).

Baseband Integrated Filters, Baseband Amplifiers, and DC Offset Compensation. Immediately following the quadrature mixer (demodulator) is the baseband section (DC offset compensation circuitry, two integrated baseband filters and two programmable gain amplifiers). Each programmable gain amplifier in the baseband section, both labelled PGD, has four different gain settings: 0 dB, 10 dB, 20 dB, or 30 dB.

The corner frequency of the integrated baseband filters is adjustable by using an appropriate value resistor at pin 26, LPFADJ. At the nominal cutoff frequency of 105 kHz, the resistor value is 75.1 kΩ.

Due to possible high gain of the baseband amplifiers (PGD), any DC offsets at the outputs of the quadrature mixer are amplified and, if uncorrected, the I and Q outputs can suffer from significant unwanted DC offset voltages. To cancel out these effects, the RF133 must be calibrated.

During compensation, the correction voltages are stored in external hold capacitors CTH1 and CTH2, then the loop is opened immediately thereafter. The corrected I and Q outputs are then fed directly to external circuitry for further baseband processing.

The timing diagram for this calibration sequence in reference to the receive slot is shown in Figure 4 (the front-end mixer is assumed to be Rockwell’s RF210 dual-band, image reject downconverter). At first, the RF133 receiver is turned on (RXENA is high). After time T1, the track and hold signal, T/H, places the DC compensation circuitry in the track mode for time T2. Then, there is a settling time, T3, before the external front-end is turned on. Finally, the front-end must be turned on for time T4 before the receive slot.

Time T2 can vary from 10 µsec to 350 µsec. This duration is dependent on 1) the value of the hold capacitors (CTH1 and CTH2), and 2) whether the calibration is done from frame to frame or from a cold start. This is tabulated in Table 2.

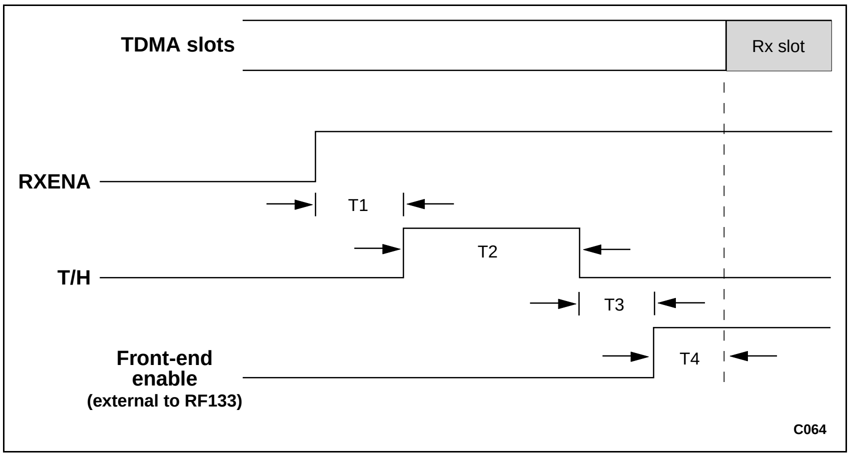


Figure 4. RF133 Sample and Hold Timing Diagram

Table 2. Minimum Required DC Offset Calibration Time T2 and Droop Rate

Hold Capacitor (CTH1, CTH2)	22 nF	120 nF
Cold start	60 µsec	350 µs
Frame-to-frame	10 µsec	60 µs
Typical droop-rate (@ I/Q outputs)	1 mV/msec	0.17 mV/ms

Because of on-chip loading currents, the hold capacitors (CTH1 and CTH2) slowly discharge causing the I and Q DC offset voltages to droop if the RF133 remains uncalibrated for an extended period of time (the droop rate versus the hold capacitor is also shown in Table 2).

To rectify this voltage droop, it is recommended that recalibration occur before every receive slot (i.e., every 4.6 ms for GSM).

Internal Voltage Controlled Oscillator (VCO) and Frequency Dividers. The differential VCO output is buffered and then fed to three frequency dividers (Rx, Tx, PLL) with a selectable divide ratio of either 2 or 4. The Rx and Tx dividers are both quadrature dividers, which generate in-phase and quadrature LOs. The buffered PLL divider output can be used to drive an external PLL IC. The resonant element of the VCO is connected to pins 28 (RES1) and 29 (RES2). Figure 5 shows the VCO configuration.

Transmit Path

The transmit path consists of the following functional blocks:

- An I/Q modulator with IF output amplifier.
- A translation loop circuit consisting of a phase/frequency detector, a charge pump, a Tx RF input buffer, an LO input buffer, a mixer, two dividers, and a low pass filter.

The inputs to the I/Q modulator are differential I and Q baseband signals which are low-pass filtered and then applied to a pair of double balanced mixers (see Figure 2). The outputs of the mixers are combined to produce a modulated signal which is then filtered externally and input through pins 6 and 7 (TXIFIN+ and TXIFIN-) to the reference divider in the translation loop.

The translation loop circuit together with the external transmit VCO, external LO, and loop filter, form a PLL with a mixer in the feedback loop. This PLL upconverts the modulated IF signal to the transmit frequency which then drives the final power amplifier. Since inherent bandpass filtering occurs in the PLL, the need for a post PA duplexer is removed. This is the major advantage a translation loop approach has over the conventional upconversion scheme. The elimination of this duplexer reduces the loss in the transmit path which in turn reduces the output level of the final power amplifier and, therefore, reduces the current consumption. Immediate benefits of this approach are increased handset talk time and standby time, and less component count.

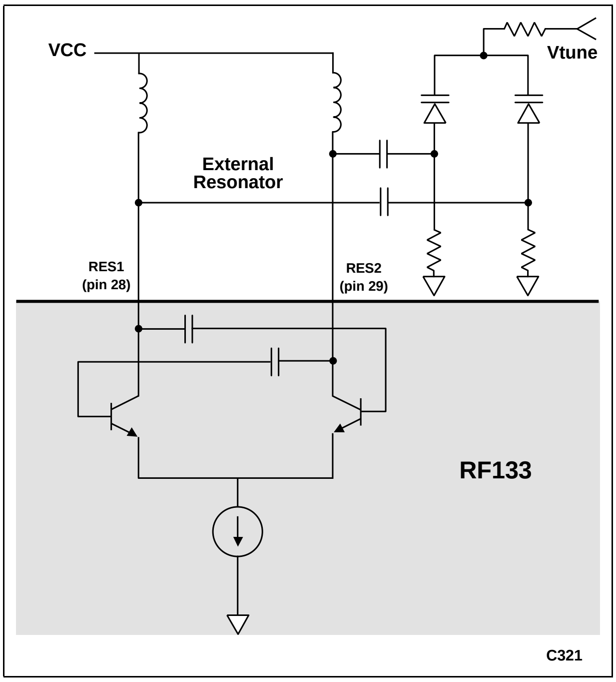


Figure 5. RF133 Internal VCO

Table 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Ambient Operating Temperature	–40	+85	°C
Storage Temperature	–50	+125	°C
Power Dissipation		600	mW
Supply Voltage (VCC)	0	+5	V
Input Voltage Range	GND	VCC	V

The charge pump current can be programmed to be either 1 mA or 0.5 mA and the translation loop can also be programmed to allow for high side or low side injection of the first LO input with respect to the transmit RF.

Even greater flexibility in the transceiver frequency planning is possible because of the programmable dividers in the feedback and the reference paths.

The absolute maximum ratings of the RF133 are provided in Table 3, and the electrical specifications are provided in Table 4. Tables 5, 6, and 7 detail the setting of the programmable operation modes. Figure 6 illustrates the timing of the three-wire bus control signal and Figure 7 provides a graph of the input compression versus the receiver gain.

Figure 8 shows a typical application circuit diagram. Figure 9 provides the package dimensions for the 48-pin device.

Table 4. RF133 Electrical Specifications (1 of 4)
(Ta = 25 °C, VCC = 3.0 V, except where noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Receive IF Path						
Input impedance	Z_{IN}	Differential		1k// 0.15		Ω pF
Input operating frequency	F_{IN}		70		450	MHz
Voltage gain	 A_V A_V	F_{IN} = 400 MHz High gain mode Low gain mode	 57 –23	 60 –20	 63 –17	 dB dB
Gain step (Note 1)	dA_V			2		dB
Gain step accuracy (Note 2)			–0.5		+0.5	dB
Single-sideband noise figure	NF NF	High gain mode Low gain mode		7 23		dB dB
Input 1 dB compression point (Note 3)	P_{1dB} P_{1dB}	High gain mode (60 dB) Low gain mode (–20 dB)		–75 –12		dBV dBV
IF filter pin impedance	Z_{IF}	Differential		600// 1		Ω pF
I/Q Demodulator						
Voltage gain (Quadrature mixer)	A_V			10		dB
I/Q amplitude imbalance					1	dB
I/Q phase imbalance			–3		+3	degrees
Noise Figure	NF			15		dB
Output 1 dB compression point				–2		dBV
Baseband Filter						
Corner frequency (programmable)	F_C		50		150	kHz
Corner frequency variation	dF_C		–15		+15	%
Rejection		F_C = 105 kHz: @200 kHz @400 kHz @600 kHz	 26 	 8 30 40		 dB dB dB
Group delay		F_C = 105 kHz: DC to 100 kHz		 3	 5	 µs
Group delay variation		F_C = 105 kHz: DC to 100 kHz		 300	 500	 ns
Baseband Amplifier						
Voltage gain	A_V			0 10 20 30		dB dB dB dB

Table 4. RF133 Electrical Specifications (2 of 4)

(T_A = 25 °C, VCC = 3.0 V, except where noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Baseband Amplifier (continued)						
Output amplitude		A_V = 30 dB A_V = 20 dB A_V = 10 dB A_V = 0 dB			2.5 1.8 1.0 0.4	Vp-p Vp-p Vp-p Vp-p
Output common mode voltage				1.35		V
Output offset voltage		With DC offset compensation Without DC offset compensation and A_V = 0 dB			±5 ±100	mV mV
Output voltage droop/rise rate		With DC offset compensation, C_{TH} = 22 nF		1		mV/ ms
Output impedance	Z_{OUT}	Differential		200		Ω
I/Q Modulator						
Input impedance	Z_{IN}	Differential		20		kΩ
Input common mode voltage range	V_{CM}		0.85	1.35	VCC – 1.35	V
Input offset voltage	V_{OS}			1	5	mV
Input frequency 3 dB bandwidth				10		MHz
Input common mode rejection ratio		F_{IN} = 100 kHz F_{IN} = 1 MHz		75 55		dB dB
Output operating frequency	F_{OUT}		70		450	MHz
Output impedance	Z_{OUT}	Differential		800		Ω
Output voltage	V_{OUT}		–20	–15		dBV
Output noise power	N_O	10 MHz offset		–130	–126	dBc/Hz
LO feedthrough				–45	–40	dBc
Sideband suppression			40	50		dBc
Spurious (Note 4)		@ 200 kHz offset @ 300 kHz offset		–70 –60	–40 –45	dBc dBc
Translation Loop						
Transmit frequency (input from VCO)	f_{TX}		800		2000	MHz
LO input frequency	f_{LO}		800		2000	MHz
IF frequency	f_{IF} f_{IF}	With divide-by-2 With divide-by-1	70 70		425 300	MHz MHz
Transmit input power	P_{IN}	With external 50 Ω termination	–13	-10	–7	dBm
Transmit input impedance (at pin 47)	Z_{IN}	With pin 46 AC grounded		300// 0.3		Ω pF
LO input power with external 50 Ω termination	P_{IN}		–13	-10	–7	dBm
LO input impedance (at pin 44)	Z_{IN}	With pin 43 AC grounded		300// 0.3		Ω pF

Table 4. RF133 Electrical Specifications (3 of 4)

(T_A = 25 °C, VCC = 3.0 V, except where noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Translation Loop (continued)						
Charge-pump output current	I_{OUT}	Source/sink (CPOI = HIGH) Source/sink (CPOI = LOW) High impedance input		±1.0 ±0.5 0.02		mA mA mA
Transmit output zero crossing spurs: 2X spurs 3X spurs 4X spurs 5X spurs			 –62	 –65 –70 –70 < –70		 dBc dBc dBc dBc
Transmit output noise level (Note 5)		At 20 MHz offset from carrier		–165	–162	dBc/Hz
Device turn-on and lock time (with respect to enable input)				30	100	µs
VCO						
Operating frequency set by resonator	F_{VCO}		300		900	MHz
Tuning voltage range		Varactor ground referenced Varactor supply referenced	0.3 		 VCC–0.3	V V
Resonator pin impedance		Differential		10k//0.4		Ω pF
Tuning sensitivity (Note 6)	K_{VCO}	FVCO = 800 MHz		50		MHz/V
LO phase noise at 10 MHz offset (Note 6)		FVCO = 800 MHz Q = 20		–122		dBc/Hz
Second LO output level		Unloaded, per side		260		mVp
Second LO output impedance		Differential		200		Ω
3-Wire Control						
Data to clock setup time (Note 7)	t_{CS}		50			ns
Data to clock hold time (Note 7)	t_{CH}		10			ns
Clock pulse width high (Note 7)	t_{CWH}		50			ns
Clock pulse width low (Note 7)	t_{CWL}		50			ns
Clock to load enable setup time (Note 7)	t_{ES}		50			ns
Load enable pulse width (Note 7)	t_{EW}		50			ns

Table 4. RF133 Electrical Specifications (4 of 4)

(T_A = 25 °C, VCC = 3.0 V, except where noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Transceiver						
DC offset calibration timing (see Figure 4): T1 T2 (see Table 2) T3 T4 (assuming RF210 front-end mixer)				 40 5 20		 µs µs µs µs
Enable and control VIH	V_{IH}		VCC × 0.8			V
Enable and control VIL	V_{IL}				VCC × 0.2	V
Enable and control IIH	I_{IH}			20	60	µA
Enable and control IIL	I_{IL}		–10	–1	0	µA
Total supply current: Rx mode Tx mode Synthesizer mode Sleep mode (V_{CC} = 5.0 V)	I_{CC}	 (SXENA=RXENA=on) (SXENA=TXENA=on) (SXENA=on)		 52 54 17	 0.1	 mA mA mA mA
Power supply range (transceiver Vcc)	VCC		2.7	3.0	5.0	V
Operating temperature range	T_A		–40	+25	+85	°C

Note 1: Gain steps are such that monotonicity is maintained throughout the entire IF gain range.

Note 2: Specified down to 2.8 V supply voltage. Slight degradation at temperature extremes for 2.7 V supply voltage.

Note 3: Refer to Figure 7 for the 1 dB compression point of the entire receiver chain, including the baseband gain section.

Note 4: For 1 Vp-p 100 kHz differential signals acorss lin and Qin.

Note 5: Using transmit VCO with similar characteristics as Murata MQE 550-902.

Note 6: Using varactors with similar characteristics as Alpha part SMV1234-004.

Note 7: Refer to Figure 6.

Table 5. RF133 Control Bits and Output States

Block	C0	Bit	State	1	0
LO	1	S1	RX LO ÷2/÷4	divide by 4	divide by 2
		S2	2ND LO ÷2/÷4	divide by 4	divide by 2
		S3	TX LO ÷2/÷4	divide by 4	divide by 2
TL	1	S4	TX IF ÷1/÷2	divide by 2	divide by 1
		S5	TX MIX OUT ÷1/÷2	divide by 2	divide by 1
		S6	TX LO INJECTION	High Side	Low Side
		S7	CP OUTPUT CURRENT	1 mA	0.5 mA
Receive	1	S8	RX PGA1	(see Table 6)	
		S9	RX PGB1	(see Table 6)	
		S10	RX PGB2	(see Table 6)	
		S11	RX PGB3	(see Table 6)	
		S12	RX PGB4	(see Table 6)	
		S13	RX PGC1	(see Table 6)	
		S14	RX PGC2	(see Table 6)	
		S15	RX PGC3	(see Table 6)	
		S16	RX PGC4	(see Table 6)	
		S17	RX PGD1	(see Table 7)	
		S18	RX PGD2	(see Table 7)	
TRX	1	S19	TRX BAND	High Band	Low Band
	1	S20	Reserved		
	1	S21	LO BUFFER ON/OFF	ON	OFF

Table 6. Receive IF Gain

Gain (dB)	PGA	PGB				PGC			
	1	1	2	3	4	1	2	3	4
60	1	1	1	1	1	1	1	1	1
58	1	1	1	1	0	1	1	1	1
56	1	1	1	0	1	1	1	1	1
54	1	1	1	0	0	1	1	1	1
52	1	1	0	1	1	1	1	1	1
50	1	1	0	1	0	1	1	1	1
48	1	1	0	0	1	1	1	1	1
46	1	1	0	0	0	1	1	1	1
44	1	0	1	1	1	1	1	1	1
42	1	0	1	1	0	1	1	1	1
40	1	0	1	0	1	1	1	1	1
38	1	0	1	0	0	1	1	1	1
36	1	0	0	1	1	1	1	1	1
34	1	0	0	1	0	1	1	1	1
32	1	0	0	0	1	1	1	1	1
30	1	0	0	0	0	1	1	1	1
28	0	1	0	0	1	1	1	1	1
26	0	1	0	0	0	1	1	1	1
24	0	0	1	1	1	1	1	1	1
22	0	0	1	1	0	1	1	1	1
20	0	0	1	0	1	1	1	1	1
18	0	0	1	0	0	1	1	1	1
16	0	0	0	1	1	1	1	1	1
14	0	0	0	1	0	1	1	1	1
12	0	0	0	0	1	1	1	1	1
10	0	0	0	0	0	1	1	1	1
8	0	0	0	0	0	1	1	1	0
6	0	0	0	0	0	1	1	0	1
4	0	0	0	0	0	1	1	0	0
2	0	0	0	0	0	1	0	1	1
0	0	0	0	0	0	1	0	1	0
–2	0	0	0	0	0	1	0	0	1
–4	0	0	0	0	0	1	0	0	0
–6	0	0	0	0	0	0	1	1	1
–8	0	0	0	0	0	0	1	1	0
–10	0	0	0	0	0	0	1	0	1
–12	0	0	0	0	0	0	1	0	0
–14	0	0	0	0	0	0	0	1	1
–16	0	0	0	0	0	0	0	1	0
–18	0	0	0	0	0	0	0	0	1
–20	0	0	0	0	0	0	0	0	0

Table 7. Receive Baseband Gain

Gain (dB)	PGD	
	1	2
30	1	1
20	1	0
10	0	1
0	0	0

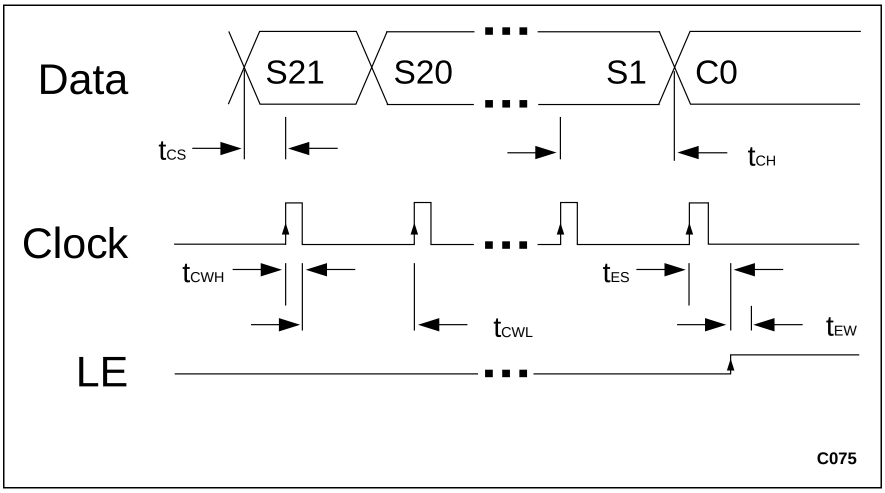


Figure 6. RF133 Timing Diagram

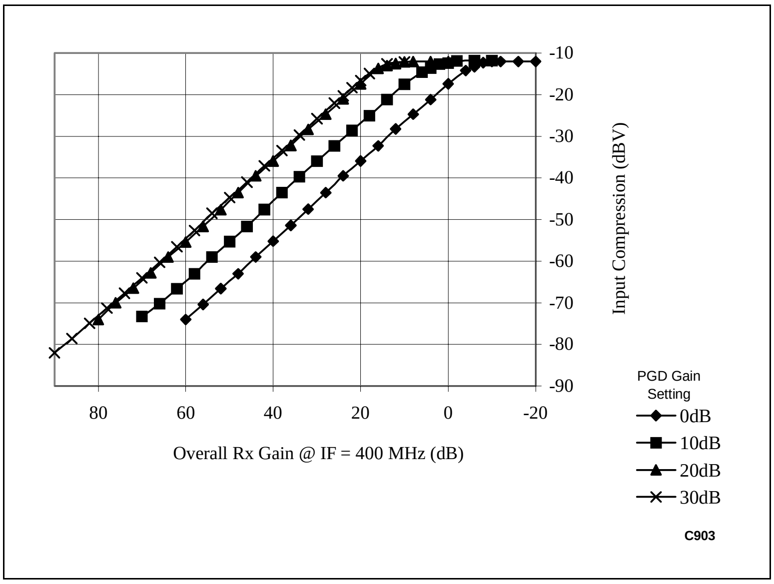


Figure 7. Receiver Input Compression Graph

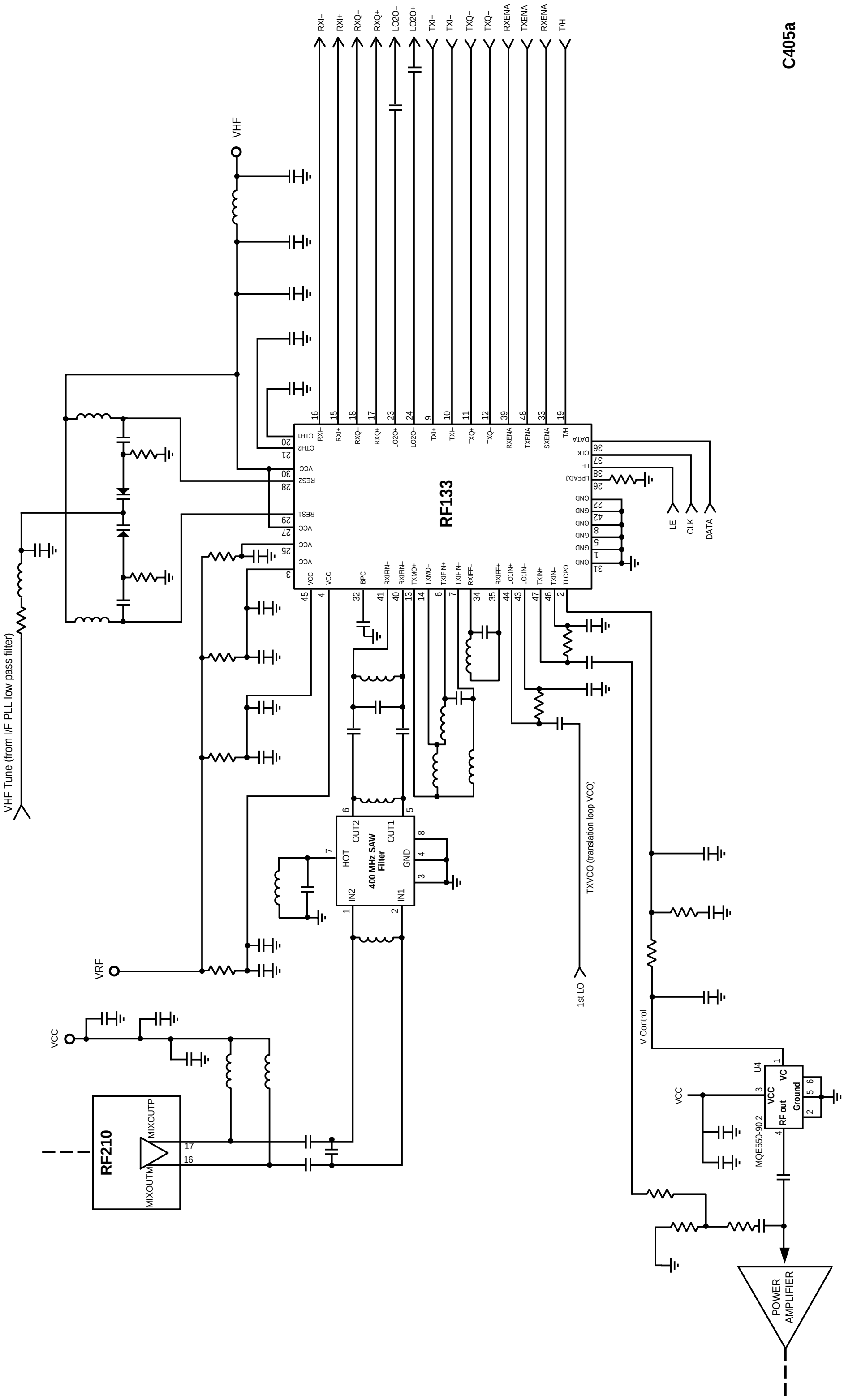
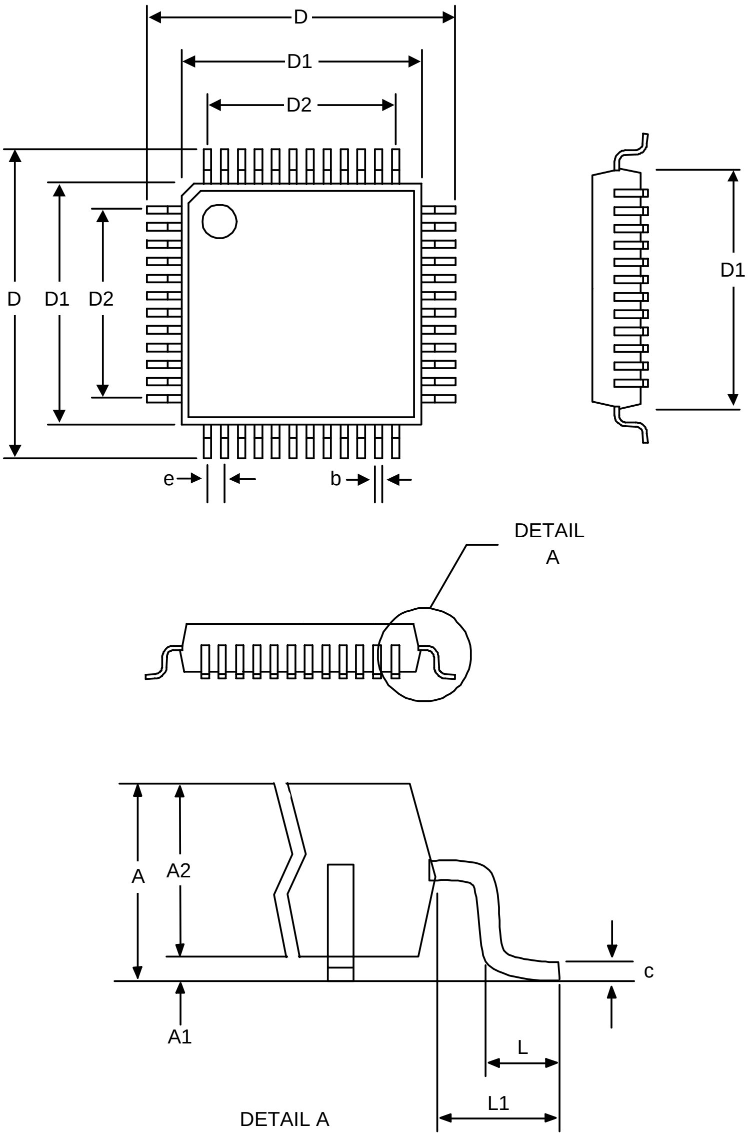


Figure 8. RF133 Typical Application Circuit



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.006
A2	1.35	1.45	0.0528	0.0571
D	8.85	9.15	0.3484	0.3602
D1	6.95	7.05	0.2736	0.2776
D2	5.5 REF		0.2165 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.500 REF		0.0197 REF	
b	0.220 REF		0.0087 REF	
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.10 MAX		0.0039 MAX	

Ref: 48-PIN TQFP (GP00-D283)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 9. RF133 Package Dimensions – 48-Pin TQFP

Ordering Information

Model Name	Manufacturing Part Number	Product Revision
RF/IF Transceiver	RF133	

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