C8051F206

Mixed-Signal 8KB ISP FLASH MCU

PRELIMINARY

ANALOG PERIPHERALS

12-bit, 32-Channel ADC

- 32 External Inputs (Each Port I/O can be configured as an ADC Input on the Fly!)
- Programmable Throughput up to 100ksps
- Programmable Amplifier Gains of 16,8,4,2,1, and 0.5
- No Missing Codes
- VREF from External Pin or VDD

Two Comparators

- Programmable Hysteresis
- Configurable to Generate Interrupts or Reset

VDD Monitor and **Brown-out Detector**

ON-CHIP JTAG DEBUG

- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Watchpoints, Stack Monitor
- Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- Low Cost, **Complete** Development Kit: $99

SUPPLY VOLTAGE ..... 2.7V to 3.6V

- Typical Operating Current: 9mA @ 25MHz
  0.1uA (sleep mode)

8051-COMPATIBLE µC Core

- Pipelined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to **25MIPS** Throughput with 25MHz Clock
- Expanded Interrupt Handler; Up to 21 Interrupt Sources

MEMORY

- 1280 Bytes Data RAM (256 + 1k)
- 8k Bytes FLASH; In-System Programmable in 512 byte Sectors

DIGITAL PERIPHERALS

- 32 Port I/O; All are 5V tolerant
- Hardware SPI™ and UART Serial Ports Available Concurrently
- Three 16-bit Counter/Timers
- Dedicated Watch-Dog Timer
- Bi-directional Reset

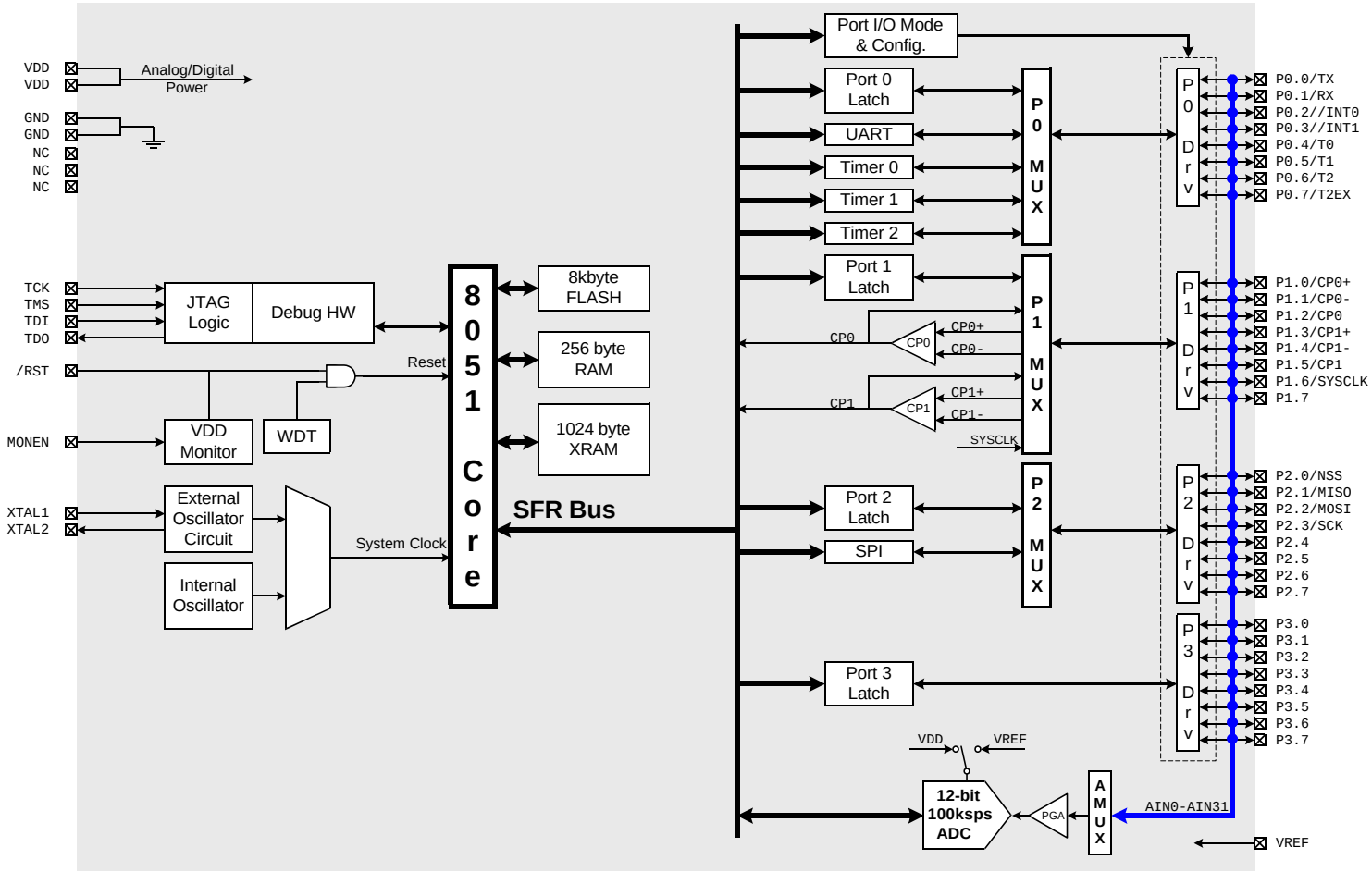
CLOCK SOURCES

- Internal Programmable Oscillator: 2-to-16MHz
- External Oscillator: Crystal, RC, C, or Clock
- Can Switch Between Clock Sources on-the-fly; Useful in Power Saving Modes

Temperature Range: –40°C to +85°C

48-Pin TQFP Package

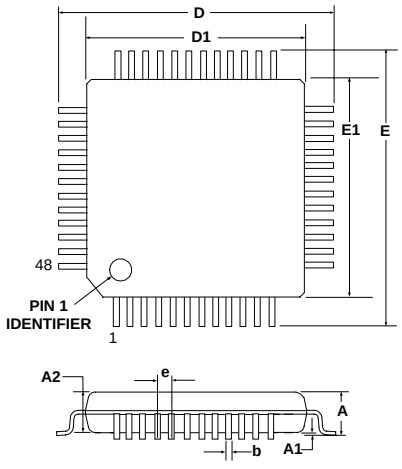
SPI is a trademark of Motorola, Inc.



SELECTED ELECTRICAL SPECIFICATIONS TA = -40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Digital Supply Voltage		2.7		3.6	V
Digital Supply Current with CPU active (VDD=2.7V)	Clock=25MHz Clock=1MHz Clock=32kHz; VDD Monitor Disabled		9 0.7 20		mA mA µA
Digital Supply Current (shutdown)	Oscillator not running; VDD Monitor Enabled Oscillator not running; VDD Monitor Disabled		10 0.1		µA µA
Digital Supply RAM Data Retention Voltage			1.5		V
CPU & DIGITAL I/O PORTS					
Clock Frequency Range		DC		25	MHz
Port Output High Voltage	I_{OH} = -3mA, Port I/O push-pull	VDD – 0.7			V
Port Output Low Voltage	I_{OL} = 8.5mA			0.6	V
Input High Voltage		0.7 x VDD			V
Input Low Voltage				0.3 x VDD	V
SPI Bus Clock Frequency	fCLK=MCU Clock; SPI in Master Mode			fCLK/2	MHz
A/D CONVERTER					
Resolution			12		bits
Integral Nonlinearity			± 1	± 2	LSB
Differential Nonlinearity	Guaranteed Monotonic			± 1	LSB
Signal-to-Noise Plus Distortion		64			dB
Throughput Rate				100	ksps
Input Voltage Range		0		VREF	V
COMPARATORS					
Response Time	| CP+ – CP- | = 100mV		4		µs
Input Voltage Range		-0.25		VDD + 0.25	V
Input Bias Current		-5	0.001	+5	nA
Input Offset Voltage		-10		+10	mV

PACKAGE INFORMATION



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	9.00	-
D1	-	7.00	-
e	-	0.50	-
E	-	9.00	-
E1	-	7.00	-

C8051F206DK DEVELOPMENT KIT ($99)