CY7C4808V25
CY7C4806V25
CY7C4804V25

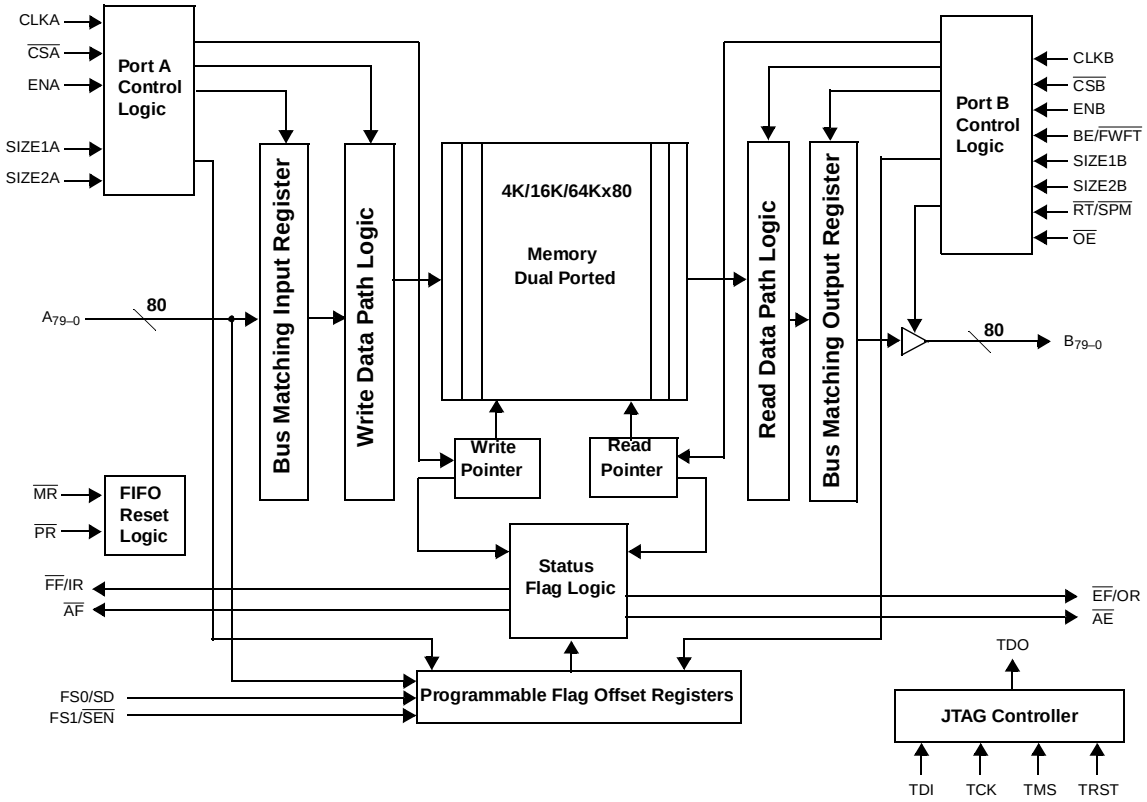
PRELIMINARY

2.5V 4K/16K/64K x 80 Unidirectional Synchronous FIFO w/Bus Matching

Features

- High-speed, low-power, unidirectional, first-in first-out (FIFO) memories w/bus matching capabilities
- 64K x 80 (CY7C4808V25)
- 16K x 80 (CY7C4806V25)
- 4K x 80 (CY7C4804V25)
- 2.5V ± 100 mV power supply
- All I/Os are 1.5V HSTL
- Individual clock frequency up to 200 MHz (5 ns read/write cycle times)
- High-speed access with t_A = 3.3 ns
- Bus matching on both ports: x80, x40, x20, x10
- Free-running CLKA and CLKB. Clocks may be asynchronous or coincident
- CY standard or First-Word Fall-Through modes
- Serial and parallel programming of Almost Empty/Full flags, each with 3 default values (8, 16, 64)
- Master and Partial reset capability
- Retransmit capability
- Big or Little Endian format on Port B
- 288 FBGA 19 mm x 19 mm (1.0-mm ball pitch) packaging
- Width and depth expansion capability
- Fabricated using Cypress 0.21-micron CMOS Technology for optimum speed/power

Preliminary Top Level Block Diagram



For the most recent information, visit the Cypress web site at www.cypress.com

Pin Configuration for CY7C4804V25 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	V_{DDQ}	V_{DDQ}	A16	A19	V_{DDQ}	A30	A34	GND	CLKA	A42	GND	A48	A51	V_{DDQ}	A55	A57	V_{DDQ}	V_{DDQ}	A
B	V_{DDQ}	A10	A14	A17	V_{DDQ}	A29	A33	GND	A39	A41	GND	A45	A50	V_{DDQ}	A54	A56	A58	V_{DDQ}	B
C	A9	A8	V_{DDQ}	A13	A18	A28	A32	A36	A38	V_{DDQ}	A44	A46	A49	A52	A53	V_{DDQ}	A59	A60	C
D	A7	A6	A11	V_{DDQ}	A20	GND	A27	SH	GND	$\overline{FF}$/IR	V_{DD}	A43	GND	A47	V_{DDQ}	A63	A67	A69	D
E	V_{DDQ}	V_{DDQ}	$\overline{MR}$	$\overline{PR}$	V_{DD}	A25	GND	$\overline{FS1}$/$\overline{SEN}$	GND	GND	$\overline{AF}$	GND	GND	V_{DD}	TDI	A66	V_{DDQ}	V_{DDQ}	E
F	A12	A15	SIZE 1A	GND	$\overline{A21}$	A24	A31	A35	A37	ENA	$\overline{CSA}$	A40	A61	V_{DD}	GND	A64	A65	A68	F
G	A5	A2	SIZE 2B	FS0/ SD	GND	A23							A62	GND	TDO	A70	A71	A72	G
H	GND	GND	$\overline{RT}$/ SPM	V_{DD}	SIZE 1B	A4							A73	A74	TCK	A75	GND	GND	H
J	B2	B3	V_{DDQ}	A1	GND	A0							A76	GND	GND	A77	A78	A79	J
K	B6	B7	B4	GND	GND	A3							B76	GND	B77	V_{DDQ}	B78	B79	K
L	GND	GND	B5	$\overline{BE}$/ $\overline{FWFT}$	A22	A26							B73	B74	TMS	B75	GND	GND	L
M	B10	B9	VREF	B8	GND	SIZE 2A							B69	GND	TRST	B70	B71	B72	M
N	B14	B13	B12	GND	B1	B11	B31	B35	B37	B40	B43	B45	B65	NC	GND	B66	B67	B68	N
P	V_{DDQ}	V_{DDQ}	B15	NC	NC	B0	GND	$\overline{EF}$/ OR	GND	GND	$\overline{CSB}$	GND	NC	V_{DD}	$\overline{OE}$	B64	V_{DDQ}	V_{DDQ}	P
R	B18	B17	B16	V_{DDQ}	NC	GND	NC	V_{DD}	$\overline{AE}$	GND	ZQ	ENB	GND	NC	V_{DDQ}	B61	B62	B63	R
T	B20	B19	V_{DDQ}	B24	B27	B28	B32	B36	V_{DDQ}	B41	B44	B46	B49	B52	B53	V_{DDQ}	B59	B60	T
U	V_{DDQ}	B21	B22	B25	V_{DDQ}	B29	B33	GND	B38	B42	GND	B47	B50	V_{DDQ}	B54	B56	B58	V_{DDQ}	U
V	V_{DDQ}	V_{DDQ}	B23	B26	V_{DDQ}	B30	B34	GND	B39	CLKB	GND	B48	B51	V_{DDQ}	B55	B57	V_{DDQ}	V_{DDQ}	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Pin Configuration for CY7C4806V25 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	V_{DDQ}	V_{DDQ}	A16	A19	V_{DDQ}	A30	A34	GND	CLKA	A42	GND	A48	A51	V_{DDQ}	A55	A57	V_{DDQ}	V_{DDQ}	A
B	V_{DDQ}	A10	A14	A17	V_{DDQ}	A29	A33	GND	A39	A41	GND	A45	A50	V_{DDQ}	A54	A56	A58	V_{DDQ}	B
C	A9	A8	V_{DDQ}	A13	A18	A28	A32	A36	A38	V_{DDQ}	A44	A46	A49	A52	A53	V_{DDQ}	A59	A60	C
D	A7	A6	A11	V_{DDQ}	A20	GND	A27	SH	GND	$\overline{FF}$/IR	V_{DD}	A43	GND	A47	V_{DDQ}	A63	A67	A69	D
E	V_{DDQ}	V_{DDQ}	$\overline{MR}$	$\overline{PR}$	V_{DD}	A25	GND	$\overline{FS1}$/ $\overline{SEN}$	GND	GND	$\overline{AF}$	GND	V_{DD}	V_{DD}	TDI	A66	V_{DDQ}	V_{DDQ}	E
F	A12	A15	SIZE 1A	GND	$\overline{A21}$	A24	A31	A35	A37	ENA	$\overline{CSA}$	A40	A61	V_{DD}	GND	A64	A65	A68	F
G	A5	A2	SIZE 2B	FS0/ SD	GND	A23							A62	GND	TDO	A70	A71	A72	G
H	GND	GND	$\overline{RT}$/ SPM	V_{DD}	SIZE 1B	A4							A73	A74	TCK	A75	GND	GND	H
J	B2	B3	V_{DDQ}	A1	GND	A0							A76	GND	GND	A77	A78	A79	J
K	B6	B7	B4	GND	GND	A3							B76	GND	B77	V_{DDQ}	B78	B79	K
L	GND	GND	B5	BE/ $\overline{FWFT}$	A22	A26							B73	B74	TMS	B75	GND	GND	L
M	B10	B9	VREF	B8	GND	SIZE 2A							B69	GND	TRST	B70	B71	B72	M
N	B14	B13	B12	GND	B1	B11	B31	B35	B37	B40	B43	B45	B65	NC	GND	B66	B67	B68	N
P	V_{DDQ}	V_{DDQ}	B15	NC	NC	B0	GND	$\overline{EF}$/ OR	GND	GND	$\overline{CSB}$	GND	NC	V_{DD}	$\overline{OE}$	B64	V_{DDQ}	V_{DDQ}	P
R	B18	B17	B16	V_{DDQ}	NC	GND	NC	V_{DD}	$\overline{AE}$	GND	ZQ	ENB	GND	NC	V_{DDQ}	B61	B62	B63	R
T	B20	B19	V_{DDQ}	B24	B27	B28	B32	B36	V_{DDQ}	B41	B44	B46	B49	B52	B53	V_{DDQ}	B59	B60	T
U	V_{DDQ}	B21	B22	B25	V_{DDQ}	B29	B33	GND	B38	B42	GND	B47	B50	V_{DDQ}	B54	B56	B58	V_{DDQ}	U
V	V_{DDQ}	V_{DDQ}	B23	B26	V_{DDQ}	B30	B34	GND	B39	CLKB	GND	B48	B51	V_{DDQ}	B55	B57	V_{DDQ}	V_{DDQ}	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Pin Configuration for CY7C4808V25 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	V_{DDQ}	V_{DDQ}	A16	A19	V_{DDQ}	A30	A34	GND	CLKA	A42	GND	A48	A51	V_{DDQ}	A55	A57	V_{DDQ}	V_{DDQ}	A
B	V_{DDQ}	A10	A14	A17	V_{DDQ}	A29	A33	GND	A39	A41	GND	A45	A50	V_{DDQ}	A54	A56	A58	V_{DDQ}	B
C	A9	A8	V_{DDQ}	A13	A18	A28	A32	A36	A38	V_{DDQ}	A44	A46	A49	A52	A53	V_{DDQ}	A59	A60	C
D	A7	A6	A11	V_{DDQ}	A20	GND	A27	SH	GND	$\overline{FF}$/IR	V_{DD}	A43	GND	A47	V_{DDQ}	A63	A67	A69	D
E	V_{DDQ}	V_{DDQ}	$\overline{MR}$	$\overline{PR}$	V_{DD}	A25	GND	$\overline{FS1}$/$\overline{SEN}$	GND	GND	$\overline{AF}$	GND	GND	V_{DD}	TDI	A66	V_{DDQ}	V_{DDQ}	E
F	A12	A15	SIZE 1A	GND	$\overline{A21}$	A24	A31	A35	A37	ENA	$\overline{CSA}$	A40	A61	GND	GND	A64	A65	A68	F
G	A5	A2	SIZE 2B	FS0/ SD	GND	A23							A62	GND	TDO	A70	A71	A72	G
H	GND	GND	$\overline{RT}$/ SPM	V_{DD}	SIZE 1B	A4							A73	A74	TCK	A75	GND	GND	H
J	B2	B3	V_{DDQ}	A1	GND	A0							A76	GND	GND	A77	A78	A79	J
K	B6	B7	B4	GND	GND	A3							B76	GND	B77	V_{DDQ}	B78	B79	K
L	GND	GND	B5	$\overline{BE}$/ $\overline{FWFT}$	A22	A26							B73	B74	TMS	B75	GND	GND	L
M	B10	B9	VREF	B8	GND	SIZE 2A							B69	GND	TRST	B70	B71	B72	M
N	B14	B13	B12	GND	B1	B11	B31	B35	B37	B40	B43	B45	B65	NC	GND	B66	B67	B68	N
P	V_{DDQ}	V_{DDQ}	B15	NC	NC	B0	GND	$\overline{EF}$/ OR	GND	GND	$\overline{CSB}$	GND	NC	V_{DD}	$\overline{OE}$	B64	V_{DDQ}	V_{DDQ}	P
R	B18	B17	B16	V_{DDQ}	NC	GND	NC	V_{DD}	$\overline{AE}$	GND	ZQ	ENB	GND	NC	V_{DDQ}	B61	B62	B63	R
T	B20	B19	V_{DDQ}	B24	B27	B28	B32	B36	V_{DDQ}	B41	B44	B46	B49	B52	B53	V_{DDQ}	B59	B60	T
U	V_{DDQ}	B21	B22	B25	V_{DDQ}	B29	B33	GND	B38	B42	GND	B47	B50	V_{DDQ}	B54	B56	B58	V_{DDQ}	U
V	V_{DDQ}	V_{DDQ}	B23	B26	V_{DDQ}	B30	B34	GND	B39	CLKB	GND	B48	B51	V_{DDQ}	B55	B57	V_{DDQ}	V_{DDQ}	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Functional Description

The CY7C480XV25 family of FIFOs is comprised of high-speed, low-power, CMOS Synchronous (clocked) FIFO memories, meaning both independent ports employ a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of the clock on either port by the enable signal. The clocks for each port are independent of one another and can be asynchronous or coincident. The enable for each port is arranged to provide a simple unidirectional interface between microprocessors and/or buses with synchronous control.

Two kinds of reset are available on the CY7C480XV25: Master Reset and Partial Reset. Master Reset initializes the read and write pointers to the first location of the memory array, configures the FIFO for Big Endian or Little Endian byte arrangement, selects the CY standard or First-Word Fall-Through (FWFT) mode, and determines the configuration of the programmable flags. The flags can be programmed either in serial mode or in parallel mode. The FIFO also comes with three possible default flag offset settings: 8, 16, or 64.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings.

The CY7C480XV25 have two modes of operation: CY Standard Mode or First-Word Fall-Through Mode (FWFT). In the CY Standard Mode, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other subsequent words residing in memory). In the FWFT Mode, the first word written to an empty FIFO appears automatically on the outputs, and no read operation is required. Nevertheless, accessing subsequent words does necessitate formal read request. FWFT mode is primarily used for cascading multiple FIFOs.

The FIFO has an $\overline{EF}$/OR flag on port B and $\overline{FF}$/IR flag on Port A. The $\overline{EF}$ and $\overline{FF}$ functions are selected in the CY Standard Mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether or not the memory is full. The IR and OR functions are selected in the First-Word Fall-Through mode. IR indicates whether or not the FIFO has memory locations available. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

The FIFO has a programmable Almost Empty flag ($\overline{AE}$) and a programmable Almost Full flag ($\overline{AF}$). $\overline{AE}$ indicates the number of words left in the FIFO memory is at the user-defined amount. $\overline{AF}$ indicates the number of words written into the FIFO memory has achieved a predetermined amount.

$\overline{FF}$/IR and $\overline{AF}$ flags are synchronized to port A clock that writes data into its array. $\overline{EF}$/OR and $\overline{AE}$ flags are synchronized to Port B clock that reads data from its array. Programmable offsets for $\overline{AE}$ and $\overline{AF}$ are loaded in parallel via Port A or in serial via the SD input. The Serial Programming Mode pin ($\overline{SPM}$) makes this selection. Three default offsets setting are also provided. The $\overline{AE}$ threshold can be set at 8, 16, or 64 locations from the empty boundary and $\overline{AF}$ threshold can be set at 8, 16, or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

The CY7C480XV25 FIFOs are characterized for operation from 0°C to 70°C commercial, and from –40°C to 85°C industrial.

Selection Guide

	CY7C480XV25-200	CY7C480XV25-166
Maximum Frequency (MHz)	200	166
Maximum Access Time (ns)	3.3	3.7
Minimum Cycle Time (ns)	5	6
Minimum Data or Enable Set-Up (ns)	0.9	0.9
Minimum Data or Enable Hold (ns)	0.6	0.6
Maximum Flag Delay (ns)	3.3	3.7

	CY7C4808V25	CY7C4806V25	CY7C4804V25
Density	64K x 80	16K x 80	4K x 80
Package	288 FBGA	288 FBGA	288 FBGA

Pin Description

Pin	Description
V_{DDQ}	Power supply for I/Os
V_{DD}	Power supply for internal logic
GND	Ground
V_{REF}	Reference voltage
$\overline{MR}$	Master reset
$\overline{PR}$	Partial reset
A_0–A_{79}	Input data bus
B_0–B_{79}	Output data bus
ENA	Port A enable pin
ENB	Port B enable pin
$\overline{CSA}$	Port A chip select
$\overline{CSB}$	Port B chip select
$\overline{OE}$	Output enable
CLKA	Port A clock
CLKB	Port B clock
BE/$\overline{FWFT}$	Big/Little Endian and CY Standard/First-Word Fall-Through mode select pin
SIZE1A, SIZE2A	Port A bus size configuration pins
SIZE1B, SIZE2B	Port B bus size configuration pins
$\overline{RT}$/$\overline{SPM}$	Retransmit pin/serial programming select
TDI, TDO, TCK, TMS, TRST	JTAG pins
FS1/$\overline{SEN}$, FS0/SD	Programmable flags configuration pins
$\overline{EF}$/OR	Empty/Output Ready flag (Port B)
$\overline{FF}$/IR	Full/Input Ready flag (Port A)
$\overline{AE}$	Programmable Almost Empty flag (Port B)
$\overline{AF}$	Programmable Almost Full flag (Port A)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied .....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[1] ..... –0.5V to V_{DDQ}+0.5V

DC Input Voltage[1] ..... –0.5V to V_{DDQ}+0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage .....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V ± 100 mV	1.4V to 1.9V
Industrial	–40°C to +85°C		

DC Specifications (All I/Os except JTAG ports will be at HSTL level)[2, 3]

Parameter	Description	Test Conditions	CY7C480XV25		Unit
			Min.	Max.	
V_{DD}	Power Supply Voltage		2.4	2.6	V
V_{DDQ}	I/O Supply Voltage		1.4	1.9	V
V_{REF}	Input Reference Voltage	Typical value = 0.75V	0.68	1.0	V
V_{OH}	Output HIGH Voltage		(V_{DDQ}/2) + 0.3	V_{DDQ}	V
V_{OL}	Output LOW Voltage		V_{SS}	(V_{DDQ}/2) – 0.3	V
V_{IH}	Input HIGH Voltage		V_{REF} + 0.1	(V_{DDQ}/2) + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	V_{REF} – 0.1	V
V_{OH_JTAG}	JTAG Port Output High Voltage	I_{OH} = –100 µA	2.1		V
		I_{OH} = –2 mA	1.7		V
V_{OL_JTAG}	JTAG Port Output Low Voltage	I_{OL}= 100 µA		0.2	V
		I_{OL}= 2 mA		0.7	V
V_{IH_JTAG}	JTAG Port Input High Voltage	$V_{OUT} \geq V_{VOH}$(min.)	1.7	V_{DD}+0.3	V
V_{IL_JTAG}	JTAG Port Input Low Voltage	$V_{OUT} \leq V_{VOL}$(max.)	–0.3	0.7	V
I_{IX}	Input Leakage Current		–10	+10	µA
I_{OZL},I_{OZH}	Output OFF, High Z Current		–10	+10	µA
I_{SB}	Average Standby Current			10	mA

Notes:
1. Minimum voltage equal –2.0V for pulse duration less than 20ns.
2. All voltage referenced to ground.
3. Overshoot: V_{IH} (AC) ≤ V_{DD}+1.5V for t ≤ t_{clk}/2, Power-Up: V_{IH}<2.6V and V_{DD}<2.4V and V_{DDQ}<1.4V for t<200 ns.

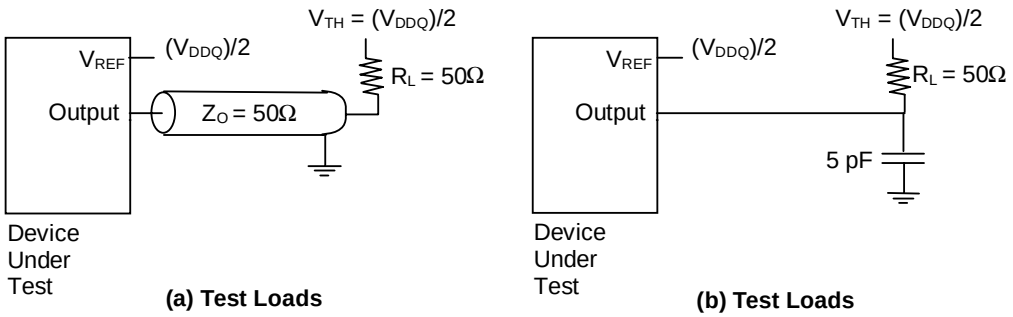
DC Specifications (continued)[4]

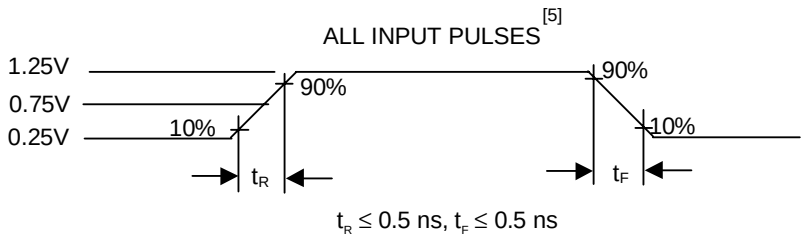
Parameter	Description	Conditions	200 MHz	166 MHz	Unit
I_{CC}	Operating current (Typical)	V_{DD} = max., I_{OUT} = 0 mA	225	185	mA
	Operating current (Max.)		300	250	mA

AC Specifications (A 50Ω load terminated into 0.75V is used with V_{DDQ})

Parameter	Description	CY7C480XV25		Unit
		Min.	Max.	
F_{MAX}	Max. Frequency		200	MHz
t_{CYC}	Clock Cycle Time	5		ns
t_{SD}	Input Data Set-Up Time	0.9		ns
t_{HD}	Input Data Hold Time	0.6		ns
t_A	Access Time	3.3		ns

AC Test Loads and Waveforms





Notes:

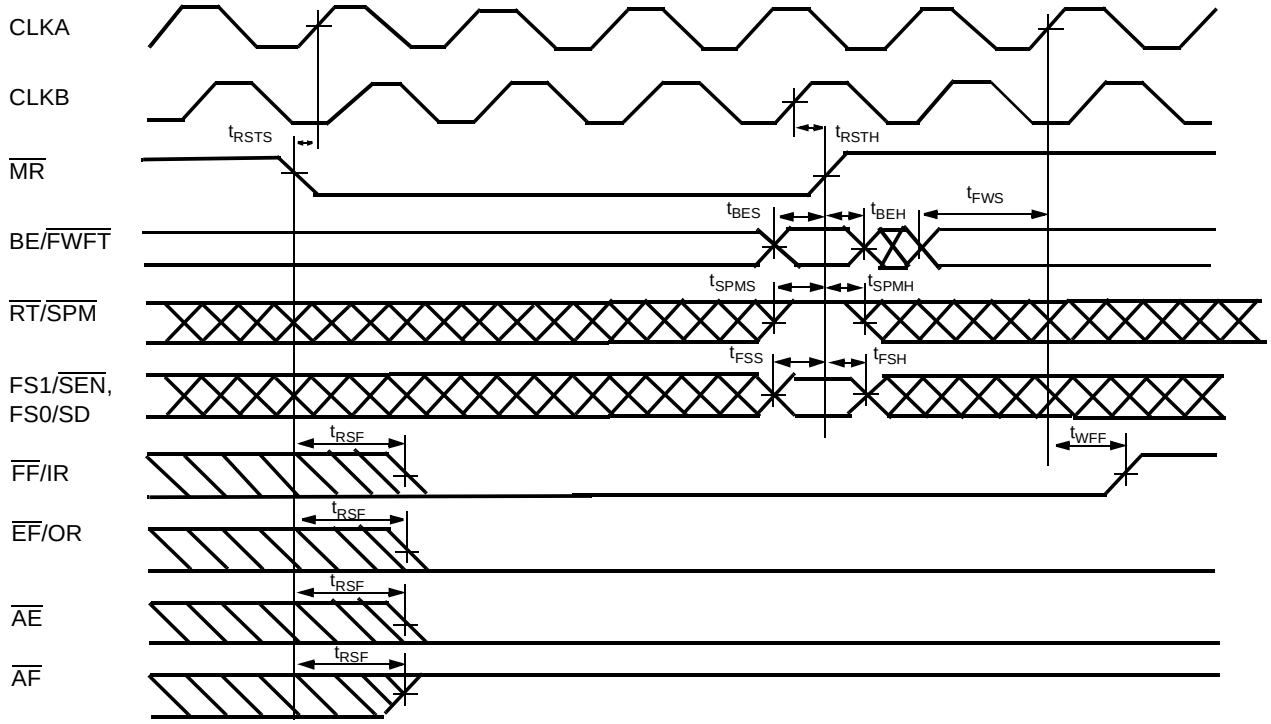
4. Both clocks switching at maximum speeds, data switching at half the clock frequency.
5. Unless otherwise noted, test conditions assume signal transition time of 2 V/ns, timing reference levels of 0.75V, V_{ref} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (b) of AC test loads.

Timing Parameters

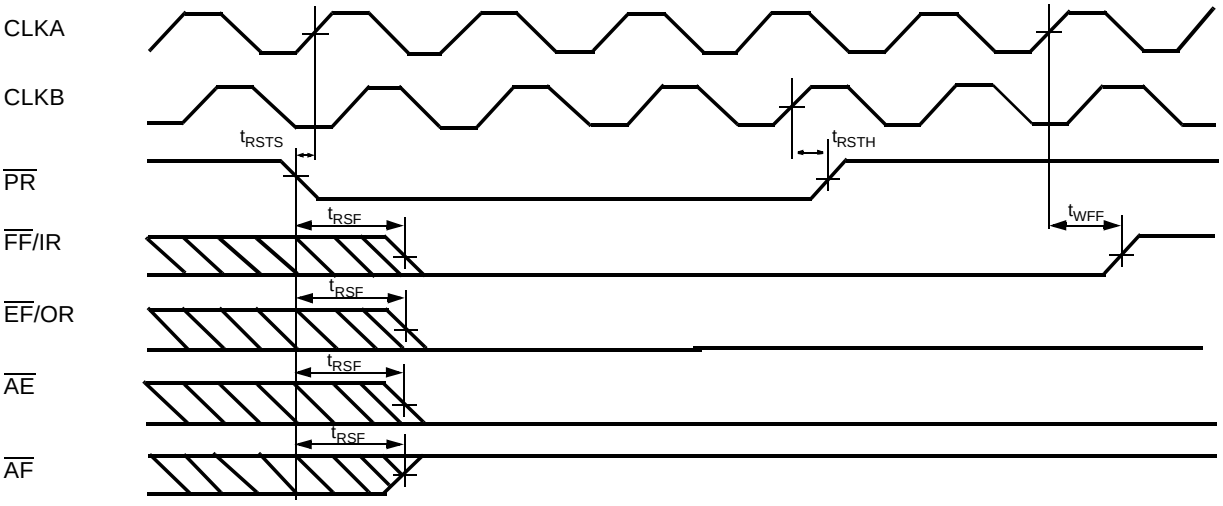
Parameter	7C480XV25-200		7C480XV25-166		Unit
	Min.	Max.	Min.	Max.	
f_S		200		166	MHz
t_{CLK}	5		6		ns
t_{CLKH}	2.5		3		ns
t_{CLKL}	2.5		3		ns
t_{DS}	0.9		0.9		ns
t_{ENS}	0.9		0.9		ns
t_{RSTS}	2		2		ns
t_{FSS}	2		2		ns
t_{BES}	2		2		ns
t_{SMPS}	2		2		ns
t_{SDS}	0.9		0.9		ns
t_{SENS}	0.9		0.9		ns
t_{FWS}	0.9		0.9		ns
t_{DH}	0.6		0.6		ns
t_{ENH}	0.6		0.6		ns
t_{RSTH}	2		2		ns
t_{FSH}	2		2		ns
t_{BEH}	2		2		ns
t_{SPMH}	2		2		ns
t_{SDH}	0.6		0.6		ns
t_{SENH}	0.6		0.6		ns
t_{SPH}	0.6		0.6		ns
t_{SKEW1}	8		10		ns
t_{SKEW2}	8		10		ns
t_A		3.3		3.7	ns
t_{WFF}		3.3		3.7	ns
t_{REF}		3.3		3.7	ns
t_{PAE}		3.3		3.7	ns
t_{PAF}		3.3		3.7	ns
t_{RSF}		4		4	ns
t_{EN}		3.5		3.5	ns
t_{DIS}		3.5		3.5	ns
t_{PRT}	25		25		ns
t_{RTR}	45		45		ns

Switching Waveforms

Master Reset Loading X and Y with a Preset Value of Eight [6]



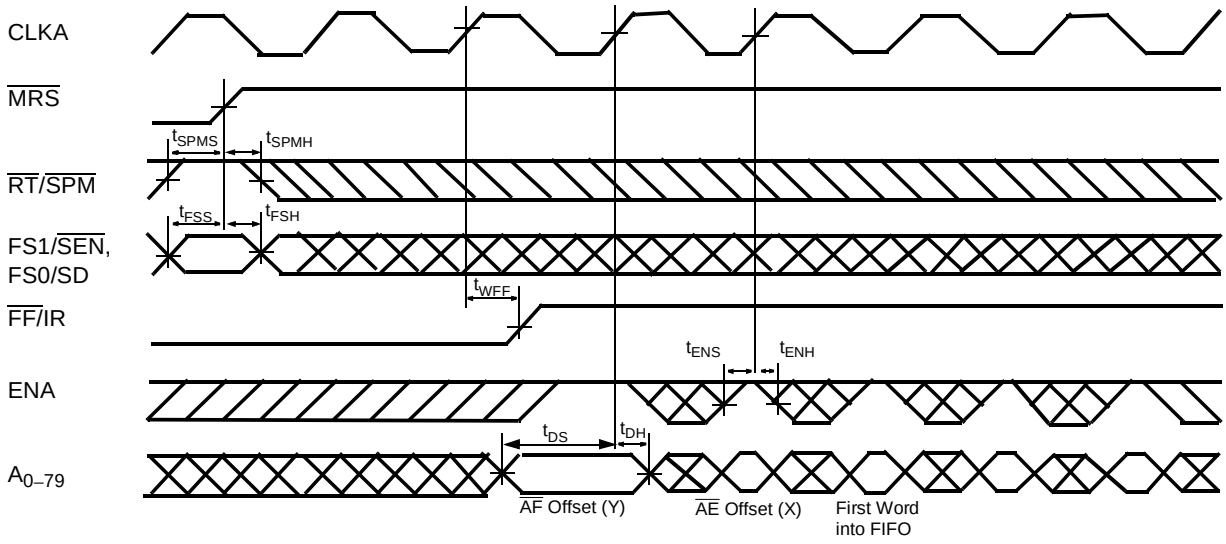
Partial Reset (CY Standard and FWFT Modes) [7]



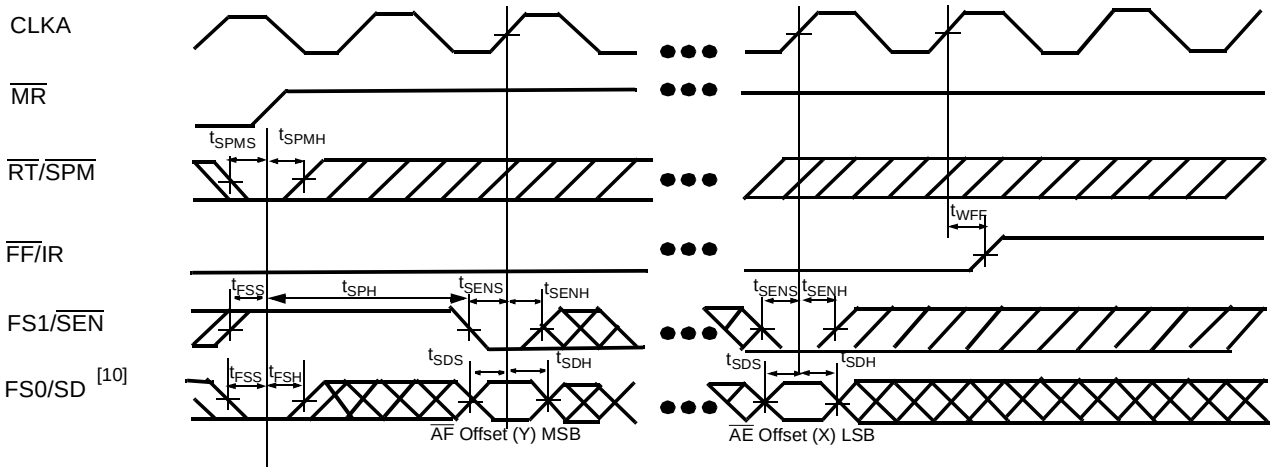
Notes:
6. $\overline{PR}$ must be HIGH during Master Reset.
7. $\overline{MR}$ must be HIGH during Partial Reset.

Switching Waveforms (continued)

Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (CY Standard and FWFT Modes) [8]



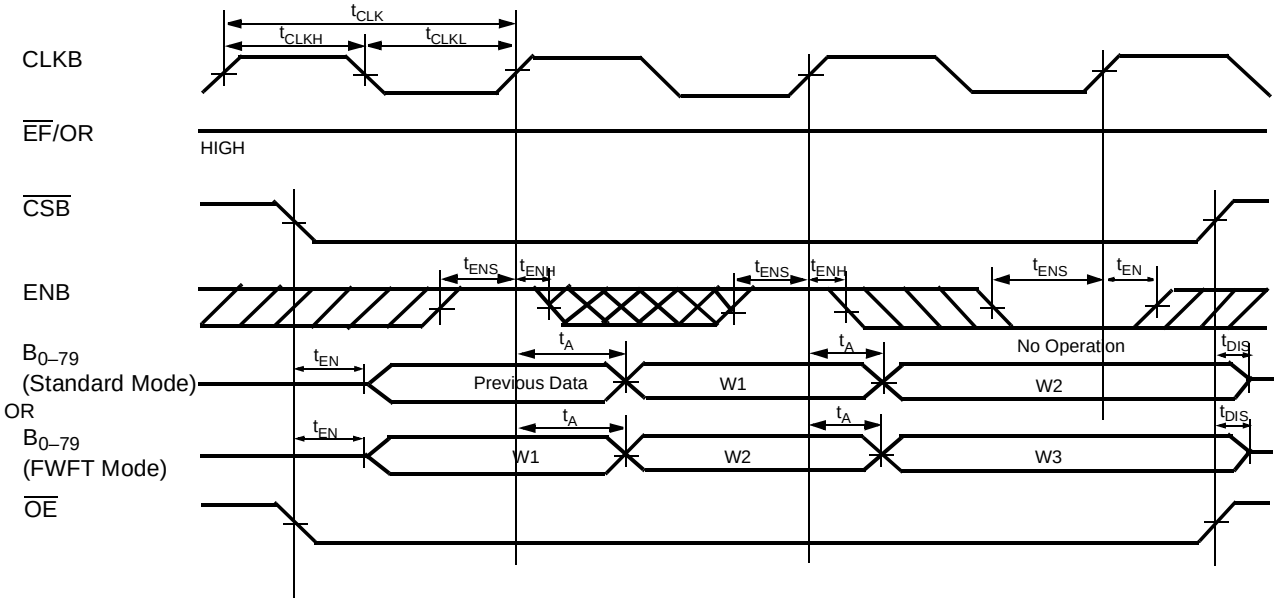
Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values (CY Standard and FWFT Modes) [9]



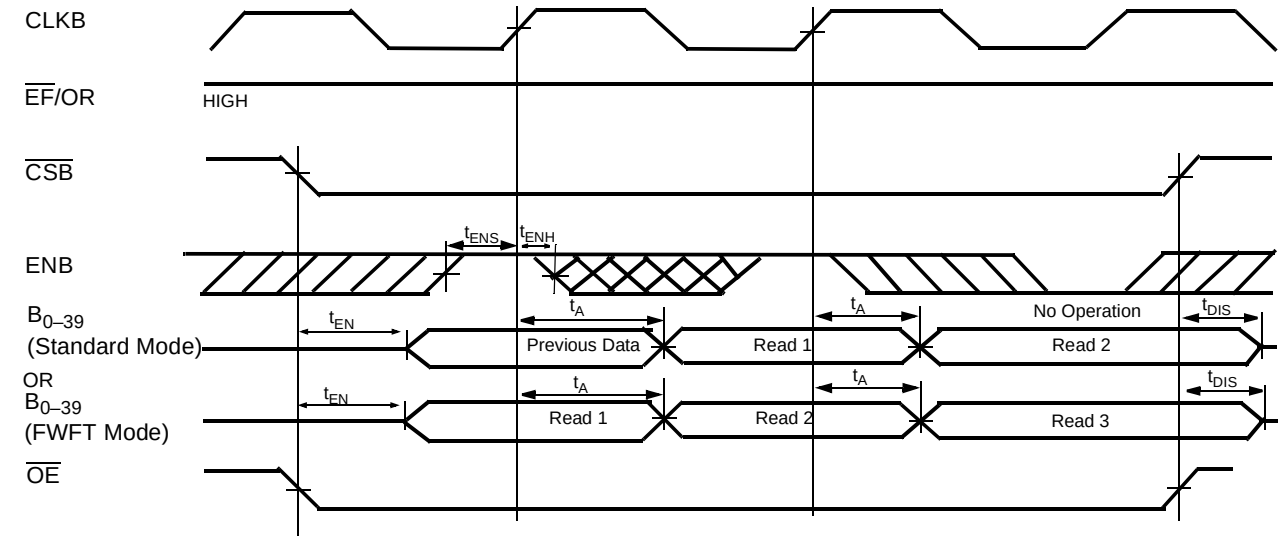
Notes:
8. $\overline{CSA}$ = LOW. It is not necessary to program offset register on consecutive clock cycles.
9. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set HIGH.
10. Programmable offsets are written serially to the SD input in the order $\overline{AF}$ offset (Y) then $\overline{AE}$ offset (X).

Switching Waveforms (continued)

Port B Long-Word Read Cycle Timing for FIFO (CY Standard and FWFT Modes)



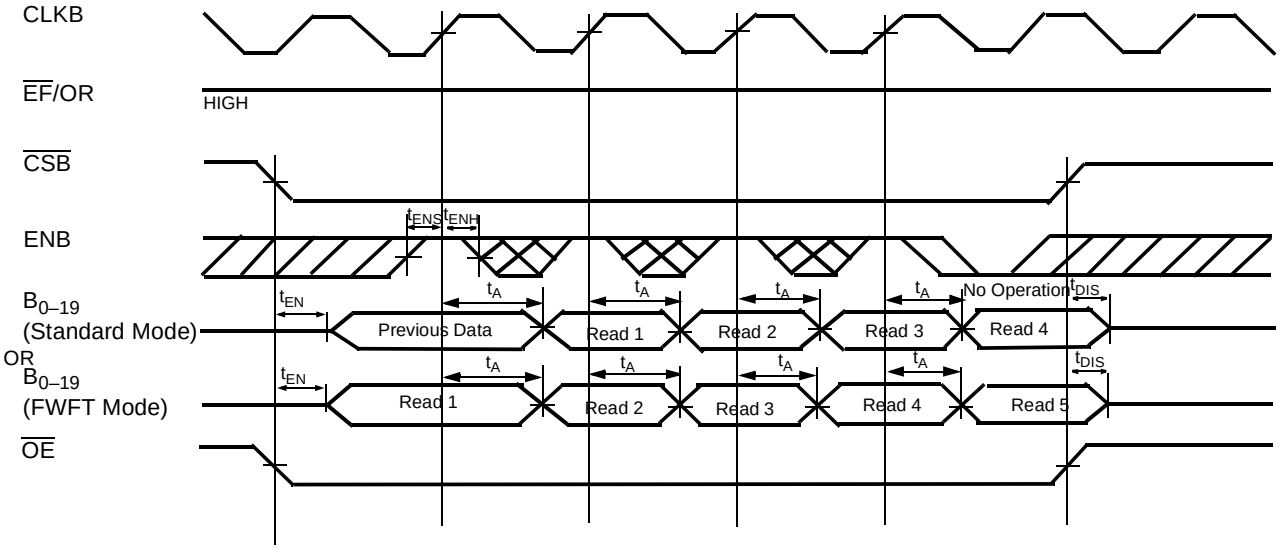
Port B Word Read Cycle Timing for FIFO (CY Standard and FWFT Modes) [11]



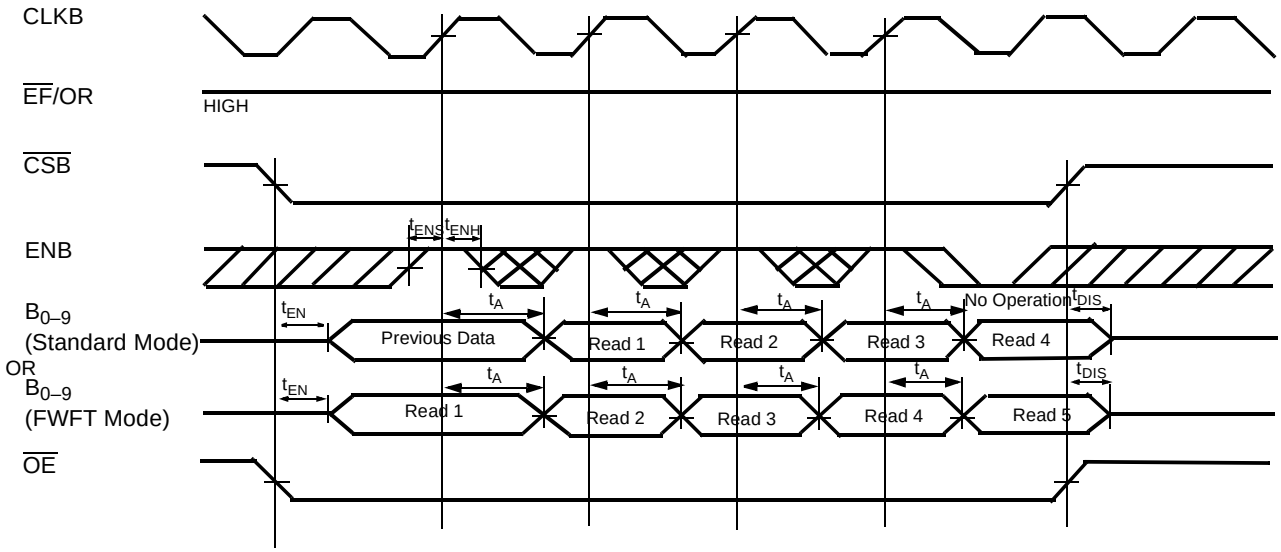
Note:
11. Unused bits $B_{40–79}$ are zeroes for word-size reads.

Switching Waveforms (continued)

Port B Short Word Read Cycle Timing for FIFO (CY Standard and FWFT Modes) [12]



Port B Byte Read Cycle Timing for FIFO (CY Standard and FWFT Modes) [13]

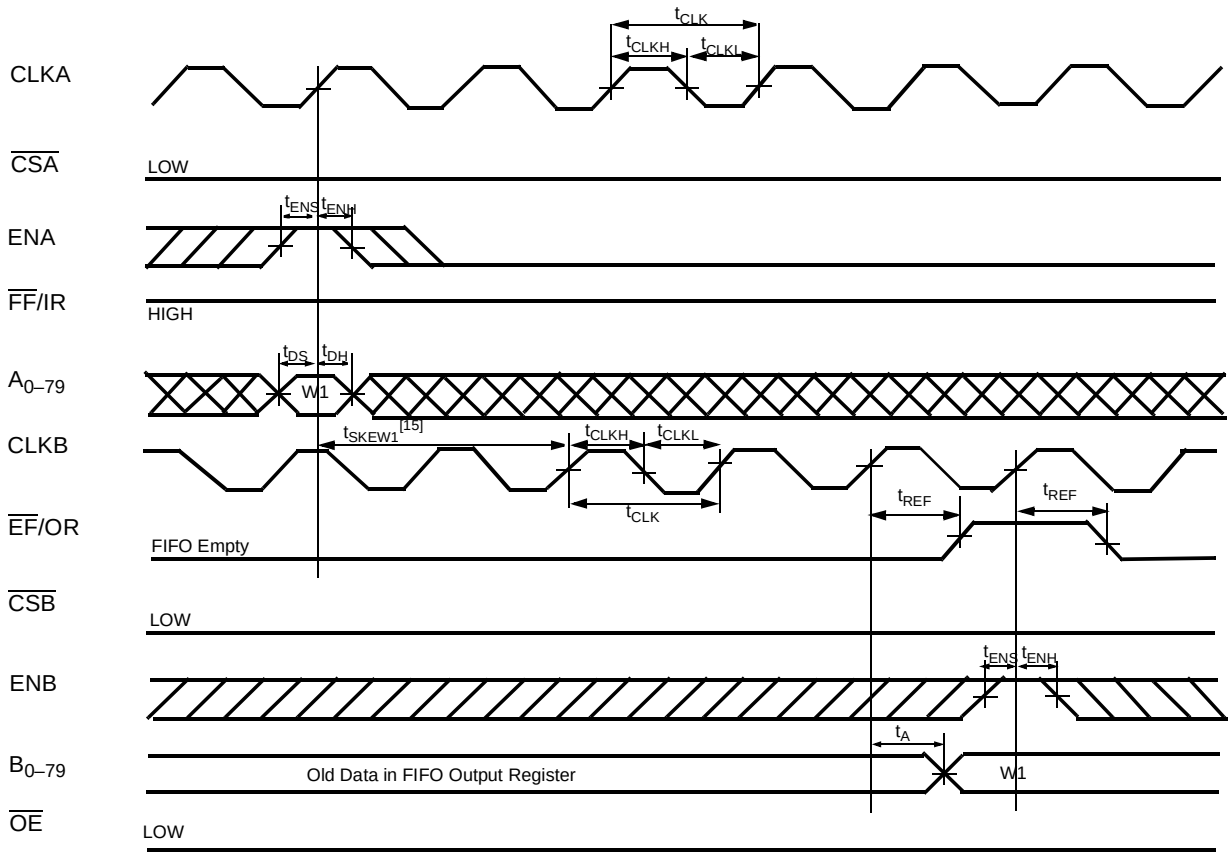


Notes:

12. Unused bits $B_{20–79}$ are zeroes for short word-size reads.
13. Unused bits $B_{10–79}$ are zeroes for byte-size reads.

Switching Waveforms (continued)

OR Flag Timing and First Data Word Fall Through when FIFO is Empty (FWFT Mode) [14]

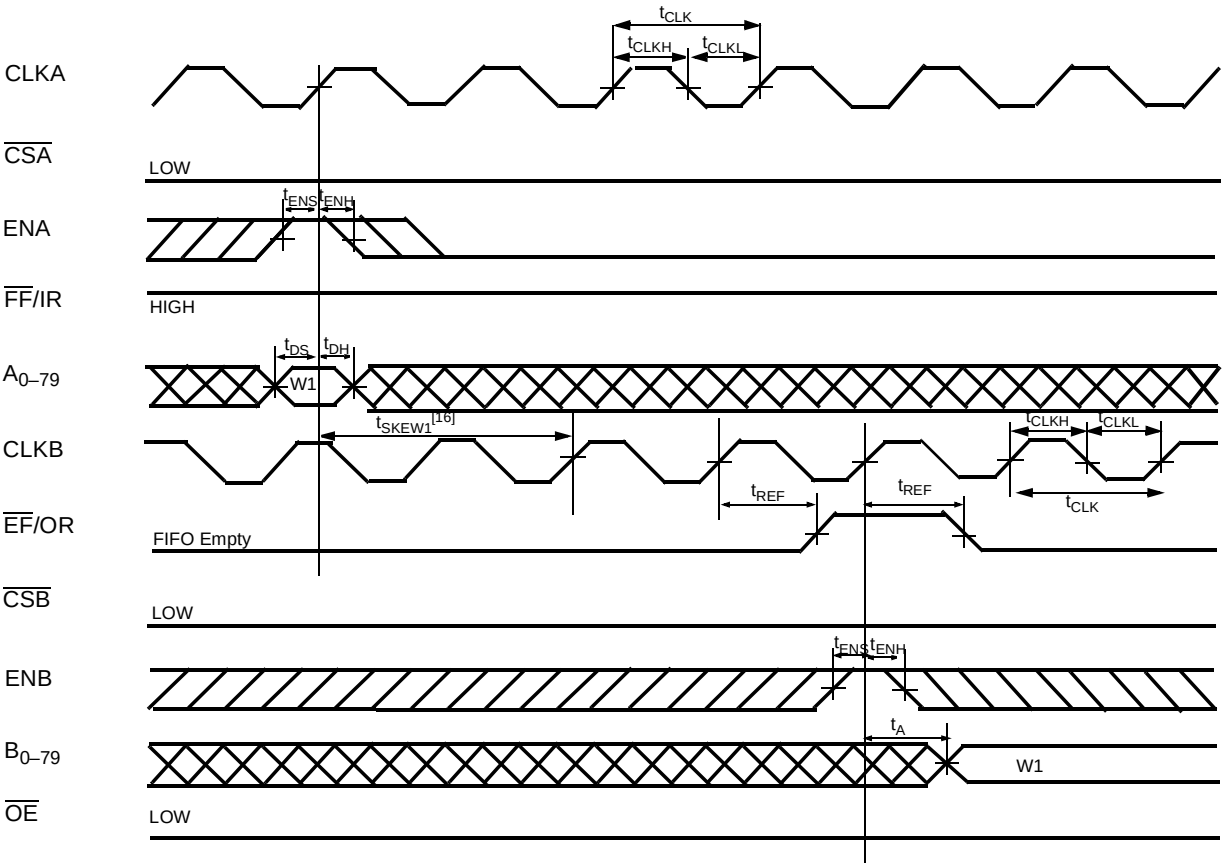


Notes:

14. If Port B size is word, short word or byte, $\overline{EF}$ is set LOW by the last word, short word or byte read from the FIFO, respectively.
15. t_{SKEW1} (7 ns minimum) is the time between a rising CLKA edge and a rising CLKB edge for OR flag to transition HIGH. If the time between these two edges is less than t_{SKEW1}, then the transition of OR HIGH may occur one CLKB cycle later than shown. CLKA and CLKB above are assumed to run at 200MHz (5 ns cycle time), which results in OR flag being updated after the 4th CLKB edge. If the clock cycles are more than 7 ns, OR flag may get updated after the 3rd clock edge, depending on when the clock edges occur. In general, OR flag update cycle = (t_{SKEW1}) + (2 clock cycle) + (t_{REF}).

Switching Waveforms (continued)

$\overline{EF}$ Flag Timing and First Data Read Fall Through when FIFO is Empty (CY Standard Mode)[14]

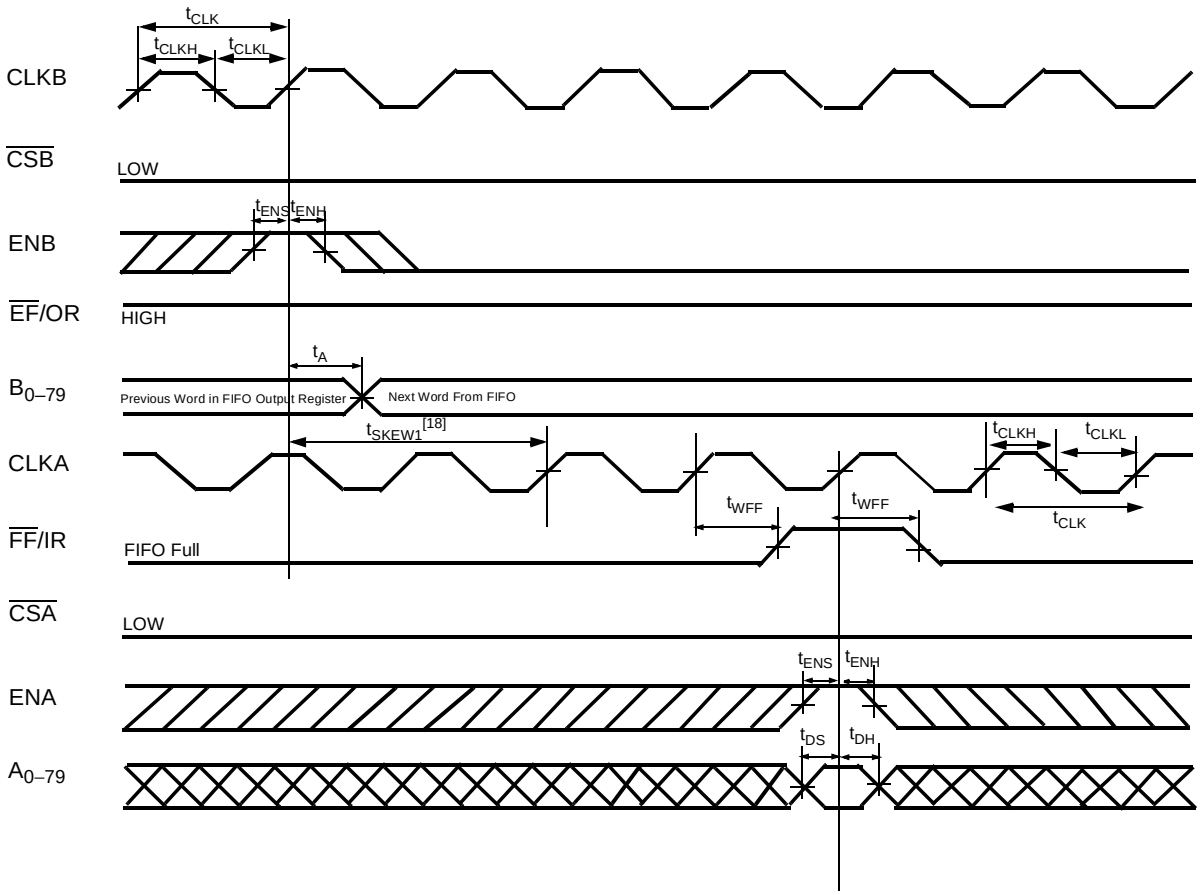


Notes:

16. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH. If the time between these two edges is less than t_{SKEW1}, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown. CLKA and CLKB above are assumed to run at 200 MHz (5 ns cycle time), which results in $\overline{EF}$ flag being updated after the 3rd CLKB edge. If the clock cycles are more than 7 ns, $\overline{EF}$ flag may get updated after the 2nd clock edge, depending on when the clock edges occur. In general, $\overline{EF}$ flag update cycle = (t_{SKEW1}) + (1 clock cycle) + (t_{REF}).

Switching Waveforms (continued)

$\overline{FF}$/IR Flag Timing and First Available Write when FIFO is Full (CY Standard and FWFT Mode) [17]

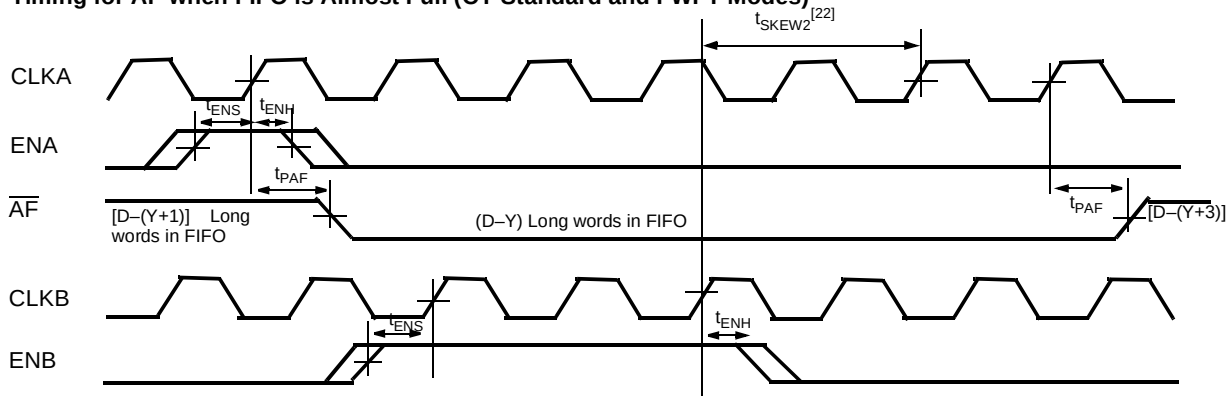


Notes:

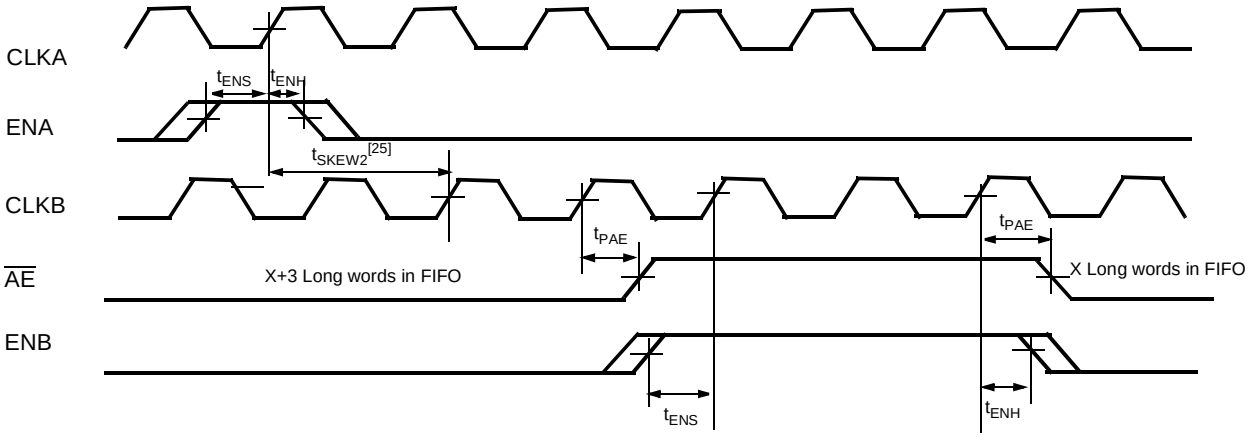
17. If Port B size is word, short word or byte, t_{SKEW1} is referenced to the rising CLKB edge that reads the last word, short word or byte write of the long-word, respectively.
18. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$/IR to transition HIGH. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{FF}$/IR HIGH may occur one CLKA cycle later than shown. CLKA and CLKB above are assumed to run at 200 MHz (5 ns cycle time), which results in $\overline{FF}$/IR flag being updated after the 3rd CLKA edge. If the clock cycles are more than 7 ns, $\overline{FF}$/IR flag may get updated after the 2nd clock edge, depending on when the clock edges occur. In general, $\overline{FF}$/IR flag update cycle = (t_{SKEW1}) + (1 clock cycle) + (t_{WFF}).

Switching Waveforms (continued)

Timing for $\overline{AF}$ when FIFO is Almost Full (CY Standard and FWFT Modes) [19, 20, 21]



Timing for $\overline{AE}$ when FIFO is Almost Empty (CY Standard and FWFT Modes) [23, 24]

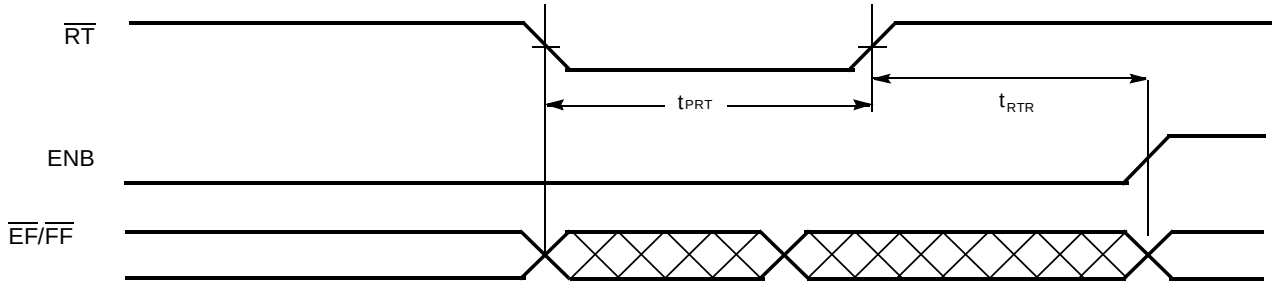


Notes:

19. FIFO Write ($\overline{CSA}$ = LOW) on Port A, FIFO read ($\overline{CSB}$ = LOW) on Port B. Data in the FIFO output register has been read from the FIFO.
20. D = Maximum FIFO Depth = 4K for the CY7C4804V25, 16K for the CY7C4806V25, and 64K for the CY7C4808V25.
21. If Port B size is word, short word or byte, t_{SKEW2} is referenced to the rising CLKB edge that writes the last word, short word or byte of the long word, respectively.
22. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between these two edges is less than t_{SKEW2}, then $\overline{AF}$ may transition HIGH one CLKB cycle later than shown. CLKA and CLKB above are assumed to run at 200MHz (5 ns cycle time), which results in $\overline{AF}$ flag being updated after the 3rd CLKA edge. If the clock cycles are more than 7 ns, $\overline{AF}$ flag may get updated after the 2nd clock edge, depending on when the clock edges occur. In general, $\overline{AF}$ flag update cycle = (t_{SKEW2}) + (1 clock cycle) + (t_{PAF}).
23. FIFO Write ($\overline{CSA}$ = LOW) on Port A, FIFO read ($\overline{CSB}$ = LOW) on Port B. Data in the FIFO output register has been read from the FIFO.
24. If Port B size is word, short word or byte, $\overline{AE}$ is set LOW by the last word, short word or byte read from FIFO, respectively.
25. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown. CLKA and CLKB above are assumed to run at 200 MHz (5 ns cycle time), which results in $\overline{AE}$ flag being updated after the 3rd CLKB edge. If the clock cycles are more than 7 ns, $\overline{AE}$ flag may get updated after the 2nd clock edge, depending on when the clock edges occur. In general, $\overline{AE}$ flag update cycle = (t_{SKEW2}) + (1 clock cycle) + (t_{PAE}).

Switching Waveforms (continued)

FIFO Retransmit Timing[26, 27, 28]



Notes:
26. Clocks are free-running in this case.
27. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTR}.
28. For the AE and AF flags, two clock cycles are necessary after t_{RTR} to update these flags.

Signal Description

Master Reset ($\overline{MR}$)

The FIFO memory of the CY7C480XV25 undergoes a complete reset by taking its associated Master Reset ($\overline{MR}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Master Reset input can switch asynchronously to the clocks. A Master Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost Empty flag ($\overline{AE}$) LOW, and the Almost Full flag ($\overline{AF}$) HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation. A Master Reset must be performed on the FIFO after power up, before data is written to its memory.

A LOW-to-HIGH transition on a FIFO Master Reset ($\overline{MR}$) input latches the value of the Big Endian (BE) input, determining the order by which bytes are transferred through Port B.

A LOW-to-HIGH transition on a FIFO reset ($\overline{MR}$) input latches the values of the Flag Select (FS0, FS1) and Serial Programming Mode ($\overline{SPM}$) inputs for choosing the Almost Full and Almost Empty offset programming method (see Almost Empty and Almost Full flag offset programming below).

Partial Reset ($\overline{PR}$)

Each of the two FIFO memories of the CY7C480XV25 undergoes a limited reset by taking its associated Partial Reset ($\overline{PR}$) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Partial Reset inputs can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FF}$/IR) LOW, the Empty/Output Ready flag ($\overline{EF}$/OR) LOW, the Almost Empty flag ($\overline{AE}$) LOW, and the Almost Full flag ($\overline{AF}$) HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two clock cycles to begin normal operation.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or CY Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Master Reset would be inconvenient.

Big Endian/First-Word Fall-Through (BE/$\overline{FWFT}$)

This is a dual-purpose pin. At the time of Master Reset, the BE select function is active, permitting a choice of Big or Little Endian byte arrangement for data written to or read from either one of the ports. This selection determines the order by which bytes (or short words or words) of data are transferred through this port. For the following examples, assume that a byte (or short words or word) bus size has been selected for Port B. (Note that when Port B is configured for a long-word size, the Big Endian function has no application and the BE input is a "don't care".)

A HIGH on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MR}$) input goes from LOW to HIGH will select a Big Endian arrangement. When data is moving from Port A to Port B, the most significant byte (short word/word) of the long-word written to Port A will be transferred to Port B first; the least significant byte (short word/word) of the long-word written to Port A will be transferred to Port B last.

A LOW on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MR}$) input goes from LOW to HIGH will select a Little Endian arrangement. When data is moving from Port A to Port B, the least significant byte (short word/word) of the long-word written to Port A will be transferred to Port B first; the most significant byte (short word/word) of the long-word written to Port A will be transferred to Port B last.

After Master Reset, the FWFT select function is active, permitting a choice between two possible timing modes: CY Standard Mode or First-Word Fall-Through (FWFT) Mode. Once the Master Reset ($\overline{MR}$) input is HIGH, a HIGH on the BE/$\overline{FWFT}$ input at the second LOW-to-HIGH transition of CLKA will select CY Standard Mode. This mode uses the Empty Flag function ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In CY Standard Mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Master Reset ($\overline{MR}$) input is HIGH, a LOW on the BE/$\overline{FWFT}$ input LOW-to-HIGH transition of CLKA will select FWFT Mode. This mode uses the Output Ready function (OR) to indicate whether or not there is valid data at the data outputs ($B_{0–79}$). It also uses the Input Ready function (IR) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Master Reset, the level applied to the BE/$\overline{FWFT}$ input to choose the desired timing mode must remain static throughout the FIFO operation.

Programming the Almost Empty and Almost Full Flags

Two registers in the CY7C480XV25 are used to hold the offset values for the Almost Empty and Almost Full flags. The Port A Almost Empty flag ($\overline{AE}$) offset register is labeled X. The Port B Almost Full flag ($\overline{AF}$) offset register is labeled Y. The index of each register name corresponds with preset values during the reset of a FIFO, programmed in parallel using the FIFO's Port A data inputs, or programmed in serial using the Serial Data (SD) input (see *Table 2*).

To load a FIFO's Almost Empty flag and Almost Full flag offset registers with one of the three preset values listed in *Table 2*, the Serial Program Mode ($\overline{SPM}$) and at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of its Master Reset input ($\overline{MR}$). For example, to load the preset value of 64 into X and Y, $\overline{SPM}$, FS0, and FS1 must be HIGH when the FIFO reset ($\overline{MR}$) returns HIGH.

To program the X and Y registers from Port A, perform a Master Reset with $\overline{SPM}$ HIGH and FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{MR}$. After this reset is complete, the first two writes to the FIFO do not store data in memory but load the offset registers in the order Y and X. The Port A data inputs used by the offset registers are ($A_{0–11}$), ($A_{0–13}$), or ($A_{0–15}$),for the CY7C480XV25, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 0 to 4095 for the CY7C4804V25; 0 to 16383 for the CY7C4806V25; 0 to 65535 for the CY7C4808V25. Before programming the offset registers, $\overline{FF}$/IR is set HIGH. FIFOs begin normal operation after programming is complete.

To program the X and Y registers serially, initiate a Master Reset with $\overline{SPM}$ LOW, FS0/SD LOW, and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{MR}$. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. Twenty-four, twenty-eight or thirty-two bit writes are needed to complete the programming. The two registers are written in the order Y then finally X. The first-bit write stores the most significant bit of the Y register and the last-bit write stores the least significant bit of the X register.

When the option to program the offset registers serially is chosen, the Port A Full/Input Ready ($\overline{FF}$/IR) flag remains LOW until all register bits are written. $\overline{FF}$/IR is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO operation.

$\overline{SPM}$, FS0/SD, and FS1/$\overline{SEN}$ function the same way in both CY Standard and FWFT modes.

FIFO Write/Read Operation

The state of the Port A data ($A_{0–79}$) lines is controlled by Port A Chip Select ($\overline{CSA}$) and Output Enable ($\overline{OE}$). The $A_{0–79}$ lines are in the high-impedance state when either $\overline{CSA}$ or $\overline{OE}$ is HIGH.

Data is loaded into the FIFO from the $A_{0–79}$ inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, ENA is HIGH, and $\overline{FF}$/IR is HIGH (see *Table 3*). FIFO writes on Port A are independent of any concurrent Port B operation.

The Port B control signals are identical to those of Port A. The state of the Port B data ($B_{0–79}$) lines is controlled by the Port B Chip Select ($\overline{CSB}$) and Output Enable ($\overline{OE}$). The $B_{0–79}$ lines are in the high-impedance state when $\overline{CSB}$ or $\overline{OE}$ is HIGH. The $B_{0–79}$ lines are active outputs when $\overline{CSB}$ or $\overline{OE}$ is LOW.

Data is transferred to the $B_{0–79}$ outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{OE}$ is LOW, ENB is HIGH, and $\overline{EF}$/OR is HIGH (see *Table 4*). FIFO reads and writes on Port B are independent of any concurrent Port A operation.

The set-up and hold time constraints to the port clocks for the port Chip Selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's Chip Select may change states during the set-up and hold time window of the cycle.

When operating the FIFO in FWFT Mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of CLKB, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, and Enable.

When operating the FIFO in CY Standard Mode, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using the port's Chip Select, and Enable.

Synchronized FIFO Flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of the metastable events when CLKA and CLKB operate asynchronously to one another. $\overline{EF}$/OR and $\overline{AE}$ are synchronized to CLKA. $\overline{FF}$/IR and $\overline{AF}$ are synchronized to CLKB. *Table 5* shows the relationship of each port flag to the FIFO.

Empty/Output Ready Flags ($\overline{EF}$/OR)

These are dual-purpose flags. In the FWFT Mode, the Output Ready (OR) function is selected. When the Output Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the CY Standard Mode, the Empty Flag ($\overline{EF}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's memory for reading to the output register. When Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to CLKB. For both the FWFT and CY Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO status is empty, empty+1, or empty+2.

In FWFT Mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB. Therefore, the CLKB Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of CLKB occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In the CY Standard Mode, from the time a word is written to a FIFO, the Empty flag will indicate the presence of data available for reading in a minimum of two cycles of CLKB. Therefore, an Empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles have not elapsed since the time the word was written. The Empty flag of the FIFO remains LOW until the second LOW-to-HIGH transition of CLKB occurs, forcing the Empty flag HIGH; only then can data be read.

A LOW-to-HIGH transition on the CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Full/Input Ready Flags ($\overline{FF}$/IR)

This is a dual-purpose flag. In FWFT Mode, the Input Ready (IR) function is selected. In CY Standard Mode, the Full Flag ($\overline{FF}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the memory to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to CLKA. For both FWFT and CY Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full–1, or full–2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles CLKA. Therefore, a Full/Input Ready flag is LOW if less than two cycles of

CLKA have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

Almost Empty Flags ($\overline{AE}$)

The Almost Empty flag of a FIFO is synchronized to CLKB. The state machine that controls an Almost Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost empty, almost empty+1, or almost empty+2. The Almost Empty state is defined by the contents of register X for $\overline{AE}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of CLKB are required after a FIFO write for its Almost Empty flag to reflect the new level of fill. Therefore, the Almost Full flag of a FIFO containing (X+1) or more words remains LOW if two cycles of CLKB have not elapsed since the write that filled the memory to the (X+1) level. An Almost Empty flag is set HIGH by the second LOW-to-HIGH transition of CLKB after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Almost Full Flags ($\overline{AF}$)

The Almost Full flag of a FIFO is synchronized to CLKA. The state machine that controls an Almost Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost full, almost full–1, or almost full–2. The Almost Full state is defined by the contents of register Y for $\overline{AF}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost Empty flag and Almost Full flag offset programming above). An Almost Full flag is LOW when the number of words in its FIFO is greater than or equal to (4096–Y), (16384–Y), or (65536–Y), for the CY7C480XV25 respectively. An Almost Full flag is HIGH when the number of words in its FIFO is less than or equal to [4096–(Y+1)], [16384–(Y+1)], or [65536–(Y+1)], for the CY7C480XV25 respectively.

Two LOW-to-HIGH transitions of CLKA are required after a FIFO read for its Almost Full flag to reflect the new level of fill. Therefore, the Almost Full flag of a FIFO containing [4096/16384/65536–(Y+1)] or less words remains LOW if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [4096/16384/65536–(Y+1)]. An Almost Full flag is set HIGH by the second LOW-to-HIGH transition of CLKA after the FIFO read that reduces the number of words in memory to [4096/16384/65536–(Y+1)]. A LOW-to-HIGH transition of CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [4096/16384/65536–(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

Bus Sizing

Both Port A and Port B buses can be configured in an 80-bit long-word, 40-bit word, 20-bit short word or 10-bit byte format. The levels applied to Bus Size Select (SIZE1A, SIZE2A, SIZE1B, SIZE2B) determine the bus size. Bus size on either port can be set independent of each other. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH.

Only 80-bit long-word data is written to or read from the two FIFO memories. Bus-matching operations are done before the data is written into the memory (for Port A) and after (for Port B) data is read from the memory.

Bus-Matching FIFO Reads

Data is read from the FIFO memory in 80-bit long-word increments. If a long-word bus size is implemented, the entire long-word immediately shifts to the FIFO output register. If byte or word size is implemented on Port B, only the first one or two bytes appear on the selected portion of the FIFO output register, with the rest of the long-word stored in auxiliary registers. In this case, subsequent FIFO reads output the rest of the long-word to the FIFO output register.

When reading data from the FIFO in the byte, short word, or word format, the unused outputs are zero.

Retransmit ($\overline{RT}$)

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last reset cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. CLKA and CLKB may be free running but ENB must be deasserted during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are transmitted also. The full depth of the FIFO can be repeatedly retransmitted.

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
1	0	0	x80	0	0	x80	Write to FIFO	ABCDEFGH
							Read from FIFO	ABCDEFGH
				0	1	x40	Read from FIFO	ABCD
								EFGH
				1	0	x20	Read from FIFO	AB
								CD
								EF
								GH
				1	1	x10	Read from FIFO	A
								B
								C
								D
								E
								F
								G
								H
	0	1	x40	0	0	x80	Write to FIFO	ABCD
								EFGH
							Read from FIFO	ABCDEFGH
				0	1	x40	Read from FIFO	ABCD
								EFGH
				1	0	x20	Read from FIFO	AB
								CD
								EF
								GH
				1	1	x10	Read from FIFO	A
								B
								C
								D
								E
								F
								G
								H

Note:
29. BE is selected at Master Reset; SIZE1A, SIZE2A, SIZE1B AND SIZE2B must be static throughout device operation.

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
	1	0	x20	0	0	x80	Write to FIFO	AB
								CD
								EF
								GF
							Read from FIFO	ABCDEFGH
				0	1	x40	Read from FIFO	ABCD
								EFGH
				1	0	x20	Read from FIFO	AB
								CD
								EF
								GH
				1	1	x10	Read from FIFO	A
								B
								C
								D
								E
								F
								G
								H

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
1	1	1	x10	0	0	x80	Write to FIFO	A
								B
								C
								D
								E
								F
								G
								H
							Read from FIFO	ABCDEFGH
				0	1	x40	Read from FIFO	ABCD
								EFGH
				1	0	x20	Read from FIFO	AB
								CD
								EF
								GH
				1	1	x10	Read from FIFO	A
								B
								C
								D
								E
								F
								G
								H

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
0	0	0	x80	0	0	x80	Write to FIFO	ABCDEFGH
							Read from FIFO	ABCDEFGH
				0	1	x40	Read from FIFO	EFGH
								ABCD
				1	0	x20	Read from FIFO	GH
								EF
								CD
								AB
				1	1	x10	Read from FIFO	H
								G
								F
								E
								D
								C
								B
								A
	0	1	x40	0	0	x80	Write to FIFO	ABCD
								EFGH
							Read from FIFO	EFGHABCD
				0	1	x40	Read from FIFO	ABCD
								EFGH
				1	0	x20	Read from FIFO	CD
								AB
								GH
								EF
				1	1	x10	Read from FIFO	D
								C
								B
								A
								H
								G
								F
								E

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
0	1	0	x20	0	0	x80	Write to FIFO	AB
								CD
								EF
								GH
							Read from FIFO	GH EF CD AB
				0	1	x40	Read from FIFO	CDAB
								GHEF
				1	0	x20	Read from FIFO	AB
								CD
								EF
								GH
				1	1	x10	Read from FIFO	B
								A
								D
								C
								F
								E
								H
								G
	1	1	x10	0	0	x80	Write to FIFO	A
								B
								C
								D
								E
								F
								G
								H
							Read from FIFO	HGFEDCBA
				0	1	x40	Read from FIFO	DCBA
								HGFE
				1	0	x20	Read from FIFO	BA
								DC
								FE
								HG

Table 1. Endian/Bus Matching Configuration[29]

Each character (“A”, “B”,..., “H”) represents 10-bit data								
BE/FWFT	**Size 1A**	**Size 2A**	**Port A**	**Size 1B**	**Size 2B**	**Port B**		**bit#79 bit#0**
0	1	1	x10	1	1	x10	Read from FIFO	A
								B
								C
								D
								E
								F
								G
								H

Table 2. Flag Programming

$\overline{SPM}$	FS1/$\overline{SEN}$	FS0/SD	$\overline{MR}$	X and Y Registers[30]
H	H	H	↑	64
H	H	L	↑	16
H	L	H	↑	8
H	L	L	↑	Parallel programming via Port A
L	H	L	↑	Serial programming via SD
L	H	H	↑	Reserved
L	L	H	↑	Reserved
L	L	L	↑	Reserved

Table 3. Port A Enable Function

$\overline{CSA}$	ENA	CLKA	A_{0-79} Inputs	Port Function
H	X	X	In high-impedance state	None
L	L	X	In high-impedance state	None
L	H	↑	In high-impedance state	FIFO write

Table 4. Port B Enable Function

$\overline{CSB}$	ENB	CLKB	B_{0-79} Inputs	Port Function
H	X	X	In high-impedance state	None
L	L	X	Active, FIFO output register	None
L	H	↑	Active, FIFO output register	FIFO read

Table 5. FIFO Flag Operation (CY Standard and FWFT Modes)

Number of Words in FIFO Memory[31, 32, 33, 34]			Synchronized to CLKB		Synchronized to CLKA	
CY7C4804V25	CY7C4806V25	CY7C4808V25	$\overline{EF}$/OR	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$/IR
0	0	0	L	L	H	H
1 TO X	1 TO X	1 TO X	H	L	H	H
(X+1) to [4096–(Y+1)]	(X+1) to [16834–(Y+1)]	(X+1) to [65536–(Y+1)]	H	H	H	H
(4096–Y1) to 4095	(16384–Y1) to 16383	(65536–Y1) to 65535	H	H	L	H
4096	16384	65536	H	H	L	L

Notes:
30. X register holds the offset for $\overline{AE}$; Y register holds the offset for $\overline{AF}$.
31. X is the Almost Empty offset for FIFO used by $\overline{AE}$. Y is the Almost Full offset for FIFO used by $\overline{AF}$. Both X and Y are selected during a FIFO reset or Port A programming.
32. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
33. Data in the output register does not count as a “word in FIFO memory”. Since in FWFT Mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
34. The OR and IR functions are active during FWFT mode; the $\overline{EF}$ and $\overline{FF}$ functions are active in CY Standard Mode.

2.5V 64K x80 Unidirectional Synchronous FIFO w/bus matching

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C4808V25-166BBC	BB288	288-Ball Grid Array (1.0 mm pitch, 19x19mm)	Commercial
200	CY7C4808V25-200BBC			
200	CY7C4808V25-200BBI	BB288	288-Ball Grid Array (1.0 mm pitch, 19x19mm)	Industrial

Shaded areas contain advance information.

2.5V 16K x80 Unidirectional Synchronous FIFO w/bus matching

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C4806V25-166BBC	BB288	288-Ball Grid Array (1.0 mm pitch, 19x19mm)	Commercial
200	CY7C4806V25-200BBC			

2.5V 4K x80 Unidirectional Synchronous FIFO w/bus matching

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C4804V25-166BBC	BB288	288-Ball Grid Array (1.0 mm pitch, 19x19mm)	Commercial
200	CY7C4804V25-200BBC	BB288		Commercial

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Package Diagram

288-Ball Grid Array (1.0 pitch, 19 x 19 mm) BB288