PRELIMINARY

CYM74BP54
CYM74P54/55
CYM74SP54/55

Intel® 82430NX Chipset Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74BP54), synchronous pipelined (CYM74P54, CYM74P55), or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins**
- **Ideal for Intel® P54C-based systems with the 82430NX (Neptune) chipset**
- **Operates at 60 and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chipset.

CYM74BP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution with industry standard 5V SRAMs and 3.3V level translators for CPU bus speeds up to 66 MHz. The CYM74BP54 is organized as 32K by 64-bits.

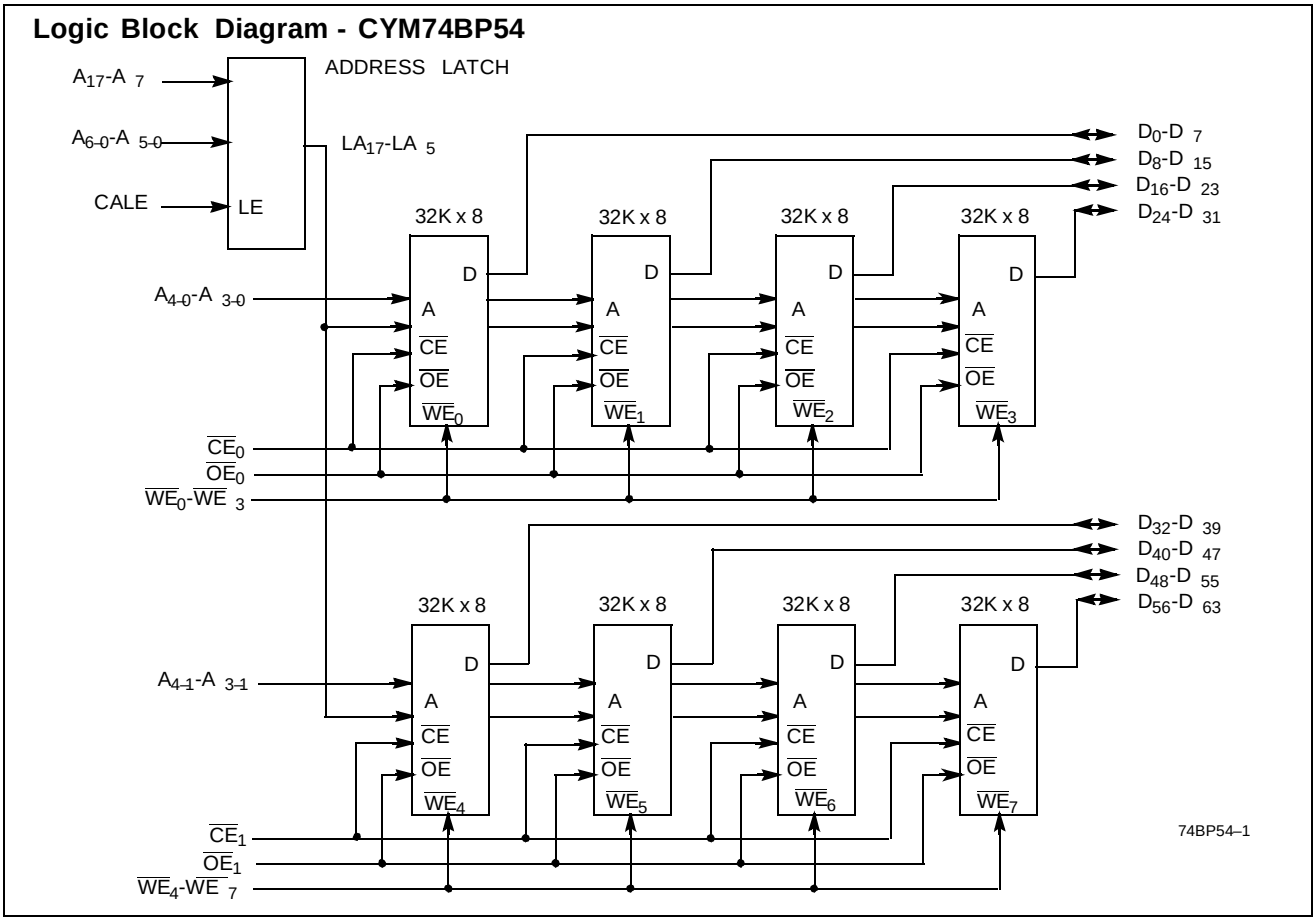
The synchronous modules are available with low-cost synchronous pipelined RAMs or higher performance synchronous burst RAMs. The synchronous pipelined modules are based on a 16Kx64 RAM. The CYM74P54 is a 256-KB module while the CYM74P55 is a 512-KB module. Both are modules without byte parity.

The CYM74SP54 and CYM74SP55 are synchronous burst cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity. The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (multifunctional) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram - CYM74BP54



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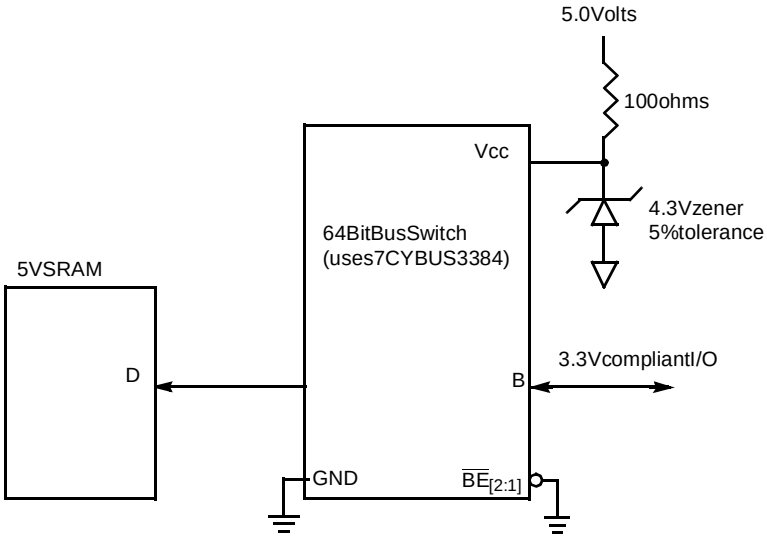
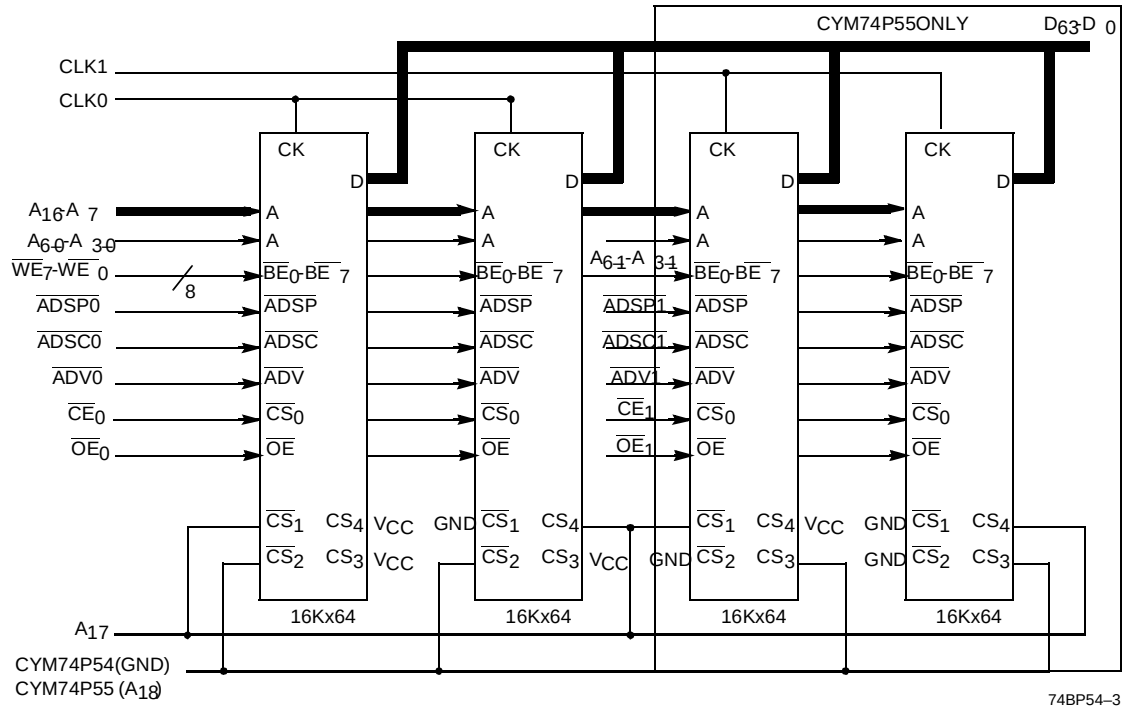
Block Diagram: 5V to 3.3V Level Conversion (CYM74BP54)

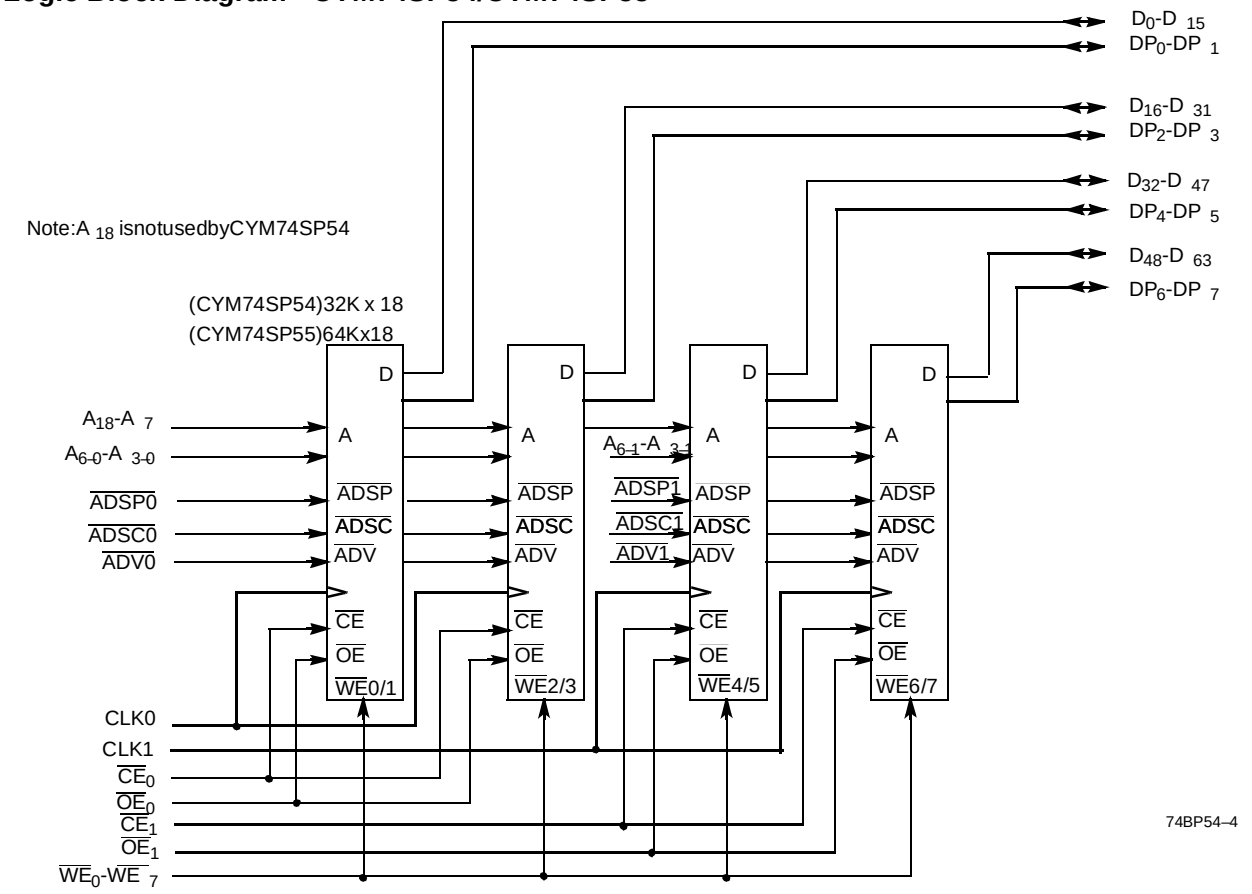


Logic Block Diagram - CYM74P54, CYM74P55

	PD_2	PD_1	PD_0
CYM74P54	TBD	TBD	TBD
CYM74P55	TBD	TBD	TBD



Logic Block Diagram - CYM74SP54/CYM74SP55



Selection Guide

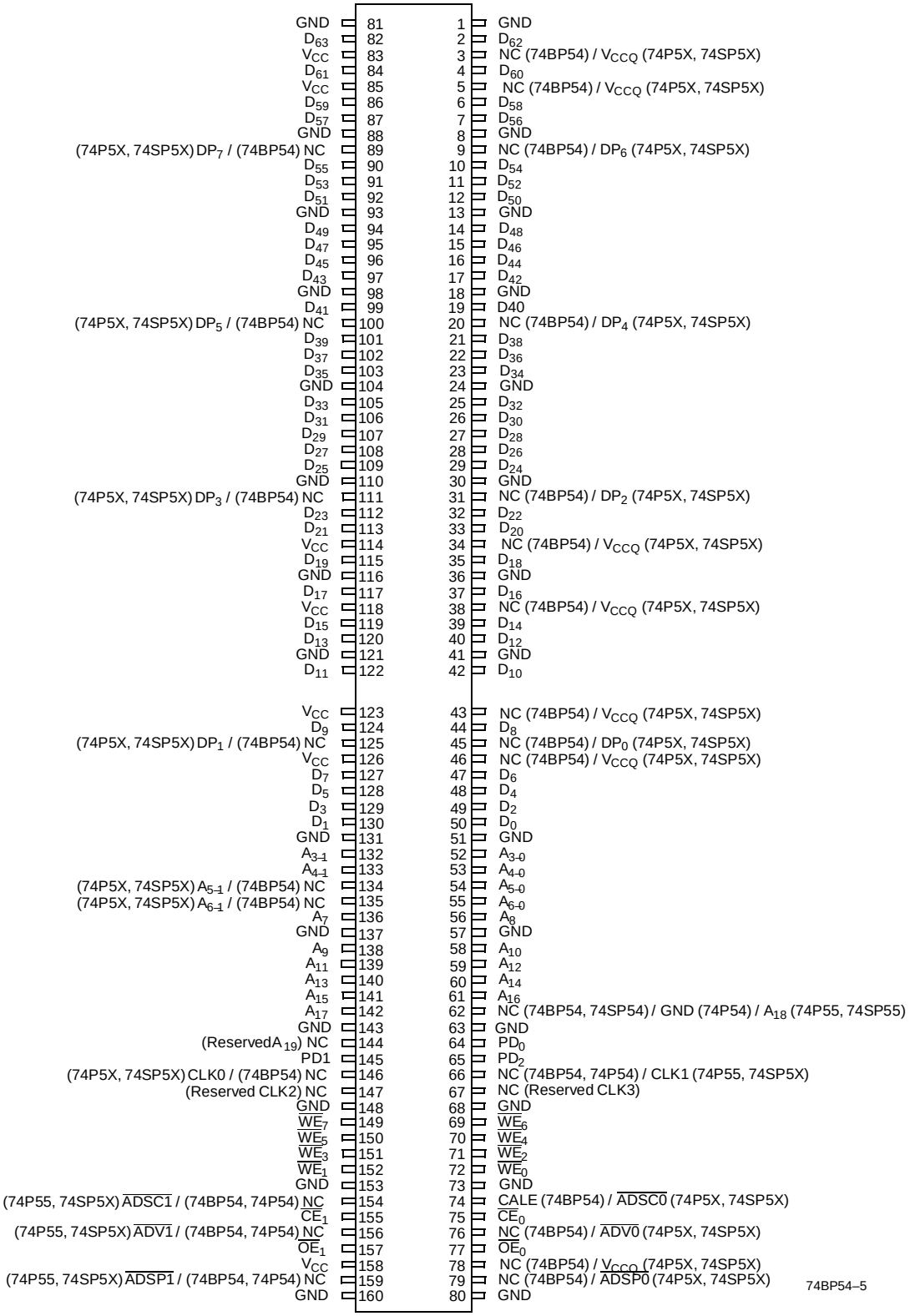
	Asynchronous Cache Modules	
Part Number	**CYM74BP54-60**	**CYM74BP54-66**
Cache Size (KB)	256	
System Clock (MHz)	60	66
RAM Speed	t_{AA}=15 ns	t_{AA}=12 ns

	Synchronous Pipelined Cache Modules			
Part Number	**CYM74P54-60**	**CYM74P54-66**	CYM74P55-60	CYM74P55-66
Cache Size (KB)	256		512	
System Clock (MHz)	60	66	60	66
RAM Speed	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns

	Synchornous Burst Cache Modules			
Part Number	**CYM74SP54-60**	**CYM74SP54-66**	CYM74SP55-60	CYM74SP55-66
Cache Size (KB)	256		512	
System Clock (MHz)	60	66	60	66
RAM Speed	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns

Pin Configuration

Dual Read–Out SIMM (DIMM)
Top View



74BP54–5

Pin Definitions

Common Signals	Description
V_{CC}	5V Supply
GND	Ground
A_7–A_{19}	Addresses from processor
A_{3-0}, A_{4-0}	Lower address from chipset, identical to the bank1 addresses
A_{3-1}, A_{4-1}	Lower address from chipset, identical to the bank0 addresses, A_{3-1}, A_{4-1} not used on CYM74P54
A_{5-0}, A_{6-0}	Lower address from processor (CYM74P5X, CYM74SP5X- identical to the bank1 addresses)
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable (same signal), $\overline{CE}_1$ not used on CYM74P54
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable (same signal), $\overline{OE}_1$ not used on CYM74P54
$\overline{WE}_0$, $\overline{WE}_1$,$\overline{WE}_2$,$\overline{WE}_3$ $\overline{WE}_4$,$\overline{WE}_5$,$\overline{WE}_6$,$\overline{WE}_7$	Byte Write Enables
PD_0–PD_2	Presence Detect pins
D_0–D_{63}	Data lines from processor
NC	Signal not connected on module.
CYM74BP54 Only Signals	**Description**
CALE	Latch Enable
CYM74P5X, CYM74SP5X Signals	**Description**
V_{CCQ}	3.3V Supply
DP_0–DP_7	Data Parity lines (Optional)
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Strobe, $\overline{ADSP1}$ not used on CYM74P54
$\overline{ADSC0}$,$\overline{ADSC1}$	Cache Controller Address Strobe, $\overline{ADSC1}$ not used on CYM74P54
$\overline{ADV0}$, $\overline{ADV1}$	Burst Address Advance, $\overline{ADV1}$ not used on CYM74P54
A_{5-1}, A_{6-1}	Lower address from processor, identical to the bank0 addresses, A_{5-1}, A_{6-1} not used on CYM74P54
CLK0, CLK1, CLK2, CLK3	Clock signals (each should be given own clk driver); CLK0 used on CYM74P5X, CYM74SP5X; CLK1 not used on CYM74P54; CLK2 and CLK3 are RSVD

Presence Detect Pins

	PD_2	PD_1	PD_0
Asynchronous – CYM74BP54	NC	GND	NC
Synchronous Pipelined – CYM74P54	TBD	TBD	TBD
Synchronous Pipelined – CYM74P55	TBD	TBD	TBD
Synchronous Burst – CYM74SP54	GND	GND	NC
Synchronous Burst – CYM74SP55	GND	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –0°C to +70°C

3.3V Supply Voltage to Ground Potential..... –0.5V to +5.25V

5V Supply Voltage to Ground Potential..... –0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +4.6V

DC Input Voltage..... –0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}	V_{CCQ}
Commercial (CYM74BP54)	0°C to +70°C	5V ± 5%	N/A
Commercial (CYM74P5X, CYM74SP5X)	0°C to +70°C	5V ± 5%	5V ± 5% 3.3V + 10% – 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2		V
V_{IL}	Input LOW Voltage	CYM74BP54	-0.5	0.8	V
V_{IL}	Input LOW Voltage	CYM74P5X, CYM74SP5X	-0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = -4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
$I_{CC\ (74BP54)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1700	mA
$I_{CC\ (74P54)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD	mA
$I_{CC\ (74P55)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		TBD	mA
$I_{CC\ (74SP54)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1100	mA
$I_{CC\ (74SP55)}$	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1400	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74BP54PM-60	PM36	160-Pin Dual-Readout SIMM	Asynchronous 256KB	Commercial
	CYM74P54PM-60	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 256KB	
	CYM74P55PM-60	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 512KB	
	CYM74SP54PM-60	PM26	160-Pin Dual-Readout SIMM	Synch Burst 256KB	
	CYM74SP55PM-60	PM26	160-Pin Dual-Readout SIMM	Synch Burst 512KB	
66	CYM74BP54PM-66	PM36	160-Pin Dual-Readout SIMM	Asynchronous 256KB	Commercial
	CYM74P54PM-66	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 256KB	
	CYM74P55PM-66	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 512KB	
	CYM74SP54PM-66	PM26	160-Pin Dual-Readout SIMM	Synch Burst 256KB	
	CYM74SP55PM-66	PM26	160-Pin Dual-Readout SIMM	Synch Burst 512KB	

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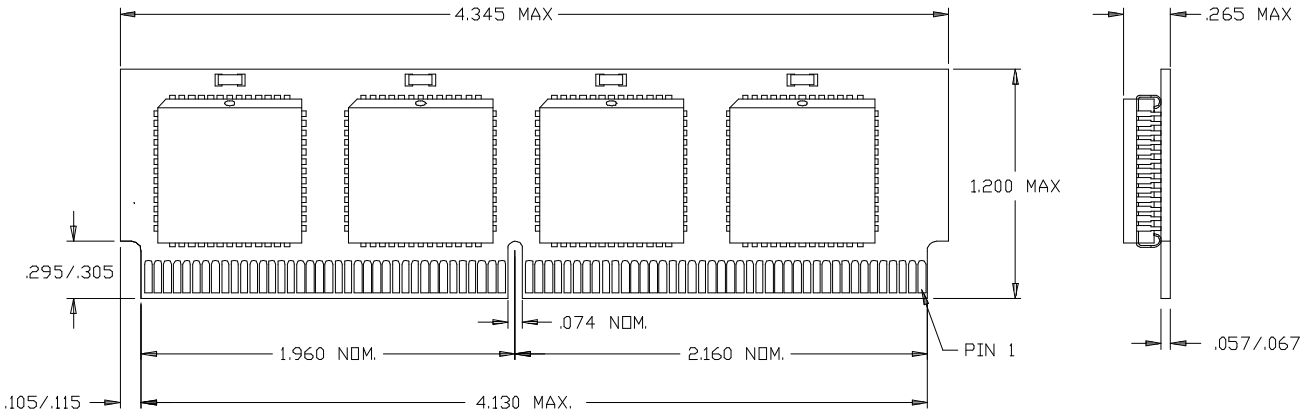
Package Diagrams

160-Pin Dual-Readout SIMM PM26



160-Pin Dual Readout SIMM PM36