



**PRELIMINARY**

**CYM74BP54  
CYM74P54/55  
CYM74SP54/55**

## Intel® 82430NX Chipset Level II Cache Module Family

### Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74BP54), synchronous pipelined (CYM74P54, CYM74P55), or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins
- Ideal for Intel® P54C-based systems with the 82430NX (Neptune) chipset
- Operates at 60 and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

### Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chipset.

CYM74BP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution with in-

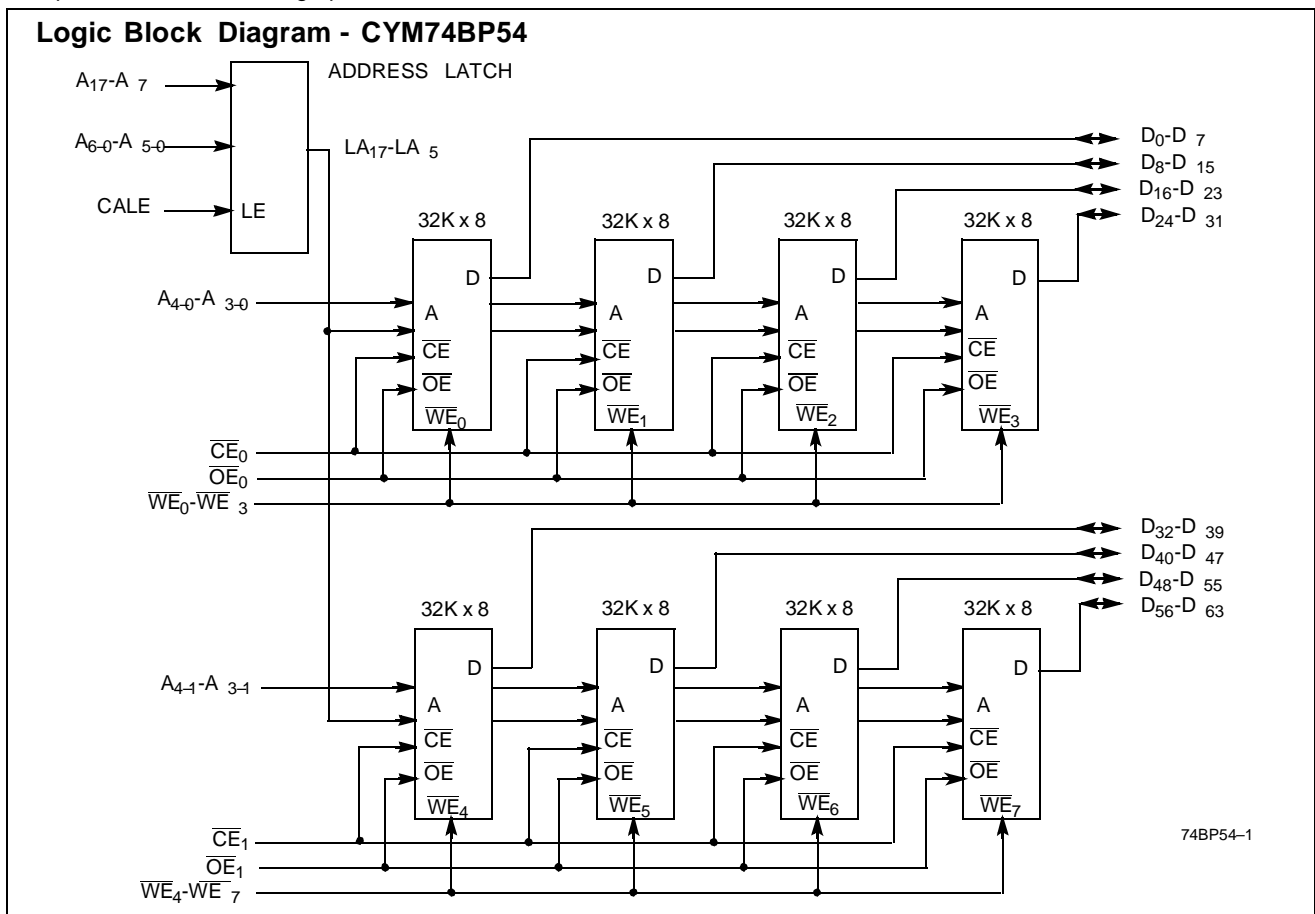
dustry standard 5V SRAMs and 3.3V level translators for CPU bus speeds up to 66 MHz. The CYM74BP54 is organized as 32K by 64-bits.

The synchronous modules are available with low-cost synchronous pipelined RAMs or higher performance synchronous burst RAMs. The synchronous pipelined modules are based on a 16Kx64 RAM. The CYM74P54 is a 256-KB module while the CYM74P55 is a 512-KB module. Both are modules without byte parity.

The CYM74SP54 and CYM74SP55 are synchronous burst cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity. The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (multifunctional) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.



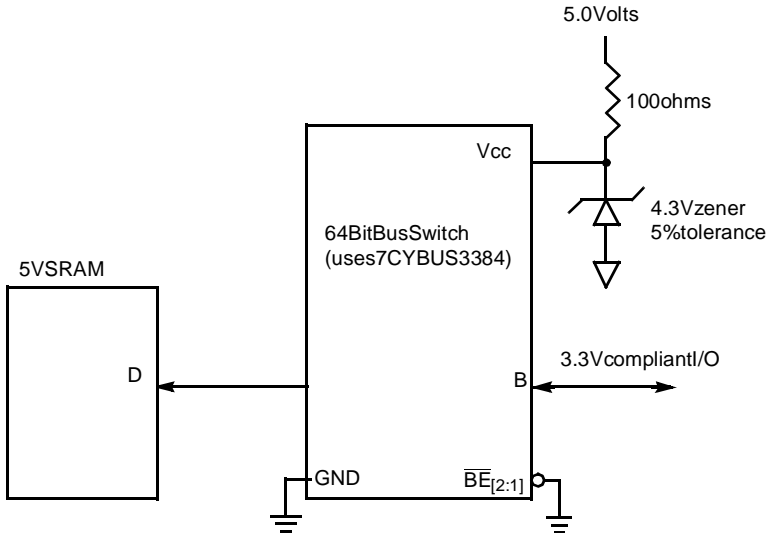
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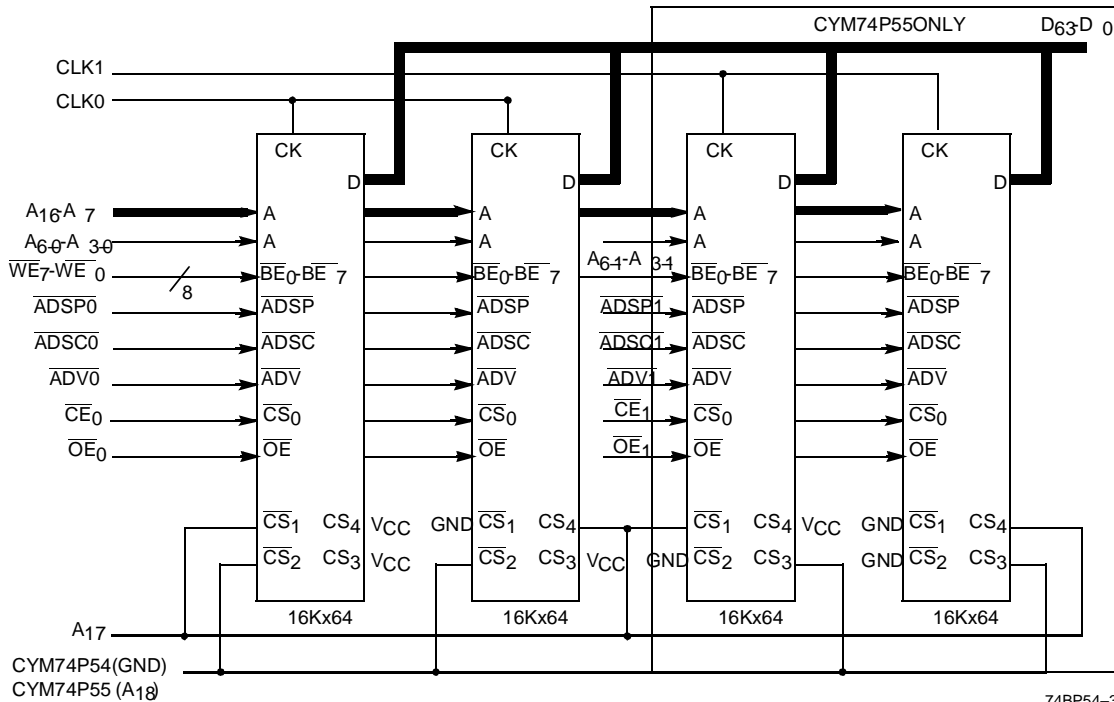
**Block Diagram: 5V to 3.3V Level Conversion (CYM74BP54)**



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**Logic Block Diagram - CYM74P54, CYM74P55**

	PD2	PD1	PD0
CYM74P54	TBD	TBD	TBD
CYM74P55	TBD	TBD	TBD

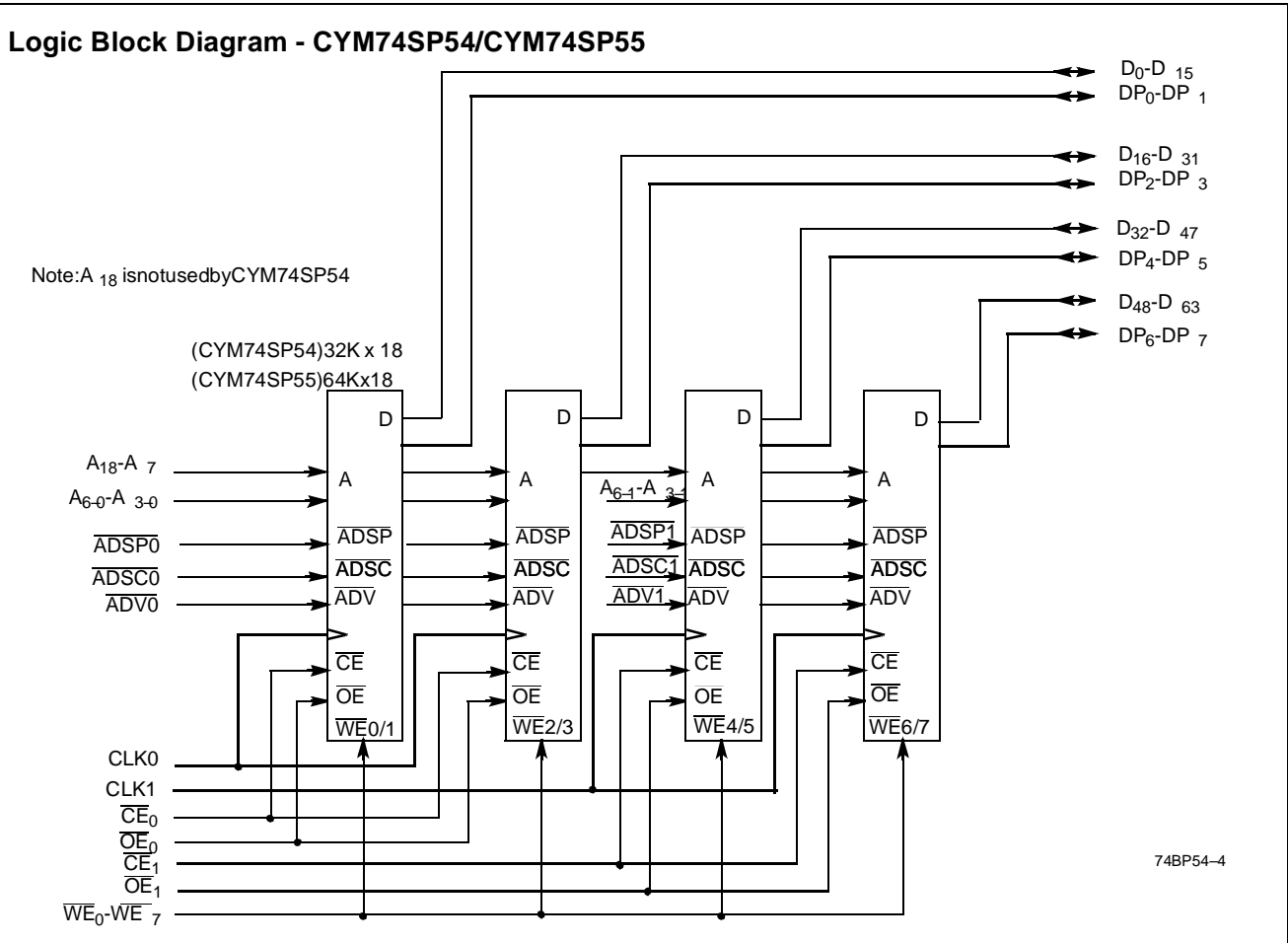


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**Selection Guide**

Asynchronous Cache Modules		
Part Number	CYM74BP54-60	CYM74BP54-66
Cache Size (KB)	256	
System Clock (MHz)	60	66
RAM Speed	t <sub>AA</sub> =15 ns	t <sub>AA</sub> =12 ns

Synchronous Pipelined Cache Modules				
Part Number	CYM74P54-60	CYM74P54-66	CYM74P55-60	CYM74P55-66
Cache Size (KB)	256		512	
System Clock (MHz)	60	66	60	66
RAM Speed	t <sub>CDV</sub> =10.5 ns	t <sub>CDV</sub> =8.5 ns	t <sub>CDV</sub> =10.5 ns	t <sub>CDV</sub> =8.5 ns

Synchronous Burst Cache Modules				
Part Number	CYM74SP54-60	CYM74SP54-66	CYM74SP55-60	CYM74SP55-66
Cache Size (KB)	256		512	
System Clock (MHz)	60	66	60	66
RAM Speed	t <sub>CDV</sub> =10.5 ns	t <sub>CDV</sub> =8.5 ns	t <sub>CDV</sub> =10.5 ns	t <sub>CDV</sub> =8.5 ns



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**Pin Configuration**

**Dual Read-Out SIMM (DIMM)  
Top View**

GND	81	1	GND
D <sub>63</sub>	82	2	D <sub>62</sub>
V <sub>CC</sub>	83	3	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
D <sub>61</sub>	84	4	D <sub>60</sub>
V <sub>CC</sub>	85	5	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
D <sub>59</sub>	86	6	D <sub>58</sub>
D <sub>57</sub>	87	7	D <sub>56</sub>
GND	88	8	GND
(74P5X, 74SP5X) DP <sub>7</sub> / (74BP54)	NC	9	NC (74BP54) / DP <sub>6</sub> (74P5X, 74SP5X)
D <sub>55</sub>	90	10	D <sub>54</sub>
D <sub>53</sub>	91	11	D <sub>52</sub>
D <sub>51</sub>	92	12	D <sub>50</sub>
GND	93	13	GND
D <sub>49</sub>	94	14	D <sub>48</sub>
D <sub>47</sub>	95	15	D <sub>46</sub>
D <sub>45</sub>	96	16	D <sub>44</sub>
D <sub>43</sub>	97	17	D <sub>42</sub>
GND	98	18	GND
D <sub>41</sub>	99	19	D <sub>40</sub>
(74P5X, 74SP5X) DP <sub>5</sub> / (74BP54)	NC	20	NC (74BP54) / DP <sub>4</sub> (74P5X, 74SP5X)
D <sub>39</sub>	101	21	D <sub>38</sub>
D <sub>37</sub>	102	22	D <sub>36</sub>
D <sub>35</sub>	103	23	D <sub>34</sub>
GND	104	24	GND
D <sub>33</sub>	105	25	D <sub>32</sub>
D <sub>31</sub>	106	26	D <sub>30</sub>
D <sub>29</sub>	107	27	D <sub>28</sub>
D <sub>27</sub>	108	28	D <sub>26</sub>
D <sub>25</sub>	109	29	D <sub>24</sub>
GND	110	30	GND
(74P5X, 74SP5X) DP <sub>3</sub> / (74BP54)	NC	31	NC (74BP54) / DP <sub>2</sub> (74P5X, 74SP5X)
D <sub>23</sub>	112	32	D <sub>22</sub>
D <sub>21</sub>	113	33	D <sub>20</sub>
V <sub>CC</sub>	114	34	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
D <sub>19</sub>	115	35	D <sub>18</sub>
GND	116	36	GND
D <sub>17</sub>	117	37	D <sub>16</sub>
V <sub>CC</sub>	118	38	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
D <sub>15</sub>	119	39	D <sub>14</sub>
D <sub>13</sub>	120	40	D <sub>12</sub>
GND	121	41	GND
D <sub>11</sub>	122	42	D <sub>10</sub>
V <sub>CC</sub>	123	43	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
(74P5X, 74SP5X) DP <sub>1</sub> / (74BP54)	D <sub>9</sub>	44	D <sub>8</sub>
NC	125	45	NC (74BP54) / DP <sub>0</sub> (74P5X, 74SP5X)
V <sub>CC</sub>	126	46	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
D <sub>7</sub>	127	47	D <sub>6</sub>
D <sub>5</sub>	128	48	D <sub>4</sub>
D <sub>3</sub>	129	49	D <sub>2</sub>
D <sub>1</sub>	130	50	D <sub>0</sub>
GND	131	51	GND
A <sub>3-1</sub>	132	52	A <sub>3-0</sub>
A <sub>4-1</sub>	133	53	A <sub>4-0</sub>
(74P5X, 74SP5X) A <sub>5-1</sub> / (74BP54)	NC	54	A <sub>5-0</sub>
(74P5X, 74SP5X) A <sub>6-1</sub> / (74BP54)	NC	55	A <sub>6-0</sub>
A <sub>7</sub>	136	56	A <sub>8</sub>
GND	137	57	GND
A <sub>9</sub>	138	58	A <sub>10</sub>
A <sub>11</sub>	139	59	A <sub>12</sub>
A <sub>13</sub>	140	60	A <sub>14</sub>
A <sub>15</sub>	141	61	A <sub>16</sub>
A <sub>17</sub>	142	62	NC (74BP54, 74SP54) / GND (74P54) / A <sub>18</sub> (74P55, 74SP55)
GND	143	63	GND
(Reserved A <sub>19</sub> )	NC	64	PD <sub>0</sub>
PD <sub>1</sub>	145	65	PD <sub>2</sub>
(74P5X, 74SP5X) CLK <sub>0</sub> / (74BP54)	NC	66	NC (74BP54, 74P54) / CLK <sub>1</sub> (74P55, 74SP5X)
(Reserved CLK <sub>2</sub> )	NC	67	NC (Reserved CLK <sub>3</sub> )
GND	148	68	GND
WE <sub>7</sub>	149	69	WE <sub>6</sub>
WE <sub>5</sub>	150	70	WE <sub>4</sub>
WE <sub>3</sub>	151	71	WE <sub>2</sub>
WE <sub>1</sub>	152	72	WE <sub>0</sub>
GND	153	73	GND
(74P55, 74SP5X) $\overline{\text{ADSC}}_1$ / (74BP54, 74P54)	NC	74	CALE (74BP54) / $\overline{\text{ADSC}}_0$ (74P5X, 74SP5X)
CE <sub>1</sub>	155	75	CE <sub>0</sub>
(74P55, 74SP5X) $\overline{\text{ADV}}_1$ / (74BP54, 74P54)	NC	76	NC (74BP54) / $\overline{\text{ADV}}_0$ (74P5X, 74SP5X)
OE <sub>1</sub>	157	77	OE <sub>0</sub>
V <sub>CC</sub>	158	78	NC (74BP54) / V <sub>CCQ</sub> (74P5X, 74SP5X)
(74P55, 74SP5X) $\overline{\text{ADSP}}_1$ / (74BP54, 74P54)	NC	79	NC (74BP54) / $\overline{\text{ADSP}}_0$ (74P5X, 74SP5X)
GND	160	80	GND

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**Pin Definitions**

Common Signals	Description
V <sub>CC</sub>	5V Supply
GND	Ground
A <sub>7</sub> -A <sub>19</sub>	Addresses from processor
A <sub>3-0</sub> , A <sub>4-0</sub>	Lower address from chipset, identical to the bank1 addresses
A <sub>3-1</sub> , A <sub>4-1</sub>	Lower address from chipset, identical to the bank0 addresses, A <sub>3-1</sub> , A <sub>4-1</sub> not used on CYM74P54
A <sub>5-0</sub> , A <sub>6-0</sub>	Lower address from processor (CYM74P5X, CYM74SP5X- identical to the bank1 addresses)
$\overline{CE}_0$ , $\overline{CE}_1$	Chip Enable (same signal), $\overline{CE}_1$ not used on CYM74P54
$\overline{OE}_0$ , $\overline{OE}_1$	Output Enable (same signal), $\overline{OE}_1$ not used on CYM74P54
$\overline{WE}_0$ , $\overline{WE}_1$ , $\overline{WE}_2$ , $\overline{WE}_3$ $\overline{WE}_4$ , $\overline{WE}_5$ , $\overline{WE}_6$ , $\overline{WE}_7$	Byte Write Enables
PD <sub>0</sub> -PD <sub>2</sub>	Presence Detect pins
D <sub>0</sub> -D <sub>63</sub>	Data lines from processor
NC	Signal not connected on module.
CYM74BP54 Only Signals	Description
CALE	Latch Enable
CYM74P5X, CYM74SP5X Signals	Description
V <sub>CCQ</sub>	3.3V Supply
DP <sub>0</sub> -DP <sub>7</sub>	Data Parity lines (Optional)
$\overline{ADSP0}$ , $\overline{ADSP1}$	Processor Address Strobe, $\overline{ADSP1}$ not used on CYM74P54
$\overline{ADSC0}$ , $\overline{ADSC1}$	Cache Controller Address Strobe, $\overline{ADSC1}$ not used on CYM74P54
$\overline{ADV0}$ , $\overline{ADV1}$	Burst Address Advance, $\overline{ADV1}$ not used on CYM74P54
A <sub>5-1</sub> , A <sub>6-1</sub>	Lower address from processor, identical to the bank0 addresses, A <sub>5-1</sub> , A <sub>6-1</sub> not used on CYM74P54
CLK0, CLK1, CLK2, CLK3	Clock signals (each should be given own clk driver); CLK0 used on CYM74P5X, CYM74SP5X; CLK1 not used on CYM74P54; CLK2 and CLK3 are RSVD

**Presence Detect Pins**

	PD <sub>2</sub>	PD <sub>1</sub>	PD <sub>0</sub>
Asynchronous – CYM74BP54	NC	GND	NC
Synchronous Pipelined – CYM74P54	TBD	TBD	TBD
Synchronous Pipelined – CYM74P55	TBD	TBD	TBD
Synchronous Burst – CYM74SP54	GND	GND	NC
Synchronous Burst – CYM74SP55	GND	GND	GND



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**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -55°C to +125°C
- Ambient Temperature with Power Applied ..... -0°C to +70°C
- 3.3V Supply Voltage to Ground Potential..... -0.5V to +5.25V
- 5V Supply Voltage to Ground Potential..... -0.5V to +5.25V
- DC Voltage Applied to Outputs in High Z State ..... -0.5V to +4.6V
- DC Input Voltage..... -0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>	V <sub>CCQ</sub>
Commercial (CYM74BP54)	0°C to +70°C	5V ± 5%	N/A
Commercial (CYM74P5X, CYM74SP5X)	0°C to +70°C	5V ± 5%	5V ± 5% 3.3V + 10% - 5%

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.2		V
V <sub>IL</sub>	Input LOW Voltage	CYM74BP54	-0.5	0.8	V
V <sub>IL</sub>	Input LOW Voltage	CYM74P5X, CYM74SP5X	-0.3	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min. I <sub>OH</sub> = -4 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min. I <sub>OL</sub> = 8 mA		0.4	V
I <sub>CC</sub> (74BP54)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1700	mA
I <sub>CC</sub> (74P54)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		TBD	mA
I <sub>CC</sub> (74P55)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		TBD	mA
I <sub>CC</sub> (74SP54)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1100	mA
I <sub>CC</sub> (74SP55)	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> =Max., I <sub>OUT</sub> =0 mA, f=f <sub>MAX</sub> =1/t <sub>RC</sub>		1400	mA

**Ordering Information**

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74BP54PM-60	PM36	160-Pin Dual-Readout SIMM	Asynchronous 256KB	Commercial
	CYM74P54PM-60	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 256KB	
	CYM74P55PM-60	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 512KB	
	CYM74SP54PM-60	PM26	160-Pin Dual-Readout SIMM	Synch Burst 256KB	
	CYM74SP55PM-60	PM26	160-Pin Dual-Readout SIMM	Synch Burst 512KB	
66	CYM74BP54PM-66	PM36	160-Pin Dual-Readout SIMM	Asynchronous 256KB	Commercial
	CYM74P54PM-66	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 256KB	
	CYM74P55PM-66	TBD	160-Pin Dual-Readout SIMM	Synch Pipelined 512KB	
	CYM74SP54PM-66	PM26	160-Pin Dual-Readout SIMM	Synch Burst 256KB	
	CYM74SP55PM-66	PM26	160-Pin Dual-Readout SIMM	Synch Burst 512KB	

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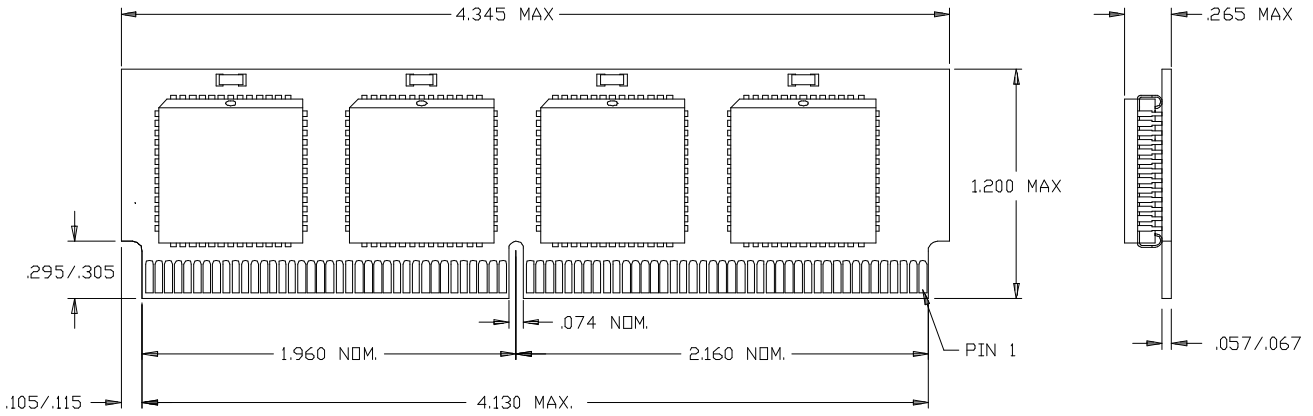


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**Package Diagrams**

**160-Pin Dual-Readout SIMM PM26**



**160-Pin Dual Readout SIMM PM36**

