# CYM1841A
# CYM1841B
# CYM1841C

## 256K x 32 Static RAM Module

### Features

- **High-density 8-megabit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.58 in.**
- **Available in ZIP, SIMM, and angled SIMM footprint**
- **72-pin SIMM version compatible with 1M x 32 (CYM1851)**

### Functional Description

The CYM1841A/B/C are high-performance 8-megabit static RAM modules organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs (1841A/C) or 256K x 16 SRAMs (1841B) in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the Input/Output pins (I/O) is written into the memory location specified on the address pins ($A_0$ through $A_{17}$).

Reading the device is accomplished by taking the Chip Select ($\overline{CS}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data Input/Output pins (I/O).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

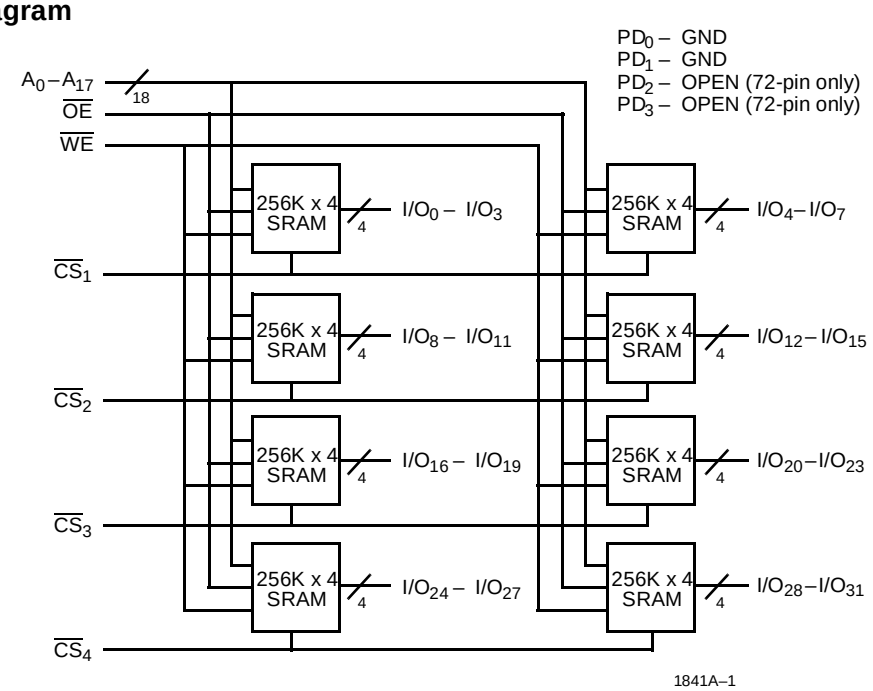
Two pins ($PD_0$ and $PD_1$) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

The CYM1841A, CYM1841B, and CYM1841C are 100% pin, package, and electrically identical. The CYM1841A utilizes corner power and ground SRAMs, the CYM1841B utilizes 256K x 16 SRAMs, the CYM1841C utilizes center power and ground SRAMs.

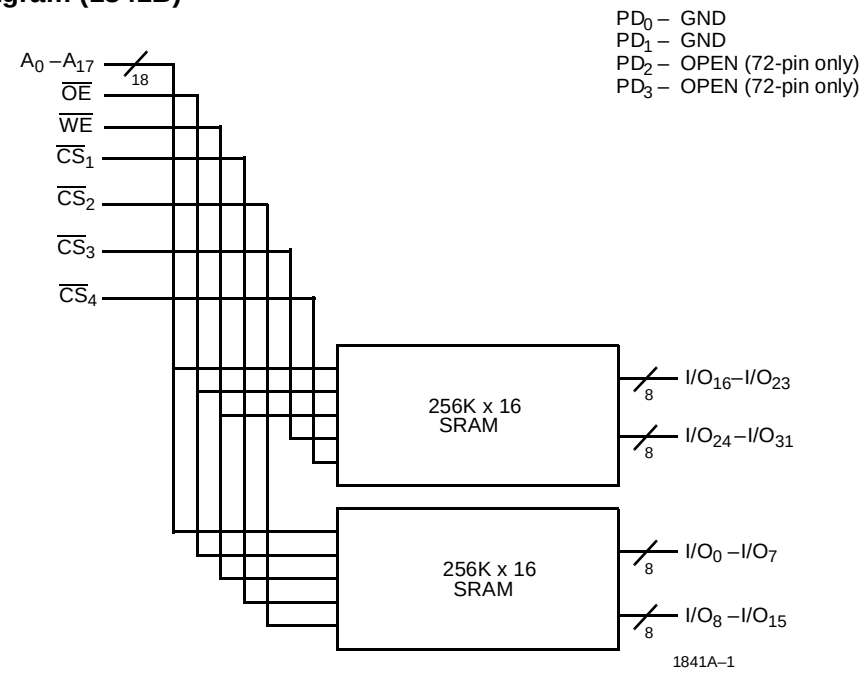
A 72-pin SIMM is offered for compatibility with the 1M x 32 CYM1851. This version is socket upgradable to the CYM1851.

Both the 64-pin and 72-pin SIMM modules are available with either tin-lead or 10 micro-inches of gold flash on the edge contacts.

### Logic Block Diagram



## Logic Block Diagram (1841B)



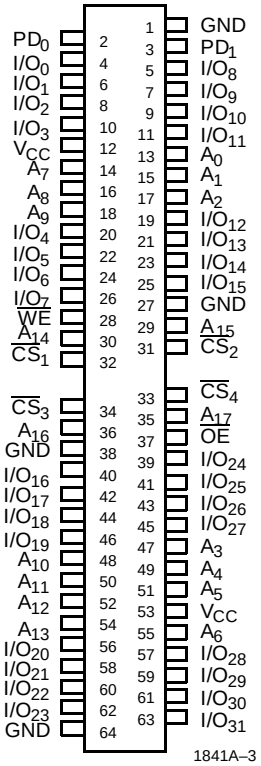

## Selection Guide

| | 1841C-12 | 1841B/C-15 | 1841A/B/C-20 | 1841A/B/C-25 | 1841A/B/C-35 | 1841A/B/C-45 |
|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | 12 | 15 | 20 | 25 | 35 | 45 |
| Maximum Operating Current (mA) | 1600 | 1600 | 1120 | 960 | 960 | 960 |
| Maximum Standby Current (mA) | 480 | 480 | 480 | 480 | 480 | 480 |

Shaded areas contain preliminary information.

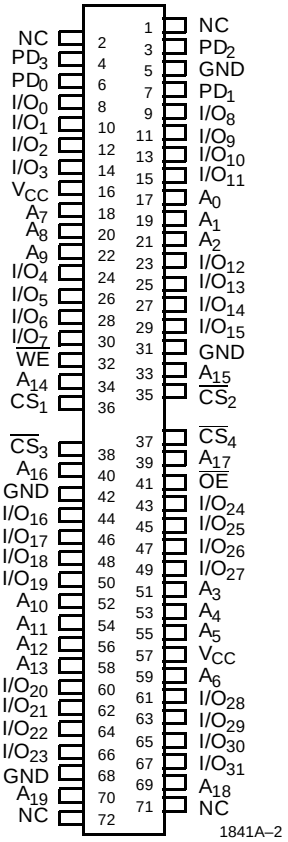
## Pin Configurations

**64-Pin ZIP/SIMM Top View**




1841A–3

**72-Pin SIMM Top View**




1841A–2

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –10°C to +85°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | 1841C-12 1841B/C-15 | | 1841A/B/C -20 | | 1841A/B/C -25, 35, 45 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –4.0 mA | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | –0.5 | 0.8 | –0.5 | 0.8 | –0.5 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –16 | +16 | –16 | +16 | –16 | +16 | mA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | –10 | +10 | –10 | +10 | –10 | +10 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, $\overline{CS}$ ≤ $V_{IL}$ | | 1600 | | 1120 | | 960 | mA |
| $I_{SB1}$ | Automatic $\overline{CS}$ Power-Down Current[1] | Max. $V_{CC}$, $\overline{CS}$ ≥ $V_{IH}$, Min. Duty Cycle = 100% | | 480 | | 480 | | 480 | mA |
| $I_{SB2}$ | Automatic $\overline{CS}$ Power-Down Current[1] | Max. $V_{CC}$, $\overline{CS}$ ≥ $V_{CC}$ - 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V, or $V_{IN}$ ≤ 0.2V | | 240 | | 200 | | 200 | mA |

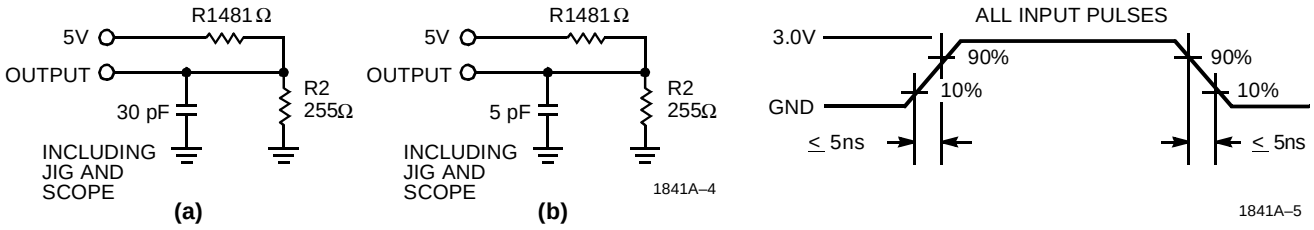
## Capacitance[2]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance[3] | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 70/20 | pF |
| $C_{OUT}$ | Output Capacitance | | 20 | pF |

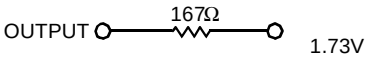
**Notes:**

1. A pull-up resistor to $V_{CC}$ on the $\overline{CS}$ input is required to keep the device deselected during $V_{CC}$ power-up, otherwise $I_{SB}$ will exceed values given.
2. Tested on a sample basis.
3. 20 pF on $\overline{CS}$, 70 pF all others.

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[4]

| Parameter | Description | 1841C-12 | | 1841B/C-15 | | 1841A/B/C-20 | | 1841A/B/C-25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{AA}$ | Address to Data Valid | | 12 | | 15 | | 20 | | 25 | ns |
| $t_{OHA}$ | Output Hold from Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{ACS}$ | $\overline{CS}$ LOW to Data Valid | | 12 | | 15 | | 20 | | 25 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 7 | | 8 | | 13 | | 15 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z | | 7 | | 8 | | 15 | | 15 | ns |
| $t_{LZCS}$ | $\overline{CS}$ LOW to Low Z[5] | 3 | | 3 | | 10 | | 10 | | ns |
| $t_{HZCS}$ | $\overline{CS}$ HIGH to High Z[5, 6] | | 7 | | 8 | | 20 | | 20 | ns |
| $t_{PD}$ | $\overline{CS}$ HIGH to Power-Down | | 12 | | 15 | | 20 | | 25 | |
| **WRITE CYCLE**[7] | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{SCS}$ | $\overline{CS}$ LOW to Write End | 9 | | 10 | | 15 | | 20 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 9 | | 10 | | 18 | | 20 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 10 | | 13 | | 15 | | 20 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 7 | | 8 | | 13 | | 15 | | ns |
| $t_{HD}$ | Data Hold from Write End | 1 | | 1 | | 2 | | 2 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[6] | 0 | 5 | 0 | 7 | 0 | 15 | 0 | 15 | ns |

Shaded areas contain preliminary information.

**Notes:**

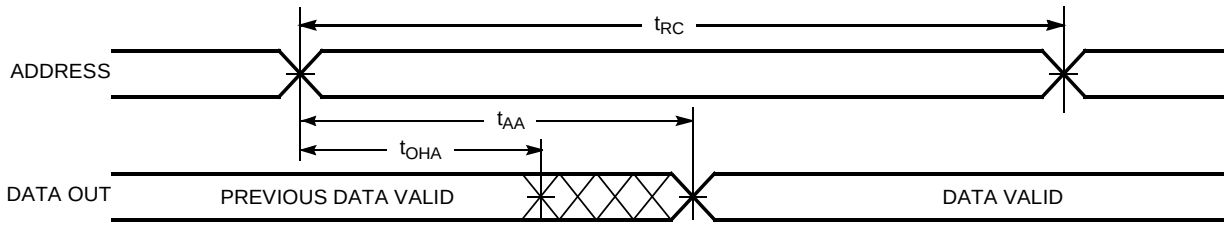
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
5. At any given temperature and voltage condition, $t_{HZCS}$ is less than $t_{LZCS}$ for any given device. These parameters are guaranteed by design and not 100% tested.
6. $t_{HZCS}$ and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Characteristics Over the Operating Range[4]

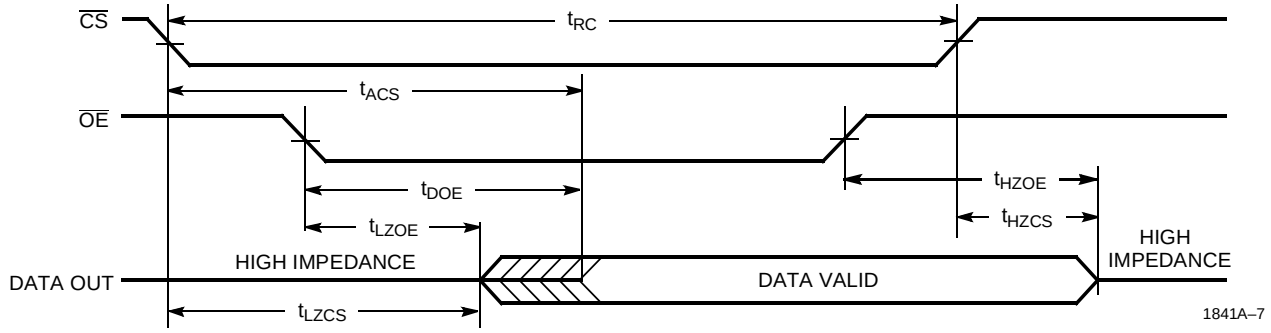
| Parameter | Description | 1841A/B/C-35 | | 1841A/B/C-45 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 35 | | 45 | | ns |
| $t_{AA}$ | Address to Data Valid | | 35 | | 45 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | 3 | | ns |
| $t_{ACS}$ | $\overline{CS}$ LOW to Data Valid | | 35 | | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 30 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 0 | | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ LOW to High Z | | 15 | | 15 | ns |
| $t_{LZCS}$ | $\overline{CS}$ LOW to Low Z[5] | 10 | | 10 | | ns |
| $t_{HZCS}$ | $\overline{CS}$ HIGH to High Z[5, 6] | | 20 | | 20 | ns |
| $t_{PD}$ | $\overline{CS}$ HIGH to Power-Down | | 35 | | 45 | ns |
| **WRITE CYCLE**[7] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 35 | | 45 | | ns |
| $t_{SCS}$ | $\overline{CS}$ LOW to Write End | 30 | | 40 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 30 | | 40 | | ns |
| $t_{HA}$ | Address Hold from Write End | 2 | | 2 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 2 | | 2 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 30 | | 35 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 20 | | 25 | | ns |
| $t_{HD}$ | Data Hold from Write End | 2 | | 2 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[6] | 0 | 15 | 0 | 15 | ns |

## Switching Waveforms

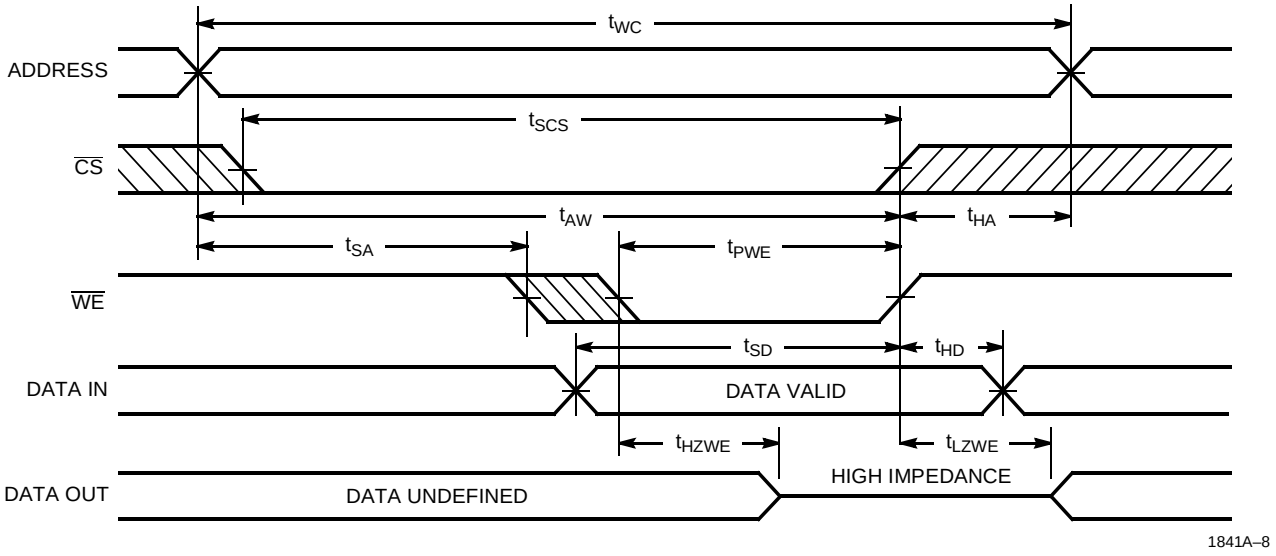
**Read Cycle No. 1**[8, 9]




**Read Cycle No. 2**[8, 10]



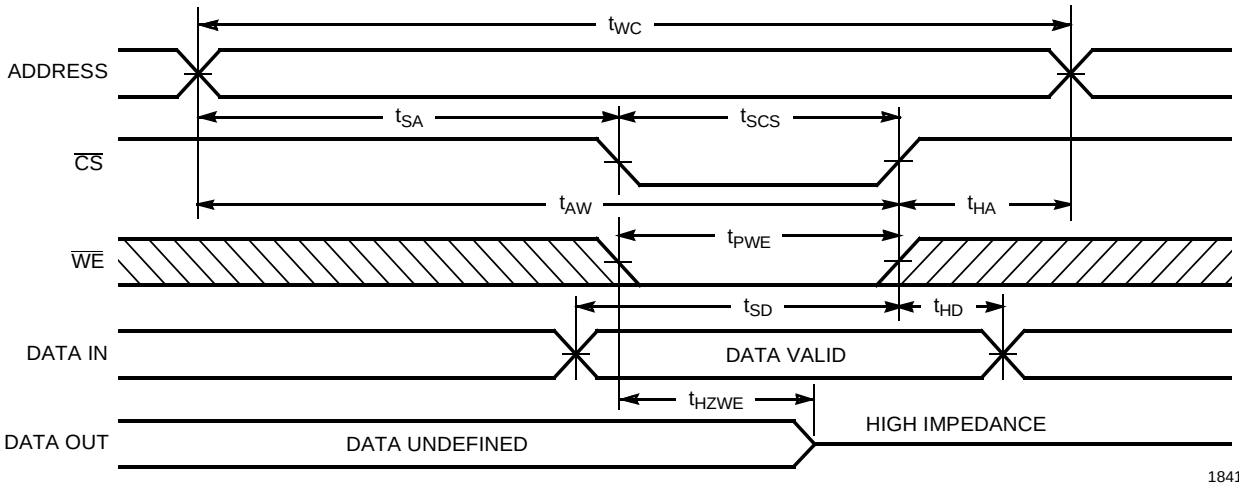

**Write Cycle No. 1 ($\overline{WE}$ Controlled)**[7]




**Notes:**
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

## Switching Waveforms (continued)

**Write Cycle No. 2 ($\overline{CS}$ Controlled)**[7, 11]




**Note:**
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

## Truth Table

| $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | Input/Output | Mode |
|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power-Down |
| L | H | L | Data Out | Read |
| L | L | X | Data In | Write |
| L | H | H | High Z | Deselect |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 12 | CYM1841CPM-12C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841CP7-12C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841CPZ-12C | PZ03 | 64-Pin Plastic ZIP Module | |
| 15 | CYM1841APM15C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841APY-15C | PM01 | 64-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APT-15C | PM01 | 64-Pin Plastic SIMM Module | |
| | CYM1841AP5-15C | PN04 | 72-Pin Plastic Angled SIMM Module | |
| | CYM1841AP6-15C | PM01 | 72-Pin Plastic Angled SIMM Module (gold contacts) | |
| | CYM1841AP7-15C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841AP8-15C | PM04 | 72-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APN-15C | PN02 | 64-Pin Plastic Angled SIMM Module | |
| | CYM1841APR-15C | PZ01 | 64-Pin Plastic ZIP Module | |
| | CYM1841APZ-15C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BPZ-15C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BP7-15C | PM04 | 72-Pin Plastic SIMM Module | |
| 20 | CYM1841APM-20C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841APY-20C | PM01 | 64-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APT-20C | PM01 | 64-Pin Plastic SIMM Module | |
| | CYM1841AP5-20C | PN04 | 72-Pin Plastic Angled SIMM Module | |
| | CYM1841AP6-20C | PM01 | 72-Pin Plastic Angled SIMM Module (gold contacts) | |
| | CYM1841AP7-20C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841AP8-20C | PM04 | 72-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APN-20C | PN02 | 64-Pin Plastic Angled SIMM Module | |
| | CYM1841APR-20C | PZ01 | 64-Pin Plastic ZIP Module | |
| | CYM1841APZ-20C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BPZ-20C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BP7-20C | PM04 | 72-Pin Plastic SIMM Module | |
| 25 | CYM1841APM-25C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841APY-25C | PM01 | 64-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APT-25C | PM01 | 64-Pin Plastic SIMM Module | |
| | CYM1841AP5-25C | PN04 | 72-Pin Plastic Angled SIMM Module | |
| | CYM1841AP6-25C | PM01 | 72-Pin Plastic Angled SIMM Module (gold contacts) | |
| | CYM1841AP7-25C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841AP8-25C | PM04 | 72-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APN-25C | PN02 | 64-Pin Plastic Angled SIMM Module | |
| | CYM1841APR-25C | PZ01 | 64-Pin Plastic ZIP Module | |
| | CYM1841APZ-25C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BPZ-25C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BP7-25C | PM04 | 72-Pin Plastic SIMM Module | |

Shaded areas contain preliminary information.

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 35 | CYM1841APM-35C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841APY-35C | PM01 | 64-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APT-35C | PM01 | 64-Pin Plastic SIMM Module | |
| | CYM1841AP5-35C | PN04 | 72-Pin Plastic Angled SIMM Module | |
| | CYM1841AP6-35C | PM01 | 72-Pin Plastic Angled SIMM Module (gold contacts) | |
| | CYM1841AP7-35C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841AP8-35C | PM04 | 72-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APN-35C | PN02 | 64-Pin Plastic Angled SIMM Module | |
| | CYM1841APR-35C | PZ01 | 64-Pin Plastic ZIP Module | |
| | CYM1841APZ-35C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BPZ-35C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BP7-35C | PM04 | 72-Pin Plastic SIMM Module | |
| 45 | CYM1841APM-45C | PM02 | 64-Pin Plastic SIMM Module | Commercial |
| | CYM1841APY-45C | PM01 | 64-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APT-45C | PM01 | 64-Pin Plastic SIMM Module | |
| | CYM1841AP5-45C | PN04 | 72-Pin Plastic Angled SIMM Module | |
| | CYM1841AP6-45C | PM01 | 72-Pin Plastic Angled SIMM Module (gold contacts) | |
| | CYM1841AP7-45C | PM04 | 72-Pin Plastic SIMM Module | |
| | CYM1841AP8-45C | PM04 | 72-Pin Plastic SIMM Module (gold contacts) | |
| | CYM1841APN-45C | PN02 | 64-Pin Plastic Angled SIMM Module | |
| | CYM1841APR-45C | PZ01 | 64-Pin Plastic ZIP Module | |
| | CYM1841APZ-45C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BPZ-45C | PZ03 | 64-Pin Plastic ZIP Module | |
| | CYM1841BP7-45C | PM04 | 72-Pin Plastic SIMM Module | |

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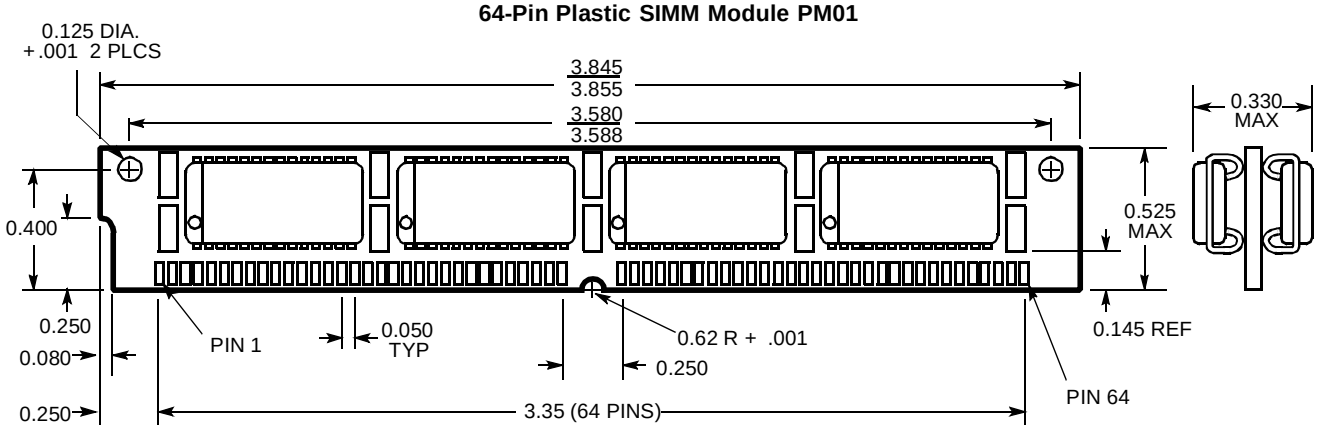
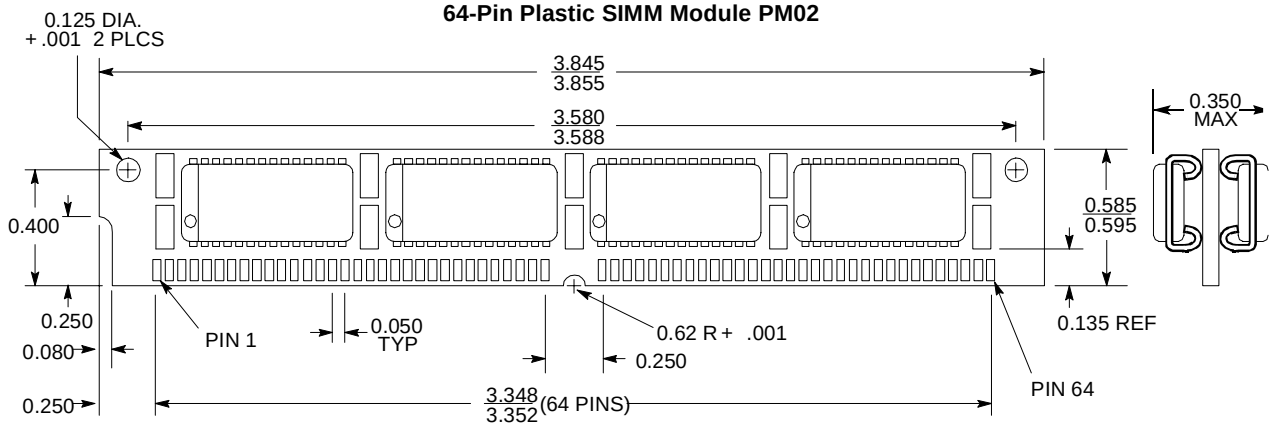
## Package Diagrams

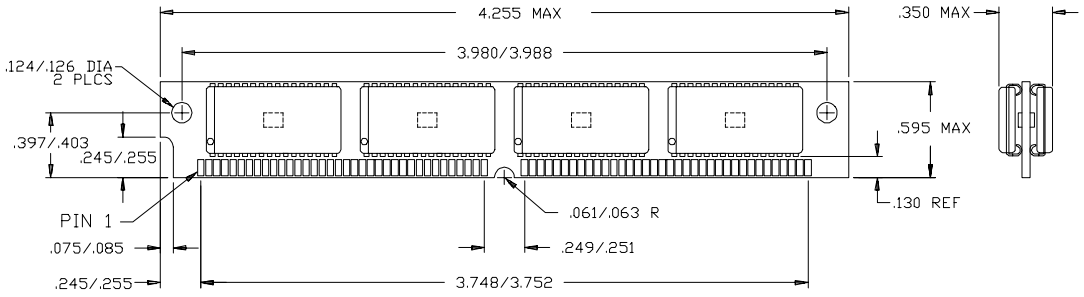
**64-Pin Plastic SIMM Module PM01**




**64-Pin Plastic SIMM Module PM02**

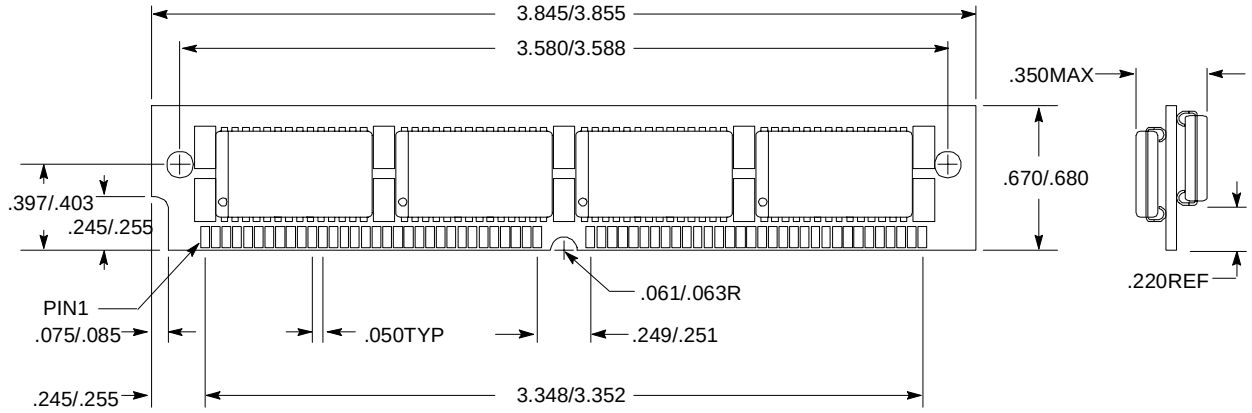



**72-Pin Plastic SIMM Module PM04**

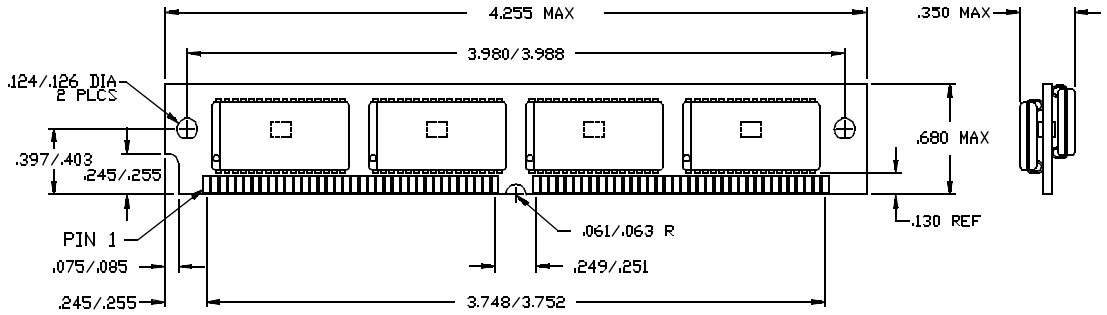


## Package Diagrams (continued)

**64-Pin Plastic Angled SIMM Module PN02**

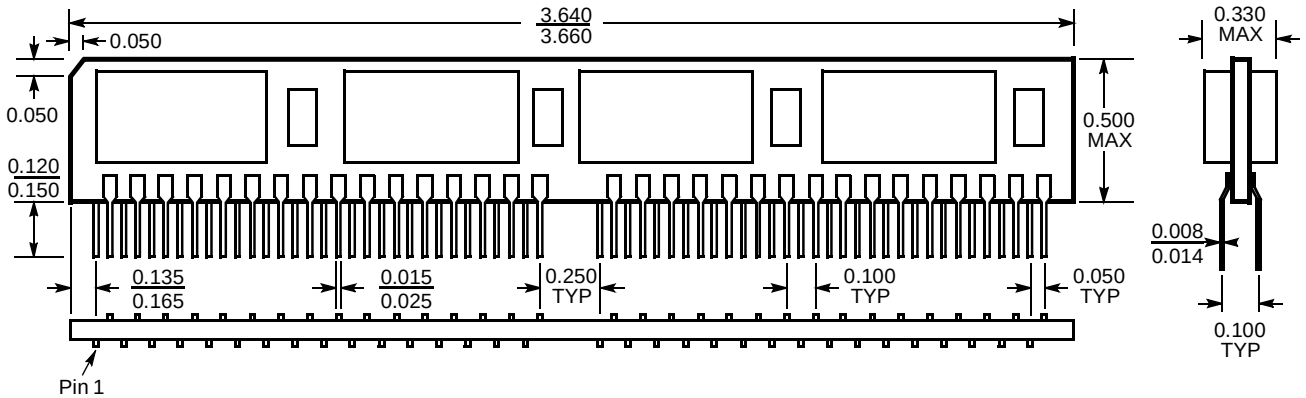



**72-Pin Plastic Angled SIMM Module PN04**




**64-Pin Plastic ZIP Module PZ01**

**Bottom View**



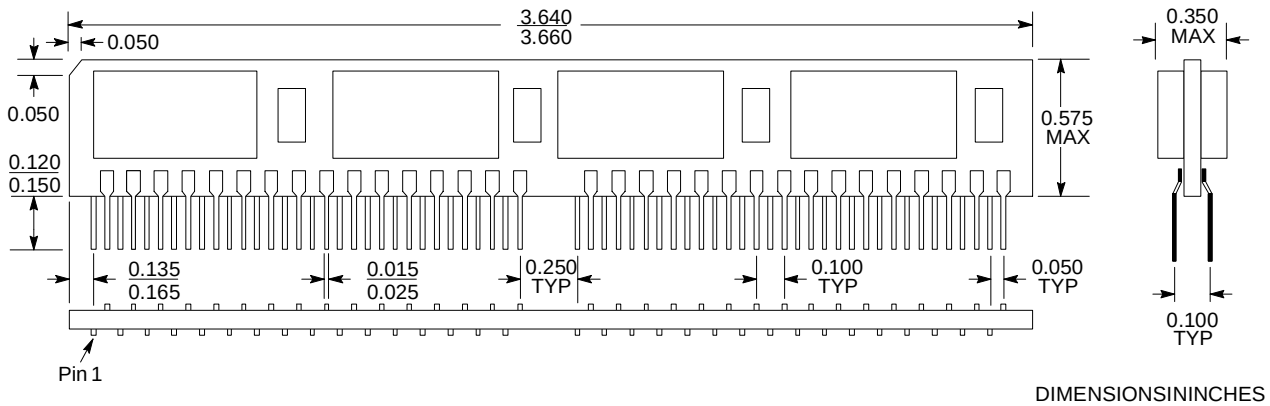

DIMENSIONS IN INCHES

MIN.
MAX.

## Package Diagrams (continued)

**64-Pin Plastic ZIP Module PZ03**

**Bottom View**




DIMENSIONSININCHES

MIN.
MAX.