

512K x 8 Static RAM

Features

- · High speed
 - $-t_{AA} = 15 \text{ ns}$
- · Low active power
 - 1210 mW (max.)
- Low CMOS standby power (Commercial L version) - 2.75 mW (max.)
- 2.0V Data Retention (400 μW at 2.0V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features

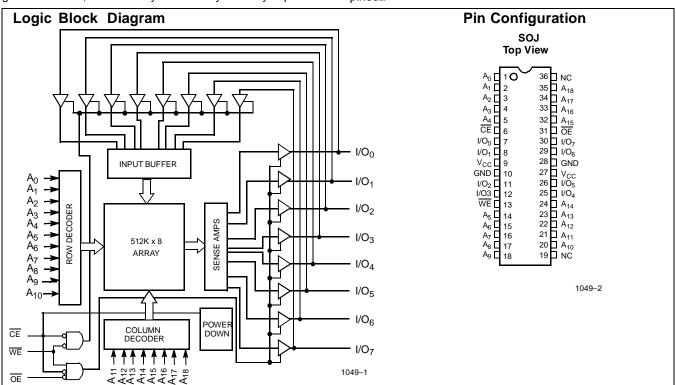
Functional Description

The CY7C1049 is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (CE), an active LOW output enable (OE), and three-state drivers. Writing to the device is accomplished by taking chip enable (CE) and write enable (WE) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking chip enable (CE) and output enable (OE) LOW while forcing write enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1049 is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

			7C1049-12	7C1049-15	7C1049-17	7C1049-20	7C1049-25
Maximum Access Time (ns)			12	15	17	20	25
Maximum Operating Current (mA)			240	220	195	185	180
Maximum CMOS Standby	Com'l		8	8	8	8	8
Current (mA)	Com'l	L	0.5	0.5	0.5	0.5	0.5
	Ind'I		9	9	9	9	9
	Military					10	10

Shaded areas contain advance information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.) Storage Temperature-65°C to +150°C Ambient Temperature with Power Applied –55°C to +125°C Supply Voltage on $\rm V_{CC}$ to Relative $\rm GND^{[1]}$ –0.5V to +7.0V DC Voltage Applied to Outputs in High Z State $^{[1]}$-0.5V to V CC + 0.5V DC Input Voltage^[1].....-0.5V to V_{CC} + 0.5V Current into Outputs (LOW)20 mA

Static Discharge Voltage	.>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature ^[2]	v _{cc}
Commercial	0°C to +70°C	4.5V-5.5V
Industrial	–40°C to +85°C	
Military	−55°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C10	049-12	7C1049-15		7C1049-17		
				Min.	Max.	Min.	Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	$V_{CC} = Min., I_{OH} = -4$.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	$V_{CC} = Min., I_{OL} = 8.0$) mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage[1]			-0.3	0.8	-0.3	0.8	-0.3	0.3	V
I _{IX}	Input Load Current	$GND \le V_1 \le V_{CC}$		-1	+1	-1	+1	-1	+1	μΑ
I _{OZ}	Output Leakage Current	$\begin{array}{l} \text{GND} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}, \\ \text{Output Disabled} \end{array}$		-1	+1	-1	+1	-1	+1	μА
I _{CC}	V _{CC} Operating Supply Current	$V_{CC} = Max.$ $f = f_{MAX} = 1/t_{RC}$			240		220		195	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	$\begin{aligned} &\text{Max. V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{IH}} \\ &\text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or} \\ &\text{V}_{\text{IN}} \leq \text{V}_{\text{IL}}, \text{ f} = \text{f}_{\text{MAX}} \end{aligned}$			40		40		40	mA
I _{SB2}	Automatic CE	Max. V _{CC} ,	Com'l		8		8		8	mA
F	Power-Down Current —CMOS Inputs	$\overline{CE} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$,	Com'l L		0.5		0.5		0.5	mA
		or $V_{IN} \le 0.3V$, f=0	Ind'I		9		9		9	mA
			Military		10		10		10	mA

Shaded areas contain advance information.

^{1.} $V_{\rm IL}$ (min.) = -2.0V for pulse durations of less than 20 ns. 2. $T_{\rm A}$ is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range (continued)

		Test Conditions		7C1	049-20	7C1		
Parameter	Description			Min.	Max.	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	$V_{CC} = Min., I_{OH} = -4.0$	0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	$V_{CC} = Min., I_{OL} = 8.0$	mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.3	2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]			-0.3	0.8	-0.3	0.8	V
I _{IX}	Input Load Current	$GND \leq V_1 \leq V_{CC}$		-1	+1	-1	+1	μΑ
I _{OZ}	Output Leakage Current	$\begin{array}{l} \text{GND} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}, \\ \text{Output Disabled} \end{array}$		-1	+1	-1	+1	μА
I _{CC}	V _{CC} Operating Supply Current	$V_{CC} = Max.$ $f = f_{MAX} = 1/t_{RC}$			185		180	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC} , $\overline{CE} \ge V_{IH}$ $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$			40		40	mA
I _{SB2}	Automatic CE	Max. V _{CC} ,	Com'l		8		8	mA
	Power-Down Current —CMOS Inputs	$CE \ge V_{CC} - 0.3V,$ $V_{IN} \ge V_{CC} - 0.3V,$	Com'l L		0.5		0.5	mA
	- CMOO IIIputo	or $V_{IN} \le 0.3V$, f=0	Ind'I		9		9	mA
			Military		10		10	mA

Capacitance^[3]

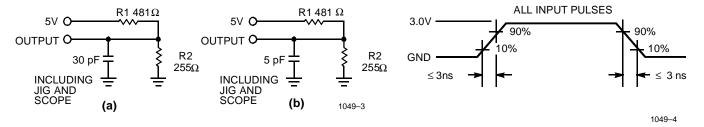
Parameter Description		Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C$, $f = 1$ MHz,	8	pF
C _{OUT}	I/O Capacitance	$V_{CC} = 5.0V$	8	pF

Note:
3. Tested initially and after any design or process changes that may affect these parameters.





AC Test Loads and Waveforms



THÉVENIN EQUIVALENT Equivalent to: 167Ω **__**O 1.73V

Switching Characteristics^[4] Over the Operating Range

	7C10	7C1049-12		7C1049-15		7C1049-17	
Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
LE	<u>'</u>				•	•	
Read Cycle Time	12		15		17		ns
Address to Data Valid		12		15		17	ns
Data Hold from Address Change	3		3		3		ns
CE LOW to Data Valid		12		15		17	ns
OE LOW to Data Valid		6		7		8	ns
OE LOW to Low Z ^[6]	0		0		0		ns
OE HIGH to High Z ^[5, 6]		6		7		7	ns
CE LOW to Low Z ^[6]	3		3		3		ns
CE HIGH to High Z ^[5, 6]		6		7		7	ns
CE LOW to Power-Up	0		0		0		ns
CE HIGH to Power-Down		12		15		17	ns
CLE ^[7,8]							•
Write Cycle Time	12		15		17		ns
CE LOW to Write End	10		12		12		ns
Address Set-Up to Write End	10		12		12		ns
Address Hold from Write End	0		0		0		ns
Address Set-Up to Write Start	0		0		0		ns
WE Pulse Width	10		12		12		ns
Data Set-Up to Write End	7		8		8		ns
Data Hold from Write End	0		0		0		ns
WE HIGH to Low Z ^[6]	3		3		3		ns
WE LOW to High Z ^[5, 6]		6		7		8	ns
	Read Cycle Time Address to Data Valid Data Hold from Address Change CE LOW to Data Valid OE LOW to Data Valid OE LOW to Low Z ^[6] OE HIGH to High Z ^[5, 6] CE LOW to Low Z ^[6] CE HIGH to High Z ^[5, 6] CE LOW to Power-Up CE HIGH to Power-Down CE LOW to Write End Address Set-Up to Write End Address Set-Up to Write Start WE Pulse Width Data Hold from Write End Data Hold from Write End Data Hold from Write End Data Hold from Write End	Description Min. LE Read Cycle Time 12 Address to Data Valid 12 Data Hold from Address Change 3 CE LOW to Data Valid 0 OE LOW to Low Z ^[6] 0 OE HIGH to High Z ^[5, 6] 3 CE LOW to Low Z ^[6] 3 CE LOW to Power-Up 0 CE HIGH to Power-Down 0 CE LOW to Vower-Up 0 CE LOW to Write End 10 Address Set-Up to Write End 10 Address Set-Up to Write End 0 Address Set-Up to Write Start 0 WE Pulse Width 10 Data Set-Up to Write End 7 Data Hold from Write End 0 WE HIGH to Low Z ^[6] 3	Description Min. Max. LE Read Cycle Time 12 Address to Data Valid 12 Data Hold from Address Change 3 CE LOW to Data Valid 12 OE LOW to Data Valid 6 OE LOW to Low Z ^[6] 0 OE HIGH to High Z ^[5, 6] 6 CE LOW to Low Z ^[6] 3 CE HIGH to High Z ^[5, 6] 6 CE LOW to Power-Up 0 CE HIGH to Power-Down 12 CE LOW to Worte End 10 Address Set-Up to Write End 10 Address Set-Up to Write End 0 Address Set-Up to Write Start 0 WE Pulse Width 10 Data Set-Up to Write End 7 Data Hold from Write End 0 WE HIGH to Low Z ^[6] 3	Description Min. Max. Min. LE Read Cycle Time 12 15 Address to Data Valid 12 15 Data Hold from Address Change 3 3 CE LOW to Data Valid 12 12 OE LOW to Data Valid 6 0 OE LOW to Low Z ^[6] 0 0 OE HIGH to High Z ^[5, 6] 6 0 CE LOW to Low Z ^[6] 3 3 CE HIGH to High Z ^[5, 6] 6 0 CE LOW to Power-Up 0 0 CE HIGH to Power-Down 12 12 CLE ^[7,8] 12 15 CE LOW to Write End 10 12 Address Set-Up to Write End 0 0 Address Set-Up to Write Start 0 0 WE Pulse Width 10 12 Data Set-Up to Write End 7 8 Data Hold from Write End 0 0 WE HIGH to Low Z ^[6] 3 3	Description Min. Max. Min. Max. LE Read Cycle Time 12 15 15 Address to Data Valid 12 15 15 Data Hold from Address Change 3 3 3 CE LOW to Data Valid 12 15 15 OE LOW to Data Valid 6 7 7 0 0 0 0 OE LOW to Low Z ^[6] 0 0	Min. Max. Min. Max. Min. Max. Min.	Description Min. Max. Min. Max. Min. Max. LE Read Cycle Time 12 15 17 Address to Data Valid 12 15 17 Data Hold from Address Change 3 3 3 CE LOW to Data Valid 6 7 8 OE LOW to Data Valid 6 7 8 OE LOW to Low Z ^[6] 0 0 0 OE HIGH to High Z ^[5, 6] 6 7 7 CE LOW to Low Z ^[6] 3 3 3 CE HIGH to High Z ^[5, 6] 6 7 7 CE LOW to Power-Up 0 0 0 CE LOW to Power-Up 0 0 0 Write Cycle Time 12 15 17 LE[7,8] 15 17 Write Cycle Time 12 15 17 CE LOW to Write End 10 12 12 Address Set-Up to Write End 0 0 0 <t< td=""></t<>

Shaded areas contain advance information.

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- thzoe, thzce, and thzwe are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- t_{HZOE}, find t_{HZWE} are specified with a load capacitance of 5 pr as in part (ii) of Ac less Loads. Italismon's measured 1500 min form steady-state variage. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZOE}, t_{HZOE} is less than t_{LZOE}, then the set of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}. 7.



$\textbf{Switching Characteristics}^{[4]} \ \, \text{Over the Operating Range (continued)}$

		7C10	49-20	7C10		
Parameter	Description	Min.	Max.	Min.	Max.	Unit
READ CYCL	E		•	•		
t _{RC}	Read Cycle Time	20		25		ns
t _{AA}	Address to Data Valid		20		25	ns
t _{OHA}	Data Hold from Address Change	3		5		ns
t _{ACE}	CE LOW to Data Valid		20		25	ns
t _{DOE}	OE LOW to Data Valid		8		10	ns
t _{LZOE}	OE LOW to Low Z ^[6]	0		0		ns
t _{HZOE}	OE HIGH to High Z ^[5, 6]		8		10	ns
t _{LZCE}	CE LOW to Low Z ^[6]	3		5		ns
t _{HZCE}	CE HIGH to High Z ^[5, 6]		8		10	ns
t _{PU}	CE LOW to Power-Up	0		0		ns
t _{PD}	CE HIGH to Power-Down		20		25	ns
WRITE CYCL	. E ^[7]	·				
t _{WC}	Write Cycle Time	20		25		ns
t _{SCE}	CE LOW to Write End	13		15		ns
t _{AW}	Address Set-Up to Write End	13		15		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	13		15		ns
t _{SD}	Data Set-Up to Write End	9		10		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[6]	3		5		ns
t _{HZWE}	WE LOW to High Z ^[5, 6]		8		10	ns

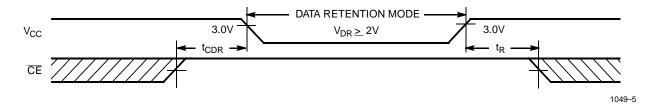
Data Retention Characteristics Over the Operating Range

Parameter	r Description			Conditions ^[10]	Min.	Max	Unit
V _{DR}	V _{CC} for Data Retention				2.0		V
I _{CCDR}	Data Retention Current	Com'l	L	$\frac{V_{CC} = V_{DR} = 3.0V}{CE \ge V_{CC} - 0.3V}$		200	μΑ
		Ind'I		$CE \ge V_{CC} - 0.3V$ $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$		1	mA
		Military				2	mA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time	•			0		ns
t _R ^[9]	Operation Recovery Time				t _{RC}		ns

^{9.} $t_r \le 3$ ns for the -12 and -15 speeds. $t_r \le 5$ ns for the -20 ns and slower speeds. 10. No input may exceed V_{CC} + 0.5V.

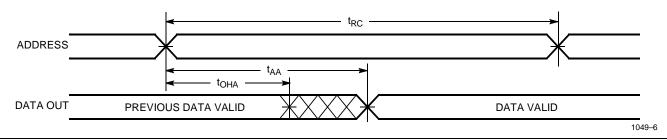


Data Retention Waveform

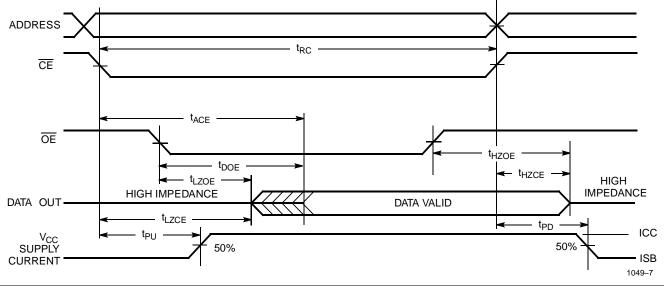


Switching Waveforms

Read Cycle No. 1^[11, 12]



Read Cycle No. 2 (OE Controlled)[12, 13]

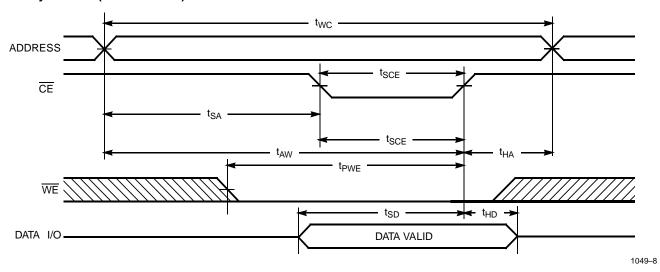


- Device is continuously selected. OE, CE = V_{IL}.
 WE is HIGH for read cycle.
 Address valid prior to or coincident with CE transition LOW.

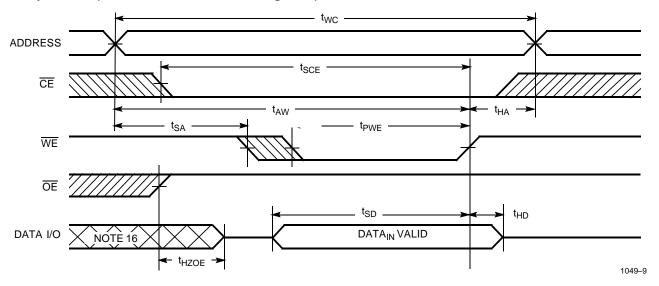


Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)[14, 15]



Write Cycle No. 2 (WE Controlled, OE HIGH During Write)[14, 15]

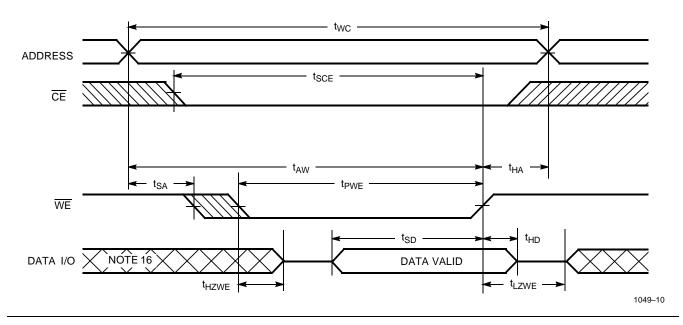


- 14. Data I/O is high impedance if OE = V_{IH}.
 15. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
 16. During this period the I/Os are in the output state and input signals should not be applied.



Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW)[15]



Ordering Information

Speed (ns)			Package Type	Operating Range
15 CY7C1049-15VC		V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-15VC	V36	36-Lead (400-Mil) Molded SOJ	
17	CY7C1049-17VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049L-17VC	V36	36-Lead (400-Mil) Molded SOJ	
20	CY7C1049-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049L-20VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-20VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049L-20VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-20VM	V36	36-Lead (400-Mil) Molded SOJ	Military
	CY7C1049L-20VM	V36	36-Lead (400-Mil) Molded SOJ	
25	CY7C1049-25VC	V36	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049L-25VC	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-25VI	V36	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049L-25VI	V36	36-Lead (400-Mil) Molded SOJ	
	CY7C1049-25VM	V36	36-Lead (400-Mil) Molded SOJ	Military
	CY7C1049L-25VM	V36	36-Lead (400-Mil) Molded SOJ	

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Package Diagram

36-Lead (400-Mil) Molded SOJ V36

