



CY7C470
CY7C472
CY7C474

8K x 9 FIFO, 16K x 9 FIFO 32K x 9 FIFO with Programmable Flags

Features

- 8K x 9, 16K x 9, and 32K x 9 FIFO buffer memory
- Asynchronous read/write
- High-speed 33.3-MHz read/write independent of depth/width
- Low operating power
 — I_{CC} (max.) = 70 mA
- Programmable Almost Full/Empty flag
- Empty, Almost Empty, Half Full, Almost Full, and Full status flags
- Programmable retransmit
- Expandable in width
- 5V ± 10% supply
- TTL compatible
- Three-state outputs
- Proprietary 0.8-micron CMOS technology

Functional Description

The CYC47X FIFO series consists of high-speed, low-power, first-in first-out (FIFO) memories with programmable flags and retransmit mark. The CY7C470, CY7C472, and CY7C474 are 8K, 16K, and 32K words by 9 bits wide, respectively. They are

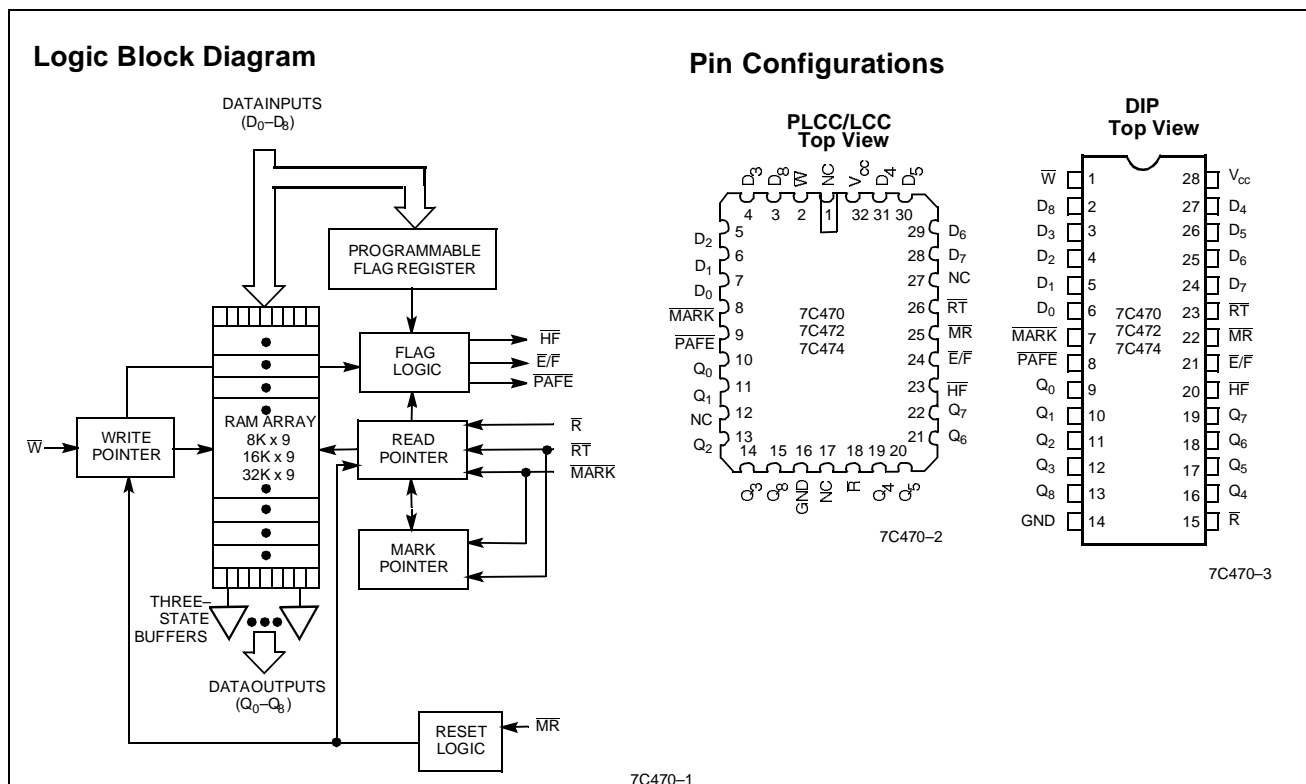
offered in 600-mil DIP, PLCC, and LCC packages. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Three status pins—Empty/Full (E/F), Programmable Almost Full/Empty (PAFE), and Half Full (HF)—are provided to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than Half Full, Greater than Half Full, Almost Full, and Full.

The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write (\bar{W}) signal goes LOW. Read occurs when read (\bar{R}) goes LOW. The nine data outputs go into a high-impedance state when \bar{R} is HIGH.

The user can store the value of the read pointer for retransmit by using the MARK pin. A LOW on the retransmit (RT) input causes the FIFO to resend data by resetting the read pointer to the value stored in the mark pointer.

In the standalone and width expansion configurations, a LOW on the retransmit (\bar{RT}) input causes the FIFO to resend the data. With the mark feature, retransmit can start from any word in the FIFO.

The CYC47X series is fabricated using a proprietary 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2001V and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.





Selection Guide

| | | 7C470-15 7C472-15 7C474-15 | 7C470-20 7C472-20 7C474-20 | 7C470-25 7C472-25 7C474-25 | 7C470-40 7C472-40 7C474-40 |
|--------------------------------|---------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| Frequency (MHz) | | 33.3 | 33.3 | 28.5 | 20 |
| Maximum Access Time (ns) | | 15 | 20 | 25 | 40 |
| Maximum Operating Current (mA) | Commercial | 105 | | | |
| | Military/Industrial | | | | |

Maximum Ratings

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs
 in High Z State -0.5V to +7.0V
 DC Input Voltage..... -3.0V to +7.0V
 Power Dissipation 1.0W
 Output Current, into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current..... >200 mA

Operating Range

| Range | Ambient Temperature | V _{CC} |
|-------------------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |
| Military ^[1] | -55°C to +125°C | 5V ± 10% |

Electrical Characteristics Over the Operating Range^[2]

| Parameter | Description | Test Conditions | 7C470-15 7C472-15 7C474-15 | | 7C470-20 7C472-20 7C474-20 | | 7C470-25 7C472-25 7C474-25 | | Unit |
|--------------------------------|------------------------------|--|----------------------------------|------|----------------------------------|------|----------------------------------|------|------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -2.0 mA | 2.4 | | 2.4 | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | | 0.4 | | 0.4 | V |
| V _{IH} | | Com'l | 2.2 | | | | 2.2 | | V |
| | | | Mil/Ind | | | 2.2 | | 2.2 | |
| V _{IL} | Input LOW Voltage | | | 0.8 | | 0.8 | | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -10 | +10 | -10 | +10 | -10 | +10 | µA |
| I _{OZ} | Output Leakage Current | $\bar{R} \geq V_{IH}$, GND ≤ V _O ≤ V _{CC} | -10 | +10 | -10 | +10 | -10 | +10 | µA |
| I _{CC} | Operating Current | V _{CC} = Max., I _{OUT} = 0 mA | Com'l | 105 | | | | 90 | mA |
| | | | Mil/Ind | | | | 110 | 95 | |
| I _{SB1} | Standby Current | All Inputs = V _{IH} Min. | Com'l | 25 | | | | 25 | mA |
| | | | Mil/Ind | | | | 30 | 30 | |
| I _{SB2} | Power-Down Current | All Inputs = V _{CC} - 0.2V | Com'l | 20 | | | | 20 | mA |
| | | | Mil/Ind | | | | 25 | 25 | |
| I _{OS} ^[3] | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = GND | | -90 | | -90 | | -90 | mA |

Notes:

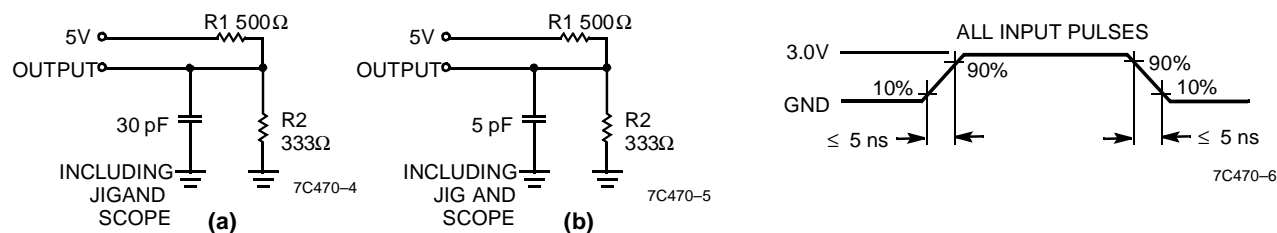
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.

Electrical Characteristics Over the Operating Range^[2] (continued)

| Parameter | Description | Test Conditions | 7C470-40 7C472-40 7C474-40 | | Unit |
|--------------------------------|------------------------------|--|----------------------------------|------|------|
| | | | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -2.0 mA | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | Com'l | 2.2 | V |
| | | | Mil/Ind | 2.2 | |
| V _{IL} | Input LOW Voltage | | | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -10 | +10 | μA |
| I _{OZ} | Output Leakage Current | $\bar{R} \geq V_{IH}$, GND ≤ V _O ≤ V _{CC} | -10 | +10 | μA |
| I _{CC} | Operating Current | V _{CC} = Max., I _{OUT} = 0 mA | Com'l | 70 | mA |
| | | | Mil/Ind | 75 | |
| I _{SB1} | Standby Current | All Inputs = V _{IH} Min. | Com'l | 25 | mA |
| | | | Mil/Ind | 30 | |
| I _{SB2} | Power-Down Current | All Inputs = V _{CC} - 0.2V | Com'l | 20 | mA |
| | | | Mil/Ind | 25 | |
| I _{OS} ^[3] | Output Short Circuit Current | V _{CC} = Max., V _{OUT} = GND | | -90 | mA |

Capacitance^[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|------------------|--------------------|---|------|------|
| C _{IN} | Input Capacitance | T _A = 25°C, f = 1 MHz, V _{CC} = 4.5V | 10 | pF |
| C _{OUT} | Output Capacitance | | 12 | pF |

AC Test Loads and Waveforms


Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT — 200Ω — 2V

Note:

4. Tested initially and after any design or process changes that may affect these parameters.



Switching Characteristics Over the Operating Range^[5, 6]

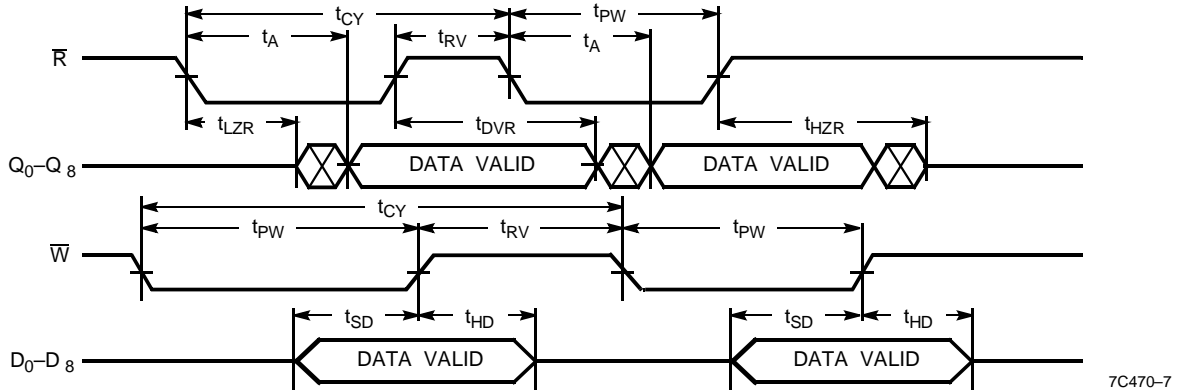
| Parameter | Description | 7C470-15 7C472-15 7C474-15 | | 7C470-20 7C472-20 7C474-20 | | 7C470-25 7C472-25 7C474-25 | | 7C470-40 7C472-40 7C474-40 | | Unit |
|--------------------------------|---|----------------------------------|------|----------------------------------|------|----------------------------------|------|----------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{CY} | Cycle Time | 30 | | 30 | | 35 | | 50 | | ns |
| t _A | Access Time | | 15 | | 20 | | 25 | | 40 | ns |
| t _{RV} | Recovery Time | 15 | | 10 | | 10 | | 10 | | ns |
| t _{PW} | Pulse Width | 15 | | 20 | | 25 | | 40 | | ns |
| t _{LZR} | Read LOW to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| t _{DV} ^[7] | Valid Data from Read HIGH | 3 | | 3 | | 3 | | 3 | | ns |
| t _{HZ} ^[7] | Read HIGH to High Z | | 15 | | 15 | | 18 | | 25 | ns |
| t _{HWZ} | Write HIGH to Low Z | 5 | | 5 | | 5 | | 5 | | ns |
| t _{SD} | Data Set-Up Time | 11 | | 12 | | 15 | | 20 | | ns |
| t _{HD} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| t _{EFD} | \bar{E}/\bar{F} Delay | | 15 | | 20 | | 25 | | 40 | ns |
| t _{EFL} | $\bar{M}\bar{R}$ to \bar{E}/\bar{F} LOW | | 25 | | 30 | | 35 | | 50 | ns |
| t _{HFD} | $\bar{H}\bar{F}$ Delay | | 25 | | 30 | | 35 | | 50 | ns |
| t _{AFED} | $\bar{P}\bar{A}\bar{F}\bar{E}$ Delay | | 25 | | 30 | | 35 | | 50 | ns |
| t _{RAE} | Effective Read from Write HIGH | 15 | | 20 | | 25 | | 40 | | ns |
| t _{WAF} | Effective Write from Read HIGH | 15 | | 20 | | 25 | | 40 | | ns |

Notes:

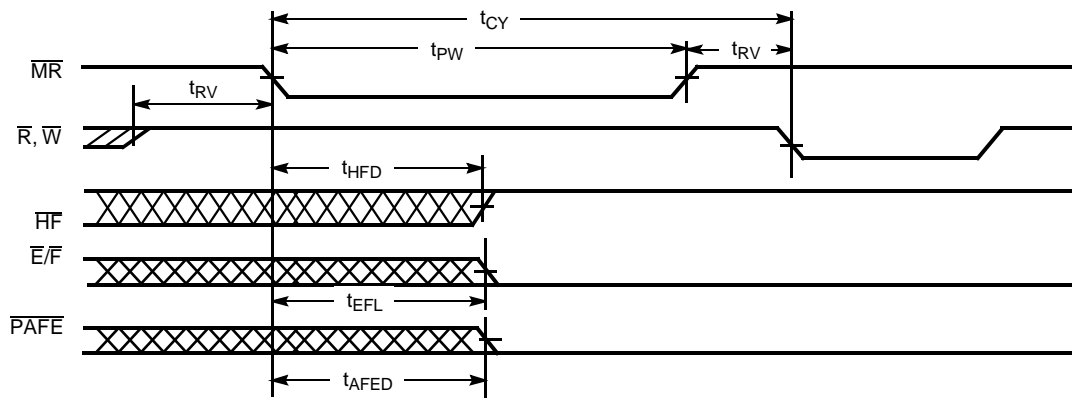
5. Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
6. See the last page of this specification for Group A subgroup testing information.
7. t_{HZR} and t_{DVR} use capacitance loading as in part (b) of AC Test Loads. t_{HZR} transition is measured at +500 mV from V_{OL} and -500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.

Switching Waveforms

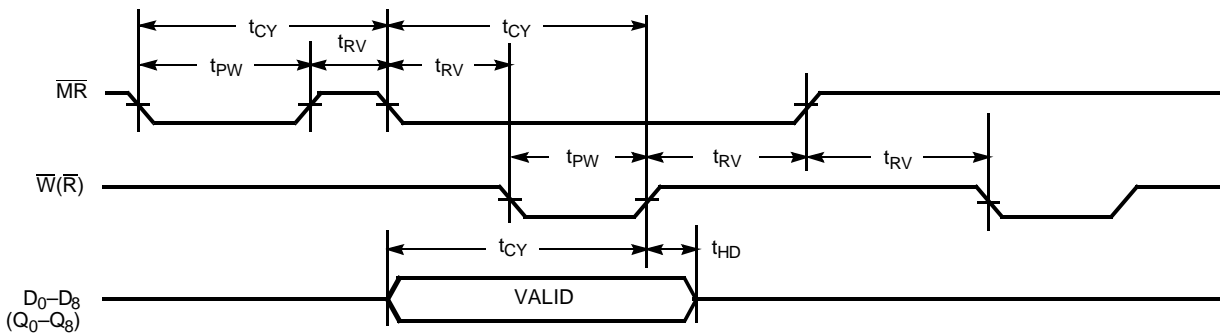
Asynchronous Read and Write



Master Reset (No Write to Programmable Flag Register)

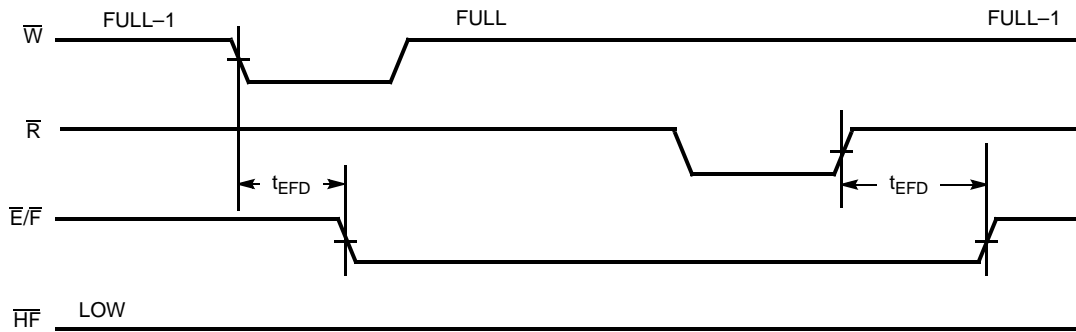


Master Reset (Write to Programmable Flag Register)^[8,9]

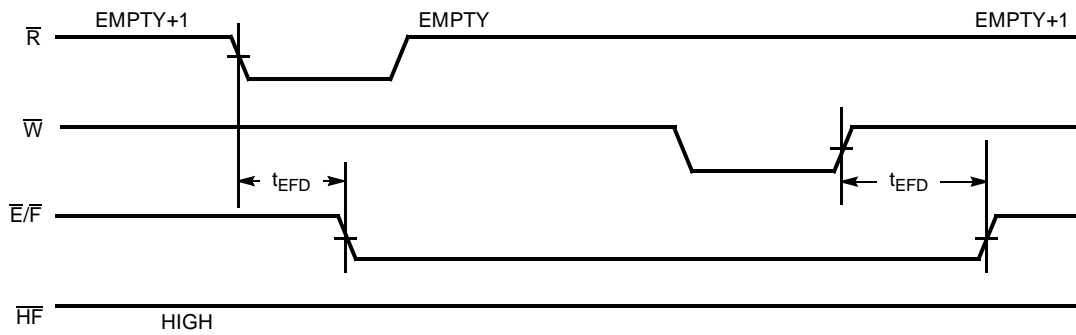


Notes:

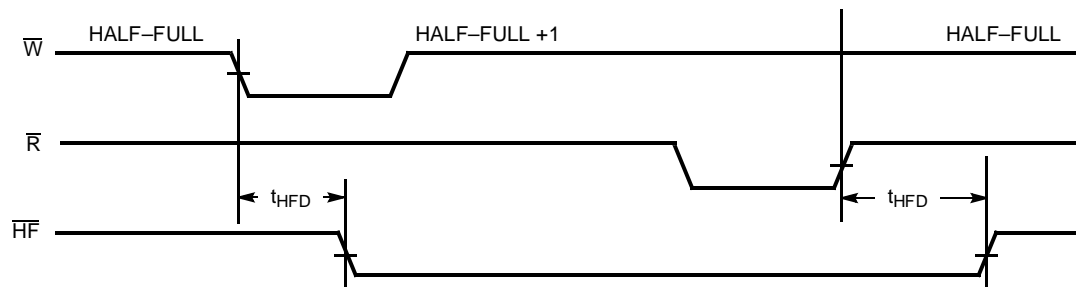
8. Waveform labels in parentheses pertain to writing the programmable flag register from the output port ($Q_0 - Q_8$).
9. Master Reset (\overline{MR}) must be pulsed LOW once prior to programming.

Switching Waveforms (Continued)
 \bar{E}/\bar{F} Flag (Last Write to First Read Full Flag)


7C470-10

 \bar{E}/\bar{F} Flag (Last Read to First Write Empty Flag)


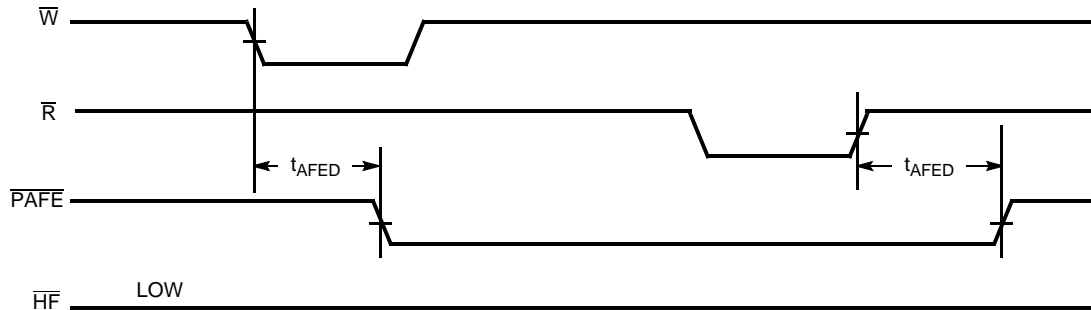
7C470-11

Half Full Flag


7C470-12

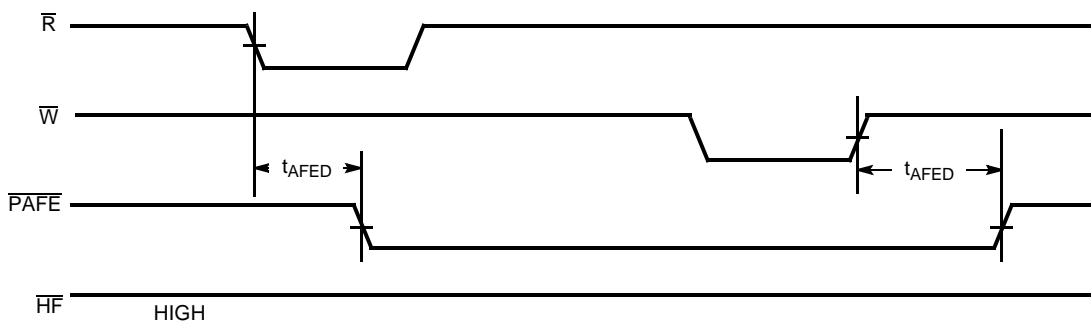
Switching Waveforms (Continued)

P $\overline{\text{AFE}}$ Flag (Almost Full)



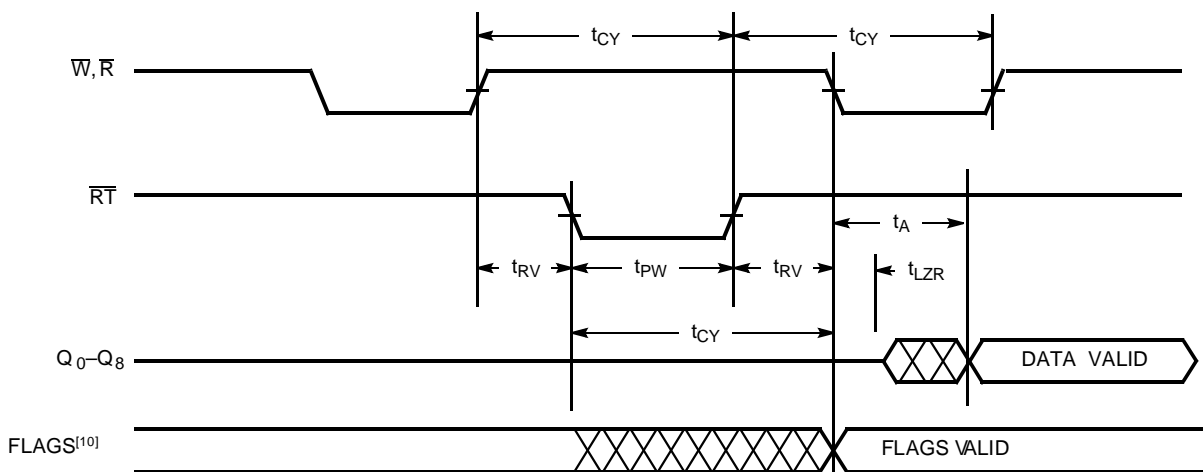
7C470-13

P $\overline{\text{AFE}}$ Flag (Almost Empty)



7C470-14

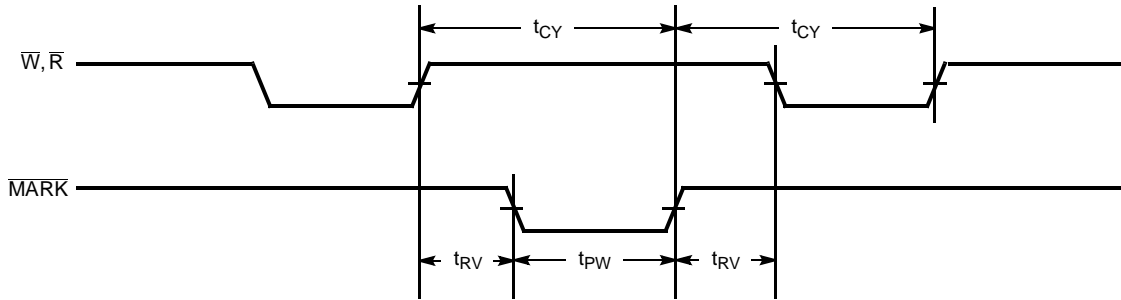
Retransmit^[10]



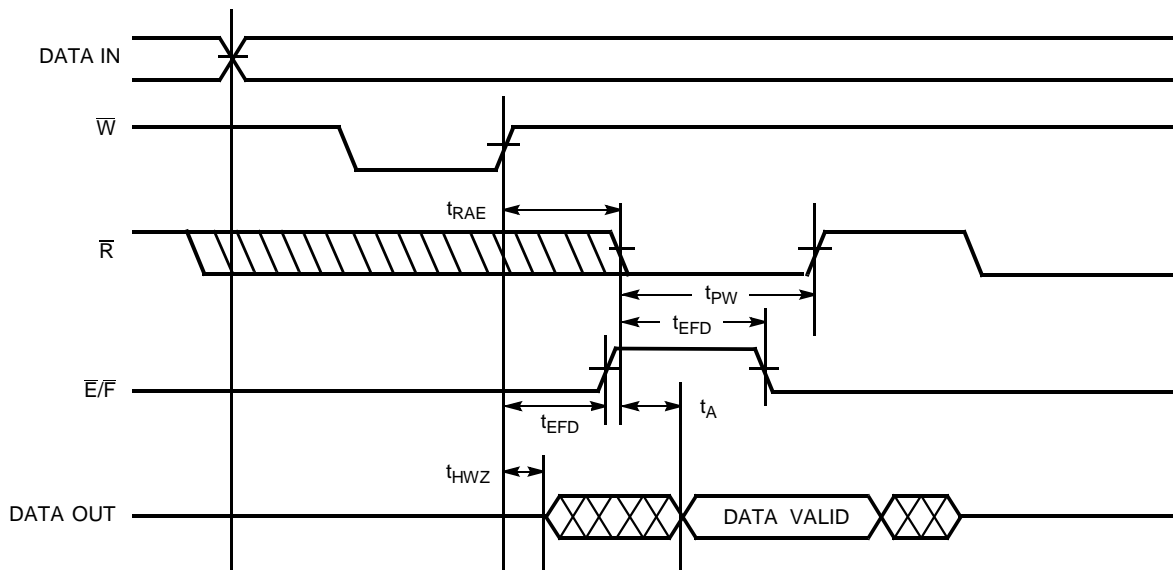
7C470-15

Note:

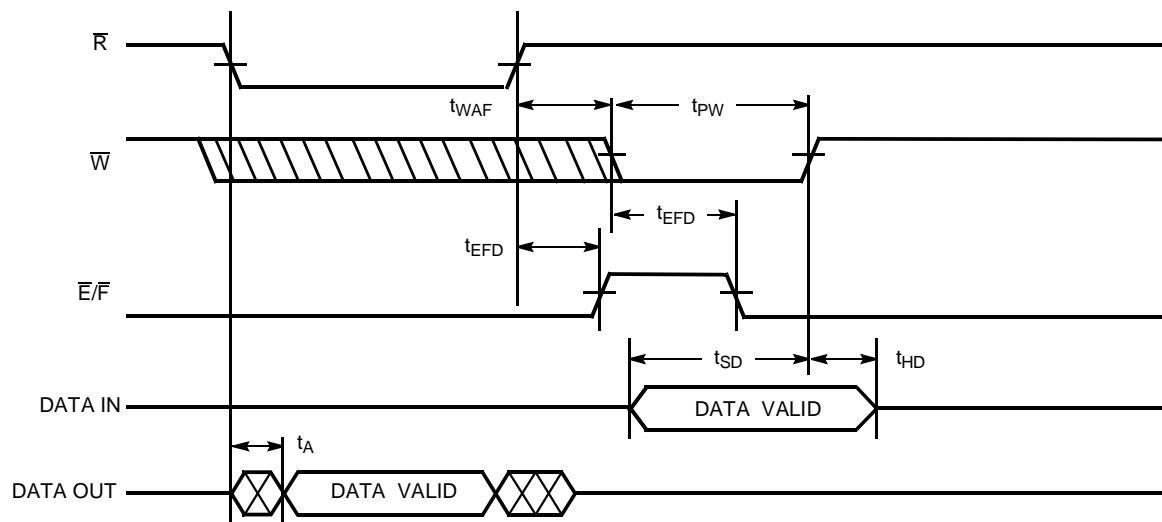
10. The flags may change state during retransmit, but they will be valid a t_{CY} later, except for the CY7C47X-20 (Military), whose flags will be valid after $t_{\text{CY}} + 10$ ns.

Switching Waveforms (Continued)
Mark


7C470-16

Empty Flag and Read Data Flow-Through Mode


7C470-17

Switching Waveforms (Continued)
Full Flag and Write Data Flow-Through Mode


7C470-18

Architecture

The CY7C470, CY7C472, and CY7C474 FIFOs consist of an array of 8,192, 16,384, and 32,768 words of 9 bits each, respectively. The control consists of a read pointer, a write pointer, a retransmit pointer, control signals (i.e., write, read, mark, retransmit, and master reset), and flags (i.e., Empty/Full, Half Full, and Programmable Almost Full/Empty).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Master Reset (\overline{MR}) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{E/F}$) and Almost Full/Empty flag (\overline{PAFE}) being LOW, and Half Full flag (\overline{HF}) being HIGH. The read pointer, write pointer, and retransmit pointer are reset to zero. For a valid reset, Read (\overline{R}) and Write (\overline{W}) must be HIGH t_{RPW}/t_{WPW} before the falling edge and t_{RMR} after the rising edge of \overline{MR} .

Writing Data to the FIFO

Data can be written to the FIFO when it is not FULL^[11]. A falling edge of \overline{W} initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of \overline{W} will be stored sequentially in the FIFO.

Reading Data from the FIFO

Data can be read from the FIFO when it is not empty^[12]. A falling edge of \overline{R} initiates a read cycle. Data outputs (Q_0-Q_8) are in a high-impedance condition when the FIFO is empty and between read operations (\overline{R} HIGH). The falling edge of \overline{R} during the last read cycle before the empty condition triggers a high-to-low transition of $\overline{E/F}$, prohibiting any further read operations until t_{RFF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and resent if necessary. Retransmission can start from anywhere in the FIFO and be repeated without limitation.

The retransmit methodology is as follows: mark the current value of the read pointer, after an error in subsequent read operations return to that location and resume reading. This effectively resends all of the data from the mark point. When \overline{MARK} is LOW, the current value of the read pointer is stored. This operation marks the beginning of the packet to be resent. When \overline{RT} is LOW, the read pointer is updated with the mark location. During each subsequent read cycle, data is read and the read pointer incremented.

Care must be taken when using the retransmit feature. Use the mark function such that the write pointer does not pass the mark pointer, because further write operations will overwrite data.

Programmable Almost Full/Empty Flag

The CY7C470/2/4 offer a variable offset for the Almost Empty and the Almost Full condition. The offset is loaded into the programmable flag register (PFR) during a master reset cycle. While \overline{MR} is LOW, the PFR can be loaded from Q_8-Q_0 by pulsing \overline{R} LOW or from D_8-D_0 by pulsing \overline{W} LOW. The offset options are listed in Table 2. See Table 1 for a description of the six FIFO states. If the PFR is not loaded during master reset (\overline{R} and \overline{W} HIGH) the default offset will be 256 words from Full and Empty.

Notes:

11. When the FIFO is less than half full, the flags make a LOW-to-HIGH transition on the rising edge of \overline{W} and make the HIGH-to-LOW transition on the falling edge of \overline{R} . If the FIFO is more than half full, the flags make the LOW-to-HIGH transition on the rising edge of \overline{R} and HIGH-to-LOW transition on the falling edge of \overline{W} .
12. Full and empty states can be decoded from the Half-Full (\overline{HF}) and Empty/Full ($\overline{E/F}$) flags.



Table 1. Flag Truth Table^[13]

| HF | \bar{E}/F | \overline{PAFE} | State | CY77C470 (8K x 9) Number of Words in FIFO | CY77C472 (16K x 9) Number of Words in FIFO | CY77C474 (32K x 9) Number of Words in FIFO |
|----|-------------|-------------------|------------------------|--|---|---|
| 1 | 0 | 0 | Empty | 0 | 0 | 0 |
| 1 | 1 | 0 | Almost Empty | $1 \Rightarrow (P - 1)$ | $1 \Rightarrow (P - 1)$ | $1 \Rightarrow (P - 1)$ |
| 1 | 1 | 1 | Less than Half Full | $P \Rightarrow 4096$ | $P \Rightarrow 8192$ | $P \Rightarrow 16384$ |
| 0 | 1 | 1 | Greater than Half Full | $4097 \Rightarrow (8192 - P)$ | $8193 \Rightarrow (16384 - P)$ | $16385 \Rightarrow (32768 - P)$ |
| 0 | 1 | 0 | Almost Full | $(8192 - P + 1) \Rightarrow 8191$ | $(16384 - P + 1) \Rightarrow 16383$ | $(32768 - P + 1) \Rightarrow 32767$ |
| 0 | 0 | 0 | Full | 8192 | 16384 | 32768 |

Table 2. Programmable Almost Full/Empty Options^[14]

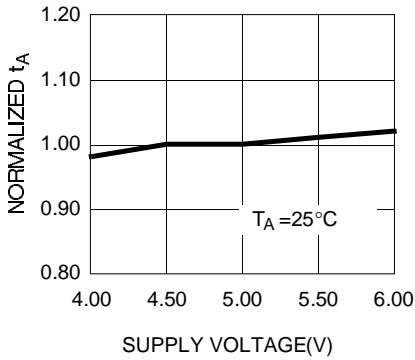
| D3 | D2 | D1 | D0 | PAFE Active when: | P |
|----|----|----|----|--|------|
| 0 | 0 | 0 | 0 | 256 or less locations from Empty/Full (default) | 256 |
| 0 | 0 | 0 | 1 | 16 or less locations from Empty/Full | 16 |
| 0 | 0 | 1 | 0 | 32 or less locations from Empty/Full | 32 |
| 0 | 0 | 1 | 1 | 64 or less locations from Empty/Full | 64 |
| 0 | 1 | 0 | 0 | 128 or less locations from Empty/Full | 128 |
| 0 | 1 | 0 | 1 | 256 or less locations from Empty/Full (default) | 256 |
| 0 | 1 | 1 | 0 | 512 or less locations from Empty/Full | 512 |
| 0 | 1 | 1 | 1 | 1024 or less locations from Empty/Full | 1024 |
| 1 | 0 | 0 | 0 | 2048 or less locations from Empty/Full | 2048 |
| 1 | 0 | 0 | 1 | 4098 or less locations from Empty/Full ^[15] | 4098 |
| 1 | 0 | 1 | 0 | 8192 or less locations from Empty/Full ^[16] | 8192 |

Notes:

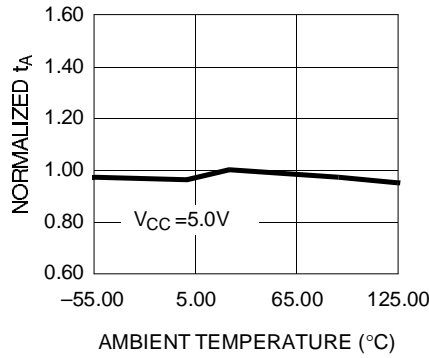
- 13. See Table 2 for P values.
- 14. Almost flags default to 256 locations from Empty/Full.
- 15. Only for CY7C472 and CY7C474.
- 16. Only for CY7C470.

Typical AC and DC Characteristics

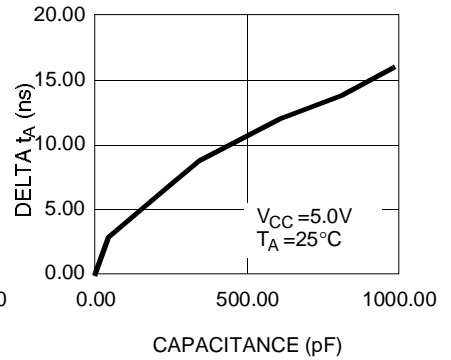
NORMALIZED t_A vs. SUPPLY VOLTAGE



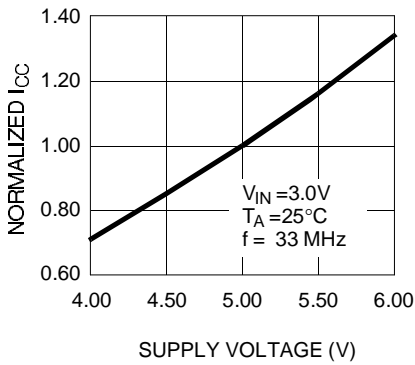
NORMALIZED t_A vs. AMBIENT TEMPERATURE



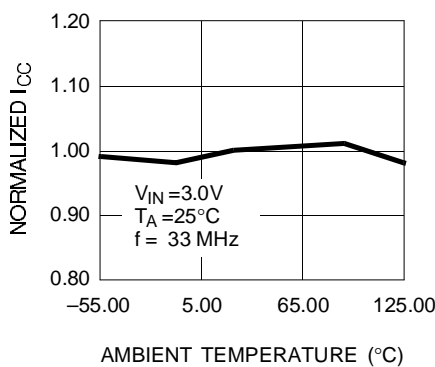
TYPICAL t_A CHANGE vs. OUTPUT LOADING



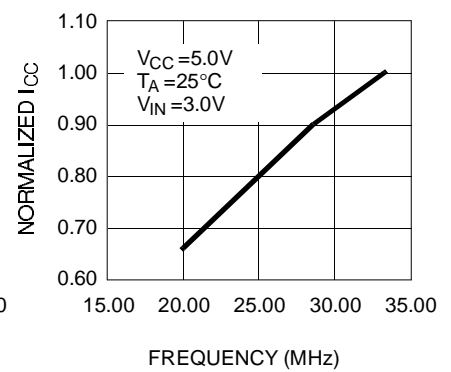
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



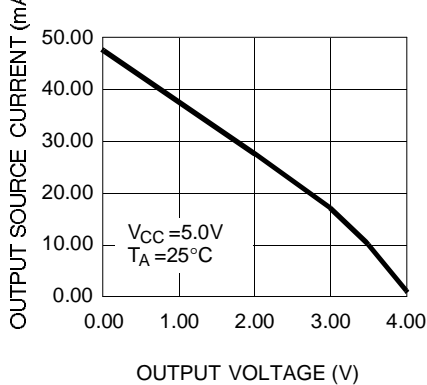
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



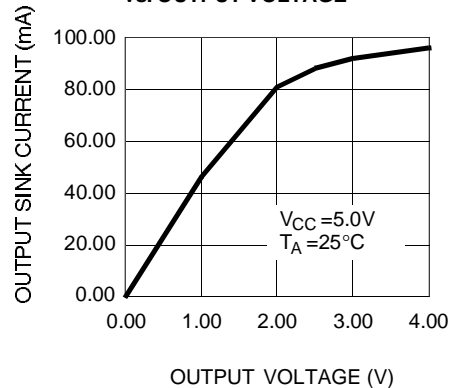
NORMALIZED SUPPLY CURRENT vs. FREQUENCY



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE





Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|--|-----------------|
| 15 | CY7C470-15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C470-15PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C470-15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 20 | CY7C470-20DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C470-20LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 25 | CY7C470-25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C470-25PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C470-25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C470-25DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C470-25LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 40 | CY7C470-40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C470-40PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C470-40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C470-40DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C470-40LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|--|-----------------|
| 15 | CY7C472-15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C472-15PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C472-15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 20 | CY7C472-20DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C472-20LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 25 | CY7C472-25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C472-25PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C472-25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C472-25DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C472-25LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 40 | CY7C472-40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C472-40PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C472-40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C472-40DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C472-40LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |



Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|---------------|--------------|--|-----------------|
| 15 | CY7C474-15JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C474-15PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C474-15JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| 20 | CY7C474-20DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C474-20LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | |
| 25 | CY7C474-25JC | J65 | 32-Lead Plastic Leaded Chip Carrier | Commercial |
| | CY7C474-25PC | P15 | 28-Lead (600-Mil) Molded DIP | Industrial |
| | CY7C474-25JI | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C474-25DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C474-25LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | Commercial |
| 40 | CY7C474-40JC | J65 | 32-Lead Plastic Leaded Chip Carrier | |
| | CY7C474-40PC | P15 | 28-Lead (600-Mil) Molded DIP | |
| | CY7C474-40JI | J65 | 32-Lead Plastic Leaded Chip Carrier | Industrial |
| | CY7C474-40DMB | D43 | 28-Lead (600-Mil) Sidebrazed CerDIP | Military |
| | CY7C474-40LMB | L55 | 32-Pin Rectangular Leadless Chip Carrier | Commercial |

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

| Parameter | Subgroups |
|---------------|-----------|
| V_{OH} | 1, 2, 3 |
| V_{OL} | 1, 2, 3 |
| V_{IH} | 1, 2, 3 |
| V_{IL} Max. | 1, 2, 3 |
| I_{IX} | 1, 2, 3 |
| I_{OS} | 1, 2, 3 |
| I_{CC} | 1, 2, 3 |

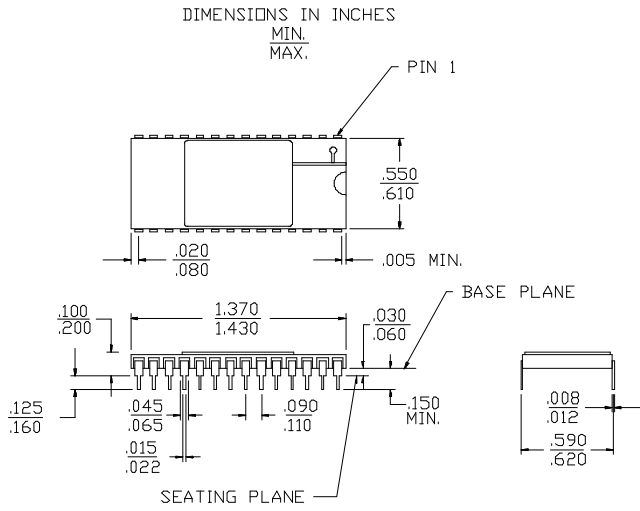
Switching Characteristics

| Parameter | Subgroups |
|------------|-----------|
| t_{CY} | 9, 10, 11 |
| t_A | 9, 10, 11 |
| t_{RV} | 9, 10, 11 |
| t_{PW} | 9, 10, 11 |
| t_{LZR} | 9, 10, 11 |
| t_{DVR} | 9, 10, 11 |
| t_{HZR} | 9, 10, 11 |
| t_{HWZ} | 9, 10, 11 |
| t_{SD} | 9, 10, 11 |
| t_{HD} | 9, 10, 11 |
| t_{EFD} | 9, 10, 11 |
| t_{HFD} | 9, 10, 11 |
| t_{AFED} | 9, 10, 11 |
| t_{RAE} | 9, 10, 11 |
| t_{WAF} | 9, 10, 11 |

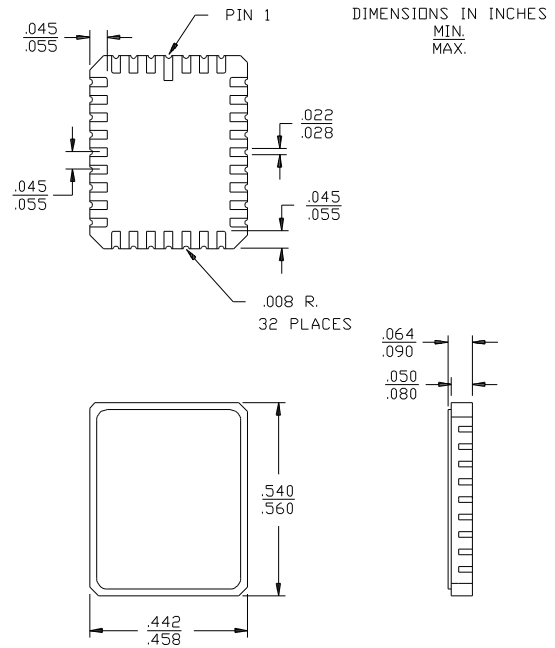
Document #: 38-00142-H

Package Diagrams

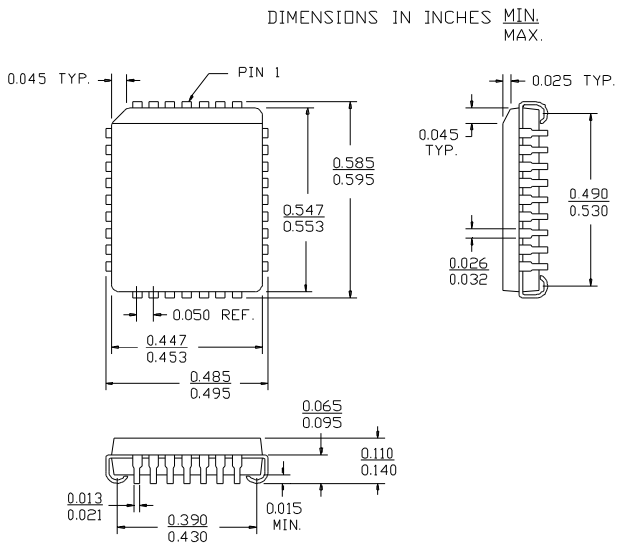
28-Lead (600-Mil) Sidebrazed DIP D43



32-Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12



32-Lead Plastic Leaded Chip Carrier



Package Diagrams

28-Lead (600-Mil) Molded DIP P15

