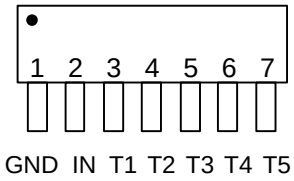
5-TAP SIP DELAY LINE
$T_D/T_R = 3$
(SERIES 1505)

data delay devices, inc.

FEATURES

- 5 taps of equal delay increment
- Very narrow device (SIP package)
- Stackable for PC board economy
- Low profile
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

PACKAGES



1505-xxz
xx = Delay (T_D)
z = Impedance Code

FUNCTIONAL DESCRIPTION

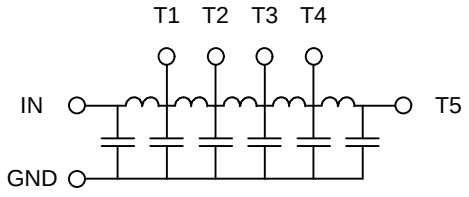
The 1505-series device is a fixed, single-input, five-output, passive delay line. The signal input (IN) is reproduced at the outputs (T1-T5) in equal increments. The delay from IN to T5 (T_D) is given by the device dash number. The characteristic impedance of the line is given by the letter code that follows the dash number (See Table). The rise time (T_R) of the line is 33% of T_D, and the 3dB bandwidth is given by 1.05 / T_D.

PIN DESCRIPTIONS

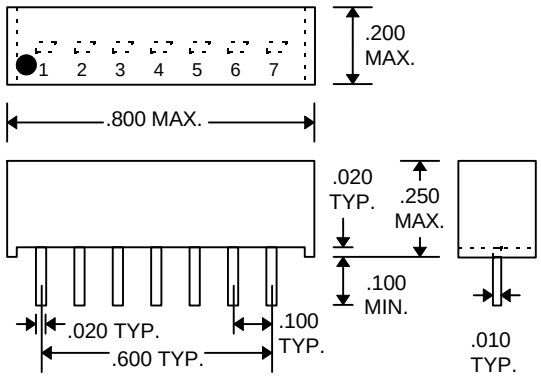
IN	Signal Input
T1-T5	Tap Outputs
GND	Ground

SERIES SPECIFICATIONS

- **Dielectric breakdown:** 50 Vdc
- **Distortion @ output:** 10% max.
- **Operating temperature:** -55°C to +125°C
- **Storage temperature:** -55°C to +125°C
- **Temperature coefficient:** 100 PPM/°C



Functional Diagram



Package Dimensions

DASH NUMBER SPECIFICATIONS

Part Number	T_D (ns)	Delay per Tap (ns)	T_R (ns)	Impedance (Ω)	R_{DC} (Ω)
1505-5A	5.0 ± 1.0	1.0 ± 0.3	2.0	50	0.6
1505-10A	10.0 ± 1.0	2.0 ± 0.4	3.0	50	0.6
1505-20A	20.0 ± 1.5	4.0 ± 0.6	6.0	50	0.7
1505-30A	30.0 ± 2.0	6.0 ± 1.0	9.0	50	0.7
1505-40A	40.0 ± 2.5	8.0 ± 1.5	12.0	50	0.9
1505-50A	50.0 ± 3.0	10.0 ± 1.8	15.0	50	1.0
1505-60A	60.0 ± 3.0	12.0 ± 2.0	18.0	50	1.2
1505-70A	70.0 ± 3.5	14.0 ± 2.0	21.0	50	1.4
1505-80A	80.0 ± 4.0	16.0 ± 2.0	24.0	50	1.6
1505-90A	90.0 ± 5.0	18.0 ± 3.0	27.0	50	1.8
1505-100A	100 ± 5.0	20.0 ± 3.0	30.0	50	2.0
1505-5B	5.0 ± 1.0	1.0 ± 0.3	2.0	100	0.7
1505-10B	10.0 ± 1.0	2.0 ± 0.4	3.0	100	0.7
1505-20B	20.0 ± 1.5	4.0 ± 0.6	6.0	100	1.0
1505-30B	30.0 ± 2.0	6.0 ± 1.0	9.0	100	1.5
1505-40B	40.0 ± 2.5	8.0 ± 1.5	12.0	100	1.8
1505-50B	50.0 ± 3.0	10.0 ± 1.8	15.0	100	2.0
1505-60B	60.0 ± 3.0	12.0 ± 2.0	18.0	100	2.0
1505-75B	75.0 ± 3.5	15.0 ± 2.0	24.0	100	2.5
1505-100B	100 ± 5.0	20.0 ± 3.0	30.0	100	2.5
1505-30C	30.0 ± 2.0	6.0 ± 1.0	9.0	200	2.5
1505-50C	50.0 ± 3.0	10.0 ± 1.8	15.0	200	3.0
1505-60C	60.0 ± 3.0	12.0 ± 2.0	18.0	200	3.5
1505-100C	100 ± 5.0	20.0 ± 3.0	30.0	200	6.0
1505-50G	50.0 ± 3.0	10.0 ± 1.8	15.0	500	5.0
1505-100G	100 ± 5.0	20.0 ± 3.0	30.0	500	15.0
1505-200G	200 ± 10.0	40.0 ± 6.0	60.0	500	21.0
1505-300G	300 ± 15.0	60.0 ± 8.0	90.0	500	29.0

PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

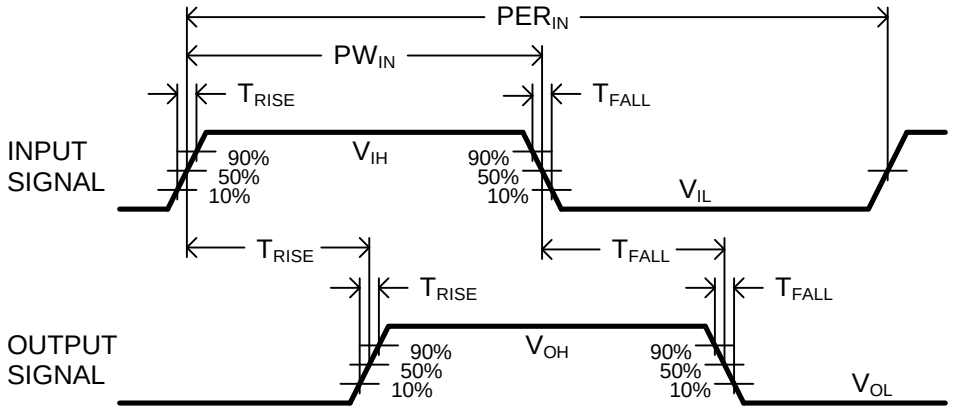
INPUT:

Ambient Temperature:	25°C ± 3°C
Input Pulse:	High = 3.0V typical Low = 0.0V typical
Source Impedance:	50Ω Max.
Rise/Fall Time:	3.0 ns Max. (measured at 10% and 90% levels)
Pulse Width (T_D <= 75ns):	PW_{IN} = 100ns
Period (T_D <= 75ns):	PER_{IN} = 1000ns
Pulse Width (T_D > 75ns):	PW_{IN} = 2 x T_D
Period (T_D > 75ns):	PER_{IN} = 10 x T_D

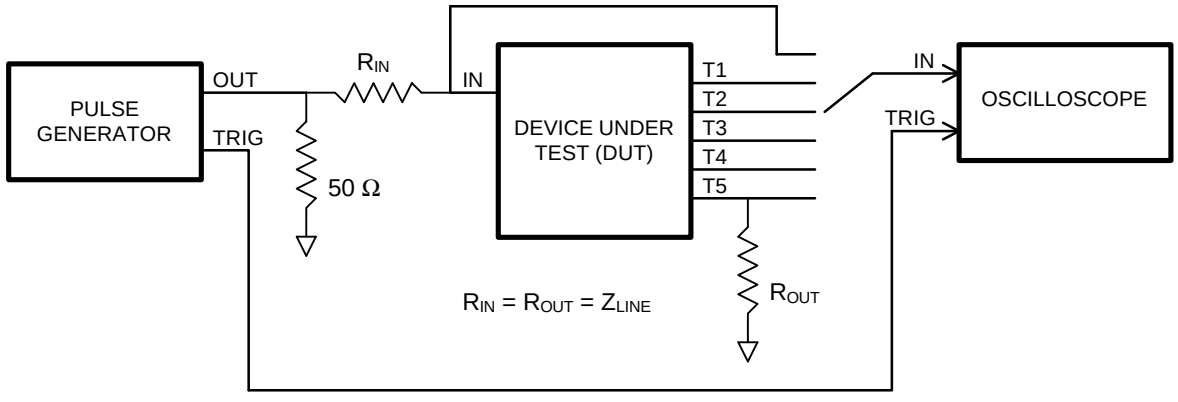
OUTPUT:

R_{load}:	10MΩ
C_{load}:	10pf
Threshold:	50% (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup