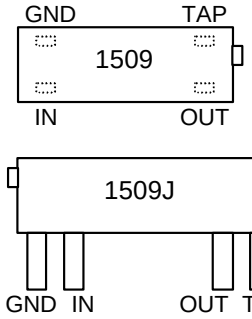
MECHANICALLY VARIABLE DELAY LINE (SERIES 1509 & 1509J)

data delay devices, inc.

FEATURES

- Ideal for "Set and Forget" applications
- Multi-turn adjustment screw
  (1509: 20 turns, 1509J: 60 turns)
- Stackable for PC board economy
- Fits standard 14-pin DIP socket (1509)
- 20mil x 10mil flat leads (1509)
- #20 gauge leads (1509J)
- **Resolution:** As low as 0.15ns
- **Dielectric breakdown:** 50 Vdc
- **Temperature coefficient:** 200 PPM/°C

PACKAGES



1509-xxz
1509J-xxz
xx = Max Delay (T_D)
z = Impedance Code

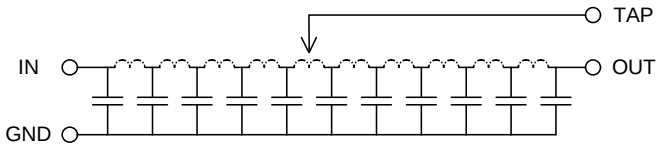
FUNCTIONAL DESCRIPTION

The 1509- and 1509J-series devices are mechanically variable, passive delay lines. The signal input (IN) is reproduced at the tap output (TAP), shifted by an amount which can be adjusted between 0 and T_D, where T_D is the device dash number. The fixed output (OUT) reproduces the input, delayed by T_D, and must be terminated to match the characteristic impedance of the line, which is given by the letter code that follows the dash number (See Table). The tap output is unbuffered. The 3dB bandwidth of the line is given by 3.5 / T_R, where T_R is the rise time of the line (See Table).

PIN DESCRIPTIONS

IN	Signal Input
TAP	Variable Output
OUT	Fixed Output
GND	Ground

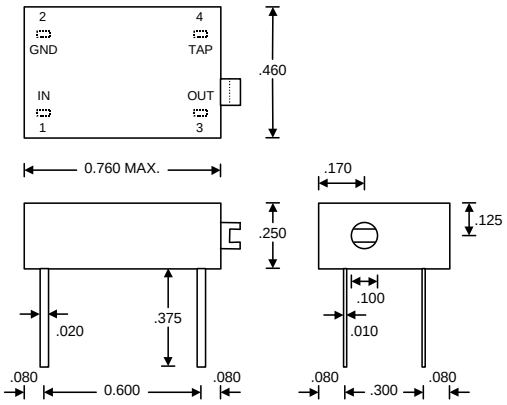
SERIES SPECIFICATIONS



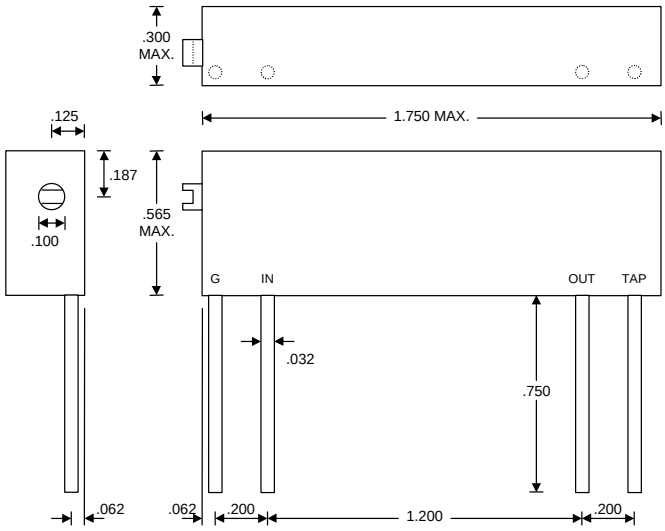
Functional Diagram

DASH NUMBER SPECIFICATIONS

Part Number	Max Dly (ns)	TR (ns)	Imped (Ω)	RDC (Ω)
1509-05B	5	3	100	0.4
1509-20C	20	8	200	1.0
1509-20D	20	8	250	1.0
1509J-10B	10	4	100	0.8
1503J-40C	40	9	200	1.5



Package Dimensions - 1509



Package Dimensions – 1509J

PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

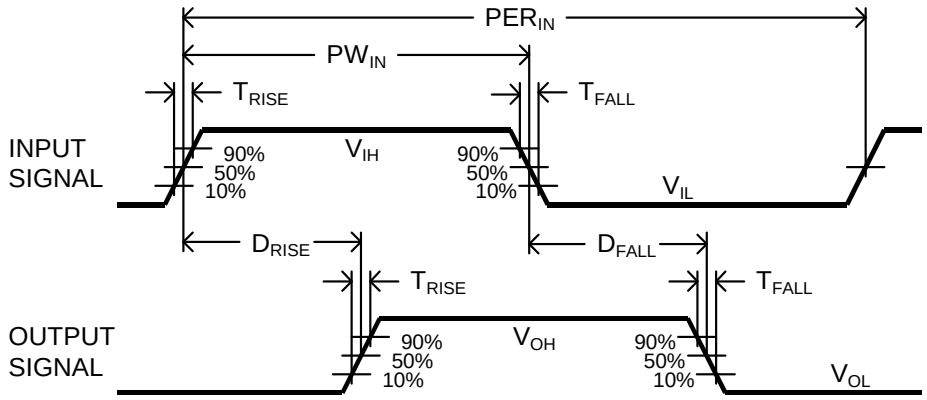
INPUT:

Ambient Temperature:	25°C ± 3°C
Input Pulse:	High = 3.0V typical
	Low = 0.0V typical
Source Impedance:	50Ω Max.
Rise/Fall Time:	3.0 ns Max. (measured at 10% and 90% levels)
Pulse Width (T_D <= 75ns):	PW_{IN} = 100ns
Period (T_D <= 75ns):	PER_{IN} = 1000ns
Pulse Width (T_D > 75ns):	PW_{IN} = 2 x T_D
Period (T_D > 75ns):	PER_{IN} = 10 x T_D

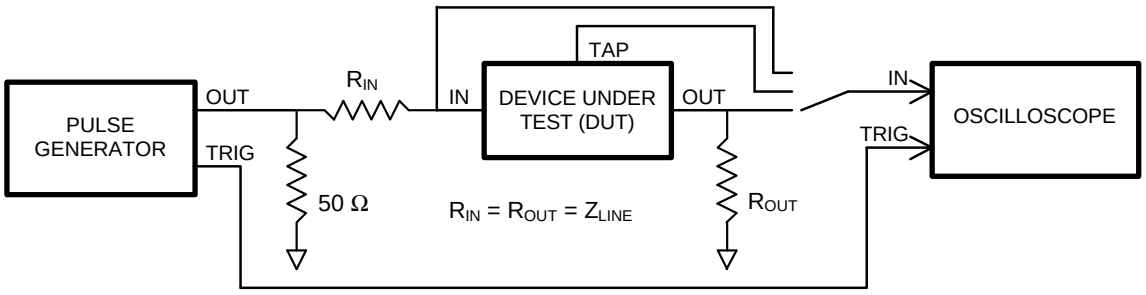
OUTPUT:

R_{load}:	10MΩ
C_{load}:	10pf
Threshold:	50% (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup