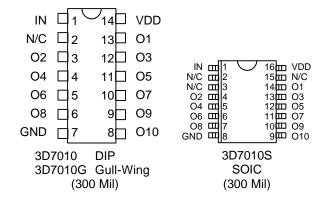
# MONOLITHIC 10-TAP FIXED DELAY LINE (SERIES 3D7010)



# FEATURES PACKAGES

- All-silicon, low-power CMOS technology\*
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Auto-insertable (DIP package)
- Low ground bounce noise
- Leading- and trailing-edge accuracy
- Delay range: 8 through 500nsDelay tolerance: 5% or 2ns
- Temperature stability: ±3% typical (0C-70C)
- **Vdd stability:** ±2% typical (4.75V-5.25V)
- Minimum input pulse width: 20% of total

delay



(For mechanical data, see Case Dimensions document)

#### **FUNCTIONAL DESCRIPTION**

The 3D7010 10-Tap Delay Line product family consists of fixed-delay CMOS integrated circuits. Each package contains a single delay line, tapped and buffered at 10 points spaced uniformly in time. Tap-to-tap (incremental) delay values can range from 8ns through 50ns. The input is reproduced at the outputs without inversion, shifted in time as per the user-specified dash number. The 3D7010 is TTL- and CMOS-compatible, capable of driving ten 74LS-type loads, and features both rising- and falling-edge accuracy.

The all-CMOS 3D7010 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL fixed delay lines. It is offered in a standard 14-pin auto-insertable DIP and a space saving surface mount 16-pin SOIC.

#### PIN DESCRIPTIONS

IIN	Delay Line Input
O1	Tap 1 Output (10%)
O2	Tap 2 Output (20%)
O3	Tap 3 Output (30%)
O4	Tap 4 Output (40%)
O5	Tap 5 Output (50%)
O6	Tap 6 Output (60%)
Ο7	Tap 7 Output (70%)
80	Tap 8 Output (80%)
O9	Tap 9 Output (90%)
O10	Tap 10 Output (100%)

Dolay Line Input

VCC +5 Volts

GND Ground

**TABLE 1: PART NUMBER SPECIFICATIONS** 

PART N	PART NUMBER		TOLERANCES		INPUT RESTRICTIONS		
DIP-14	SOIC-16	TOTAL	TAP-TO-TAP	Max Operating	Absolute Max	Min Operating	Absolute Min
3D7010	3D7010S	DELAY	DELAY	Frequency	Oper. Freq.	Pulse Width	Oper. P.W.
3D7010G		(ns)	(ns)				
-80	-80	$80 \pm 4.0$	$8.0 \pm 1.5$	4.17 MHz	31.2 MHz	120.0 ns	16.0 ns
-90	-90	$90 \pm 4.5$	$9.0 \pm 1.7$	3.70 MHz	27.8 MHz	135.0 ns	18.0 ns
-100	-100	$100 \pm 5.0$	$10.0 \pm 2.0$	3.33 MHz	25.0 MHz	150.0 ns	20.0 ns
-150	-150	$150 \pm 7.5$	$15.0 \pm 2.0$	2.22 MHz	16.7 MHz	225.0 ns	30.0 ns
-200	-200	$200 \pm 10.0$	$20.0 \pm 2.5$	1.67 MHz	12.5 MHz	300.0 ns	40.0 ns
-250	-250	$250 \pm 12.5$	$25.0 \pm 2.5$	1.33 MHz	10.0 MHz	375.0 ns	50.0 ns
-300	-300	$300 \pm 15.0$	$30.0 \pm 3.0$	1.11 MHz	8.33 MHz	450.0 ns	60.0 ns
-400	-400	$400 \pm 20.0$	$40.0 \pm 4.0$	0.83 MHz	6.25 MHz	600.0 ns	80.0 ns
-500	-500	$500 \pm 25.0$	$50.0 \pm 5.0$	0.67 MHz	5.00 MHz	750.0 ns	100.0 ns

NOTE: Any dash number between 80 and 500 not shown is also available.

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\*PATENTED

## **APPLICATION NOTES**

#### OPERATIONAL DESCRIPTION

The 3D7010 ten-tap delay line architecture is shown in Figure 1. The delay line is composed of a number of delay cells connected in series. Each delay cell produces at its output a replica of the signal present at its input, shifted in time. The delay cells are matched and share the same compensation signals, which minimizes tap-to-tap delay deviations over temperature and supply voltage variations.

#### INPUT SIGNAL CHARACTERISTICS

The Frequency and/or Pulse Width (high or low) of operation may adversely impact the specified delay accuracy of the particular device. The reasons for the dependency of the output delay accuracy on the input signal characteristics are varied and complex. Therefore a **Maximum** and an **Absolute Maximum** operating input frequency and a **Minimum** and an **Absolute Minimum** operating pulse width have been specified.

#### **OPERATING FREQUENCY**

The **Absolute Maximum Operating Frequency** specification, tabulated in **Table 1**, determines the highest frequency of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable duty cycle distortion.

The **Maximum Operating Frequency** specification determines the highest frequency of the delay line input signal for which the output delay accuracy is guaranteed.

To guarantee the **Table 1** delay accuracy for input frequencies higher than the **Maximum** Operating Frequency, the 3D7010 must be tested at the user operating frequency. Therefore, to facilitate production and device identification, the part number will include a custom reference designator identifying the intended frequency of operation. The programmed delay accuracy of the device is guaranteed, therefore, only at the user specified input frequency. Small input frequency variation about the selected frequency will only marginally impact the programmed delay accuracy, if at all. Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY **DEVICES** be consulted.

#### **OPERATING PULSE WIDTH**

The Absolute Minimum Operating Pulse Width (high or low) specification, tabulated in Table 1, determines the smallest Pulse Width of the delay line input signal that can be reproduced, shifted in time at the device output, with acceptable pulse width distortion.

The **Minimum Operating Pulse Width** (high or low) specification determines the smallest Pulse Width of the delay line input signal for which the output delay accuracy tabulated in **Table 1** is guaranteed.

To guarantee the **Table 1** delay accuracy for input pulse width smaller than the **Minimum Operating Pulse Width**, the 3D7010 must be tested at the user operating pulse width.
Therefore, to facilitate production and device identification, the **part number will include a** 

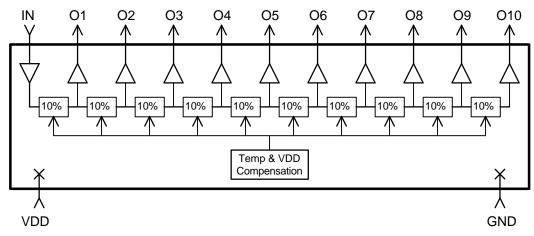


Figure 1: 3D7010 Functional Diagram

# **APPLICATION NOTES (CONT'D)**

custom reference designator identifying the intended frequency and duty cycle of operation. The programmed delay accuracy of the device is guaranteed, therefore, only for the user specified input characteristics. Small input pulse width variation about the selected pulse width will only marginally impact the programmed delay accuracy, if at all. Nevertheless, it is strongly recommended that the engineering staff at DATA DELAY DEVICES be consulted.

# **POWER SUPPLY AND** TEMPERATURE CONSIDERATIONS

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The monolithic 3D7010 programmable delay line

utilizes novel and innovative compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The thermal coefficient is reduced to 600 **PPM/C**, which is equivalent to a variation, over the 0C-70C operating range, of ±3% from the room-temperature delay settings. The power supply coefficient is reduced, over the 4.75V-5.25V operating range, to ±2% of the delay settings at the nominal 5.0VDC power supply. It is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred.

### **DEVICE SPECIFICATIONS**

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	$V_{DD}$	-0.3	7.0	V	
Input Pin Voltage	$V_{IN}$	-0.3	V <sub>DD</sub> +0.3	V	
Input Pin Current	I <sub>IN</sub>	-1.0	1.0	mA	25C
Storage Temperature	T <sub>STRG</sub>	-55	150	С	
Lead Temperature	T <sub>LEAD</sub>		300	С	10 sec

**TABLE 3: DC ELECTRICAL CHARACTERISTICS** 

(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Static Supply Current*	$I_{DD}$		15	mA	
High Level Input Voltage	$V_{IH}$	2.0		V	
Low Level Input Voltage	$V_{IL}$		0.8	V	
High Level Input Current	I <sub>IH</sub>		10	μΑ	$V_{IH} = V_{DD}$
Low Level Input Current	I <sub>IL</sub>		-250	μΑ	$V_{IL} = 0V$
High Level Output Current	I <sub>OH</sub>	-4.0		mA	$V_{DD} = 4.75V$
					$V_{OH} = 2.4V$
Low Level Output Current	I <sub>OL</sub>	4.0		mA	$V_{DD} = 4.75V$
					$V_{OL} = 0.4V$
Output Rise & Fall Time	T <sub>R</sub> & T <sub>F</sub>		2	ns	$C_{LD} = 5 pf$

 $<sup>*</sup>I_{DD}(Dynamic) = 10 * C_{LD} * V_{DD} * F$ where: C<sub>LD</sub> = Average capacitance load/tap (pf) F = Input frequency (GHz)

Input Capacitance = 10 pf typical Output Load Capacitance  $(C_{LD}) = 25 \text{ pf max}$ 

# SILICON DELAY LINE AUTOMATED TESTING

#### **TEST CONDITIONS**

INPUT: Ambient Temperature:  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$ Supply Voltage (Vcc):  $5.0\text{V} \pm 0.1\text{V}$ 

**Input Pulse:** High =  $3.0V \pm 0.1V$ 

Low =  $0.0V \pm 0.1V$ 

**Source Impedance:**  $50\Omega$  Max.

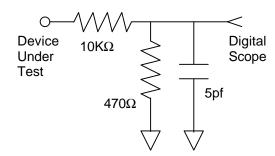
Rise/Fall Time: 3.0 ns Max. (measured

between 0.6V and 2.4V)

**Pulse Width:**  $PW_{IN} = 1.25 \text{ x Total Delay}$ **Period:**  $PER_{IN} = 2.5 \text{ x Total Delay}$  **OUTPUT:** 

 $R_{load}$ : 10KΩ ± 10%  $C_{load}$ : 5pf ± 10%

Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

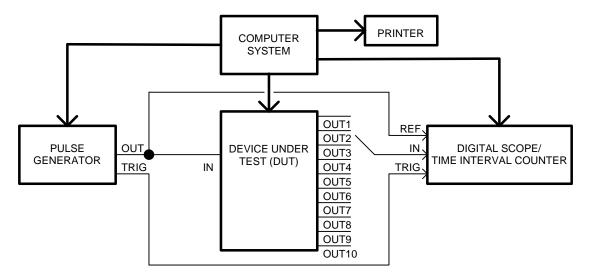


Figure 2: Test Setup

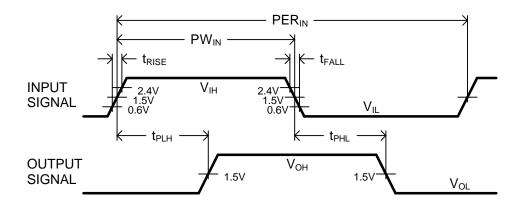


Figure 3: Timing Diagram