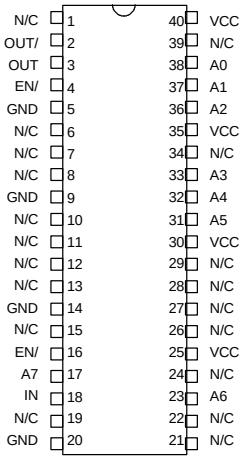
# 8-BIT PROGRAMMABLE DELAY LINE (SERIES PDU18F)

data delay devices, inc.

## FEATURES

- Digitally programmable in 256 delay steps
- Monotonic delay-versus-address variation
- Two separate outputs: inverting & non-inverting
- Precise and stable delays
- Input & outputs fully TTL interfaced & buffered
- 10 $T^2L$ fan-out capability
- Fits standard 40-pin DIP socket
- Auto-insertable

## PACKAGES




PDU18F-xx
DIP
PDU18F-xxC5
Gull-Wing
PDU18F-xxM
Military DIP
PDU18F-xxMC5
Military Gull-Wing

## FUNCTIONAL DESCRIPTION

The PDU18F-series device is a 8-bit digitally programmable delay line. The delay, $TD_A$, from the input pin (IN) to the output pins (OUT, OUT/) depends on the address code (A7-A0) according to the following formula:

$$TD_A = TD_0 + T_{INC} * A$$

where A is the address code, $T_{INC}$ is the incremental delay of the device, and $TD_0$ is the inherent delay of the device. The incremental delay is specified by the dash number of the device and can range from 0.5ns through 10ns, inclusively. The enable pins (EN/) are held LOW during normal operation. These pins must always be in the same state and may be tied together externally. When these signals are brought HIGH, OUT and OUT/ are forced into LOW and HIGH states, respectively. The address is not latched and must remain asserted during normal operation.

## PIN DESCRIPTIONS

| | |
|---|---|
| IN | Delay Line Input |
| OUT | Non-inverted Output |
| OUT/ | Inverted Output |
| A0-A7 | Address Bits |
| EN/ | Output Enable |
| VCC | +5 Volts |
| GND | Ground |

## SERIES SPECIFICATIONS

- **Programmed delay tolerance:** 5% or 2ns, whichever is greater
- **Inherent delay ($TD_0$):** 13ns typical (OUT)
  12ns typical (OUT/)
- **Setup time and propagation delay:**
  **Address to input setup ($T_{AIS}$):** 10ns
  **Disable to output delay ($T_{DISO}$):** 6ns typ. (OUT)
- **Operating temperature:** 0° to 70° C
- **Temperature coefficient:** 100PPM/°C (excludes $TD_0$)
- **Supply voltage $V_{CC}$:** 5VDC ± 5%
- **Supply current:** $I_{CCH}$ = 65ma
  $I_{CCL}$ = 128ma
- **Minimum pulse width:** 6% of total delay

## DASH NUMBER SPECIFICATIONS

| Part Number | Incremental Delay Per Step (ns) | Total Delay Change (ns) |
|---|---|---|
| PDU18F-.5 | .5 ± .3 | 127.5 ± 6.4 |
| PDU18F-1 | 1 ± .5 | 255 ± 12.8 |
| PDU18F-2 | 2 ± .5 | 510 ± 25.5 |
| PDU18F-3 | 3 ± 1.0 | 765 ± 38.3 |
| PDU18F-4 | 4 ± 1.0 | 1,020 ± 51.0 |
| PDU18F-5 | 5 ± 1.5 | 1,275 ± 63.8 |
| PDU18F-6 | 6 ± 1.5 | 1,530 ± 76.5 |
| PDU18F-8 | 8 ± 2.0 | 2,040 ± 102.0 |
| PDU18F-10 | 10 ± 2.0 | 2,550 ± 127.5 |

**NOTE: Any dash number between .5 and 10 not shown is also available.**

# APPLICATION NOTES

## ADDRESS UPDATE

The PDU18F is a memory device. As such, special precautions must be taken when changing the delay address in order to prevent spurious output signals. The timing restrictions are shown in Figure 1.

After the last signal edge to be delayed has appeared on the OUT pin, a minimum time, $T_{OAX}$, is required before the address lines can change. This time is given by the following relation:

$$T_{OAX} = \max \{ (A_i - A_{i-1}) * T_{INC} , 0 \}$$

where $A_{i-1}$ and $A_i$ are the old and new address codes, respectively. Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The possibility of spurious signals persists until the required $T_{OAX}$ has elapsed.

A similar situation occurs when using the EN/ signal to disable the output while IN is active. In this case, the unit must be held in the disabled state until the device is able to “clear” itself. This is achieved by holding the EN/ signal high and the IN signal low for a time given by:

$$T_{DISH} = A_i * T_{INC}$$

Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The possibility of spurious signals persists until the required $T_{DISH}$ has elapsed.

## INPUT RESTRICTIONS

There are three types of restrictions on input pulse width and period listed in the **AC Characteristics** table. The **recommended** conditions are those for which the delay tolerance specifications and monotonicity are guaranteed. The **suggested** conditions are those for which signals will propagate through the unit without significant distortion. The **absolute** conditions are those for which the unit will produce some type of output for a given input.

When operating the unit between the recommended and absolute conditions, the delays may deviate from their values at low frequency. However, these deviations will remain constant from pulse to pulse if the input pulse width and period remain fixed. In other words, the delay of the unit exhibits frequency and pulse width dependence when operated beyond the recommended conditions. Please consult the technical staff at Data Delay Devices if your application has specific high-frequency requirements.

Please note that the increment tolerances listed represent a design goal. Although most delay increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.

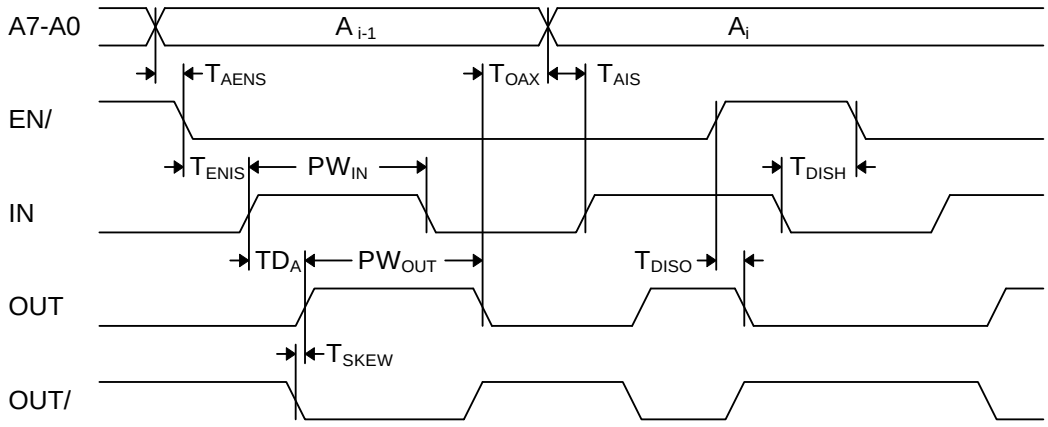



**Figure 1: Timing Diagram**

# DEVICE SPECIFICATIONS

## TABLE 1: AC CHARACTERISTICS

| PARAMETER | | SYMBOL | MIN | TYP | UNITS |
|---|---|---|---|---|---|
| Total Programmable Delay | | $TD_T$ | | 255 | $T_{INC}$ |
| Inherent Delay | | $TD_0$ | | 14.0 | ns |
| Output Skew | | $T_{SKEW}$ | | 1.5 | ns |
| Disable to Output Low Delay | | $T_{DISO}$ | | 6.0 | ns |
| Address to Enable Setup Time | | $T_{AENS}$ | 2.0 | | ns |
| Address to Input Setup Time | | $T_{AIS}$ | 10.0 | | ns |
| Enable to Input Setup Time | | $T_{ENIS}$ | 8.0 | | ns |
| Output to Address Change | | $T_{OAX}$ | See Text | | |
| Disable Hold Time | | $T_{DISH}$ | See Text | | |
| Input Period | Absolute | $PER_{IN}$ | 12 | | % of $TD_T$ |
| | Suggested | $PER_{IN}$ | 32 | | % of $TD_T$ |
| | Recommended | $PER_{IN}$ | 200 | | % of $TD_T$ |
| Input Pulse Width | Absolute | $PW_{IN}$ | 6 | | % of $TD_T$ |
| | Suggested | $PW_{IN}$ | 16 | | % of $TD_T$ |
| | Recommended | $PW_{IN}$ | 100 | | % of $TD_T$ |

## TABLE 2: ABSOLUTE MAXIMUM RATINGS

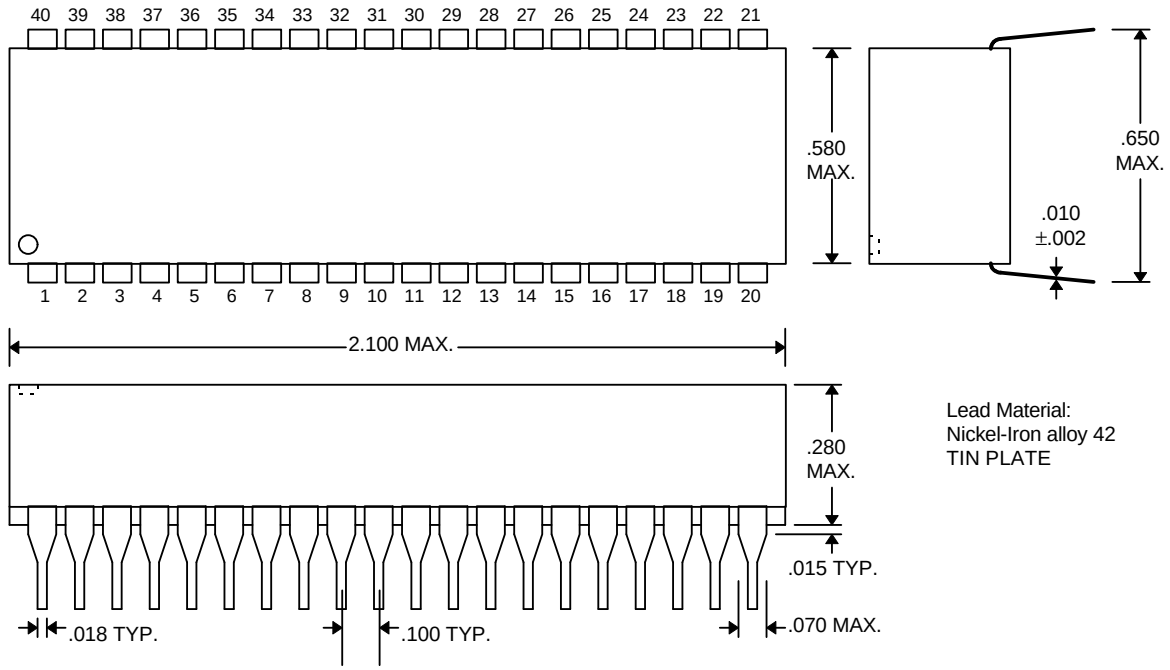
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| DC Supply Voltage | $V_{CC}$ | -0.3 | 7.0 | V | |
| Input Pin Voltage | $V_{IN}$ | -0.3 | $V_{DD}$+0.3 | V | |
| Storage Temperature | $T_{STRG}$ | -55 | 150 | C | |
| Lead Temperature | $T_{LEAD}$ | | 300 | C | 10 sec |

## TABLE 3: DC ELECTRICAL CHARACTERISTICS

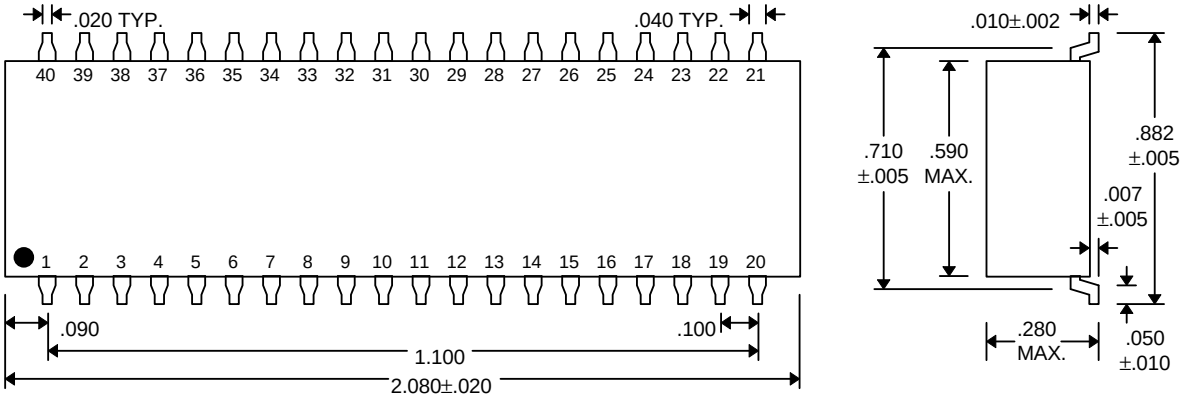
(0C to 70C, 4.75V to 5.25V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| High Level Output Voltage | $V_{OH}$ | 2.5 | 3.4 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX<br>$V_{IH}$ = MIN, $V_{IL}$ = MAX |
| Low Level Output Voltage | $V_{OL}$ | | 0.35 | 0.5 | V | $V_{CC}$ = MIN, $I_{OL}$ = MAX<br>$V_{IH}$ = MIN, $V_{IL}$ = MAX |
| High Level Output Current | $I_{OH}$ | | | -1.0 | mA | |
| Low Level Output Current | $I_{OL}$ | | | 20.0 | mA | |
| High Level Input Voltage | $V_{IH}$ | 2.0 | | | V | |
| Low Level Input Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input Clamp Voltage | $V_{IK}$ | | | -1.2 | V | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ |
| Input Current at Maximum Input Voltage | $I_{IHH}$ | | | 0.1 | mA | $V_{CC}$ = MAX, $V_I$ = 7.0V |
| High Level Input Current | $I_{IH}$ | | | 20 | µA | $V_{CC}$ = MAX, $V_I$ = 2.7V |
| Low Level Input Current | $I_{IL}$ | | | -0.6 | mA | $V_{CC}$ = MAX, $V_I$ = 0.5V |
| Short-circuit Output Current | $I_{OS}$ | -60 | | -150 | mA | $V_{CC}$ = MAX |
| Output High Fan-out | | | | 25 | Unit | |
| Output Low Fan-out | | | | 12.5 | Load | |

# PACKAGE DIMENSIONS




**DIP (PDU18F-xx, PDU18F-xxM)**



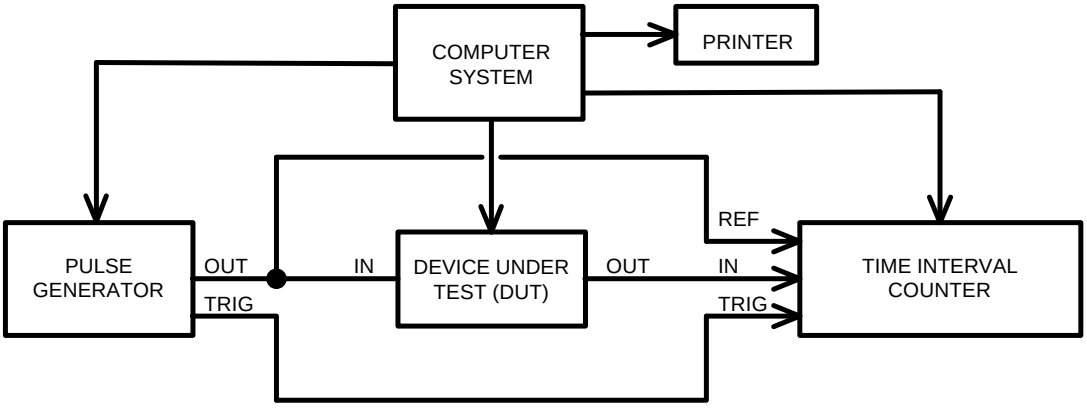

**Gull-Wing (PDU18F-xxC5, PDU18F-xxMC5)**

# DELAY LINE AUTOMATED TESTING

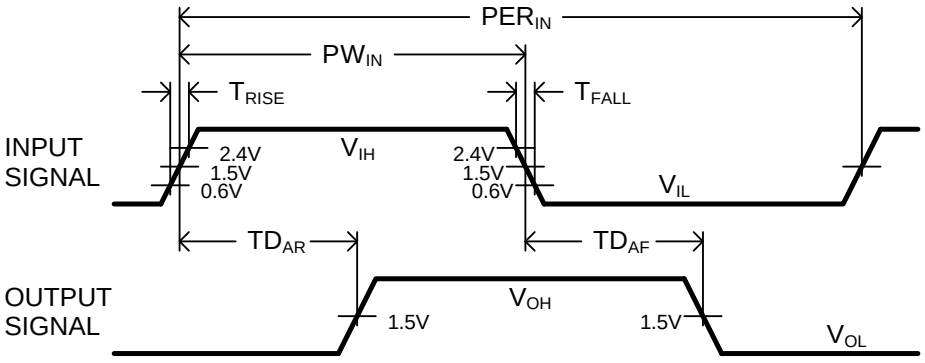
## TEST CONDITIONS

| | | | |
|---|---|---|---|
| **INPUT:** | | **OUTPUT:** | |
| **Ambient Temperature:** | 25°C ± 3°C | **Load:** | 1 FAST-TTL Gate |
| **Supply Voltage (Vcc):** | 5.0V ± 0.1V | **$C_{load}$:** | 5pf ± 10% |
| **Input Pulse:** | High = 3.0V ± 0.1V<br>Low = 0.0V ± 0.1V | **Threshold:** | 1.5V (Rising & Falling) |
| **Source Impedance:** | 50Ω Max. | | |
| **Rise/Fall Time:** | 3.0 ns Max. (measured between 0.6V and 2.4V ) | | |
| **Pulse Width:** | $PW_{IN}$ = 1.5 x Total Delay | | |
| **Period:** | $PER_{IN}$ = 4.5 x Total Delay | | |

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.




**Test Setup**




**Timing Diagram For Testing**