DS1834/A/D
Dual EconoReset with Pushbutton

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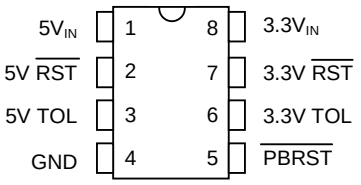
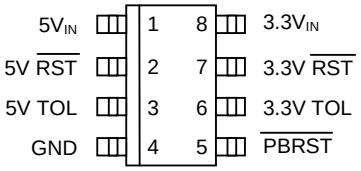
FEATURES

- 5V power-on reset
- 3.3V power-on reset
- Internal power is drawn from higher of either the $5V_{IN}$ input or the $3.3V_{IN}$ input
- Excellent for systems designed to operate with dual power supplies
- Asserts resets during power transients
- Pushbutton reset input for system override
- Maintains reset for 350 ms after V_{CC} returns to an in-tolerance condition
- Reduces need for discrete components
- Precision temperature-compensated voltage reference and voltage sensor
- 8-pin DIP, 8-pin SOIC, and 8-pin µ-SOP available
- CMOS output for low current operation on the DS1834 and DS1834D
- Operating temperature of -40°C to +85°C

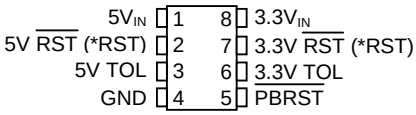
PIN ASSIGNMENT



DS1834 8-Pin DIP (300-mil)



DS1834 8-Pin SOIC (150-mil)



DS1834 8-Pin µ-SOP (118-mil)

PIN DESCRIPTION

$5V_{IN}$	- 5V Power Supply Input
5V $\overline{RST}$ (*RST)	- 5V Reset Output
5V TOL	- Selects 5V Input Tolerance
GND	- Ground
$\overline{PBRST}$	- Pushbutton Reset
3.3V TOL	- Selects 3.3V Input Tolerance
3.3V $\overline{RST}$ (*RST)	- 3.3V Reset Output
$3.3V_{IN}$	- 3.3V Power Supply Input

*DS1834D Active High Reset

DESCRIPTION

The DS1834 Dual EconoResets monitors three vital system conditions: 5-volt supply, 3.3-volt supply, and an external override. First a precision temperature reference and comparator circuit monitor the status of the 5-volt supply and the 3.3-volt supply. When an out-of-tolerance condition is detected, an internal power-fail signal is generated which forces the reset of the affected supply to an active state.

Lastly, the DS1834 supports an external reset via an internally debounced pushbutton input. When the pushbutton is pulled low both resets will be asserted for approximately 350 ms after the pushbutton is released.

OPERATION

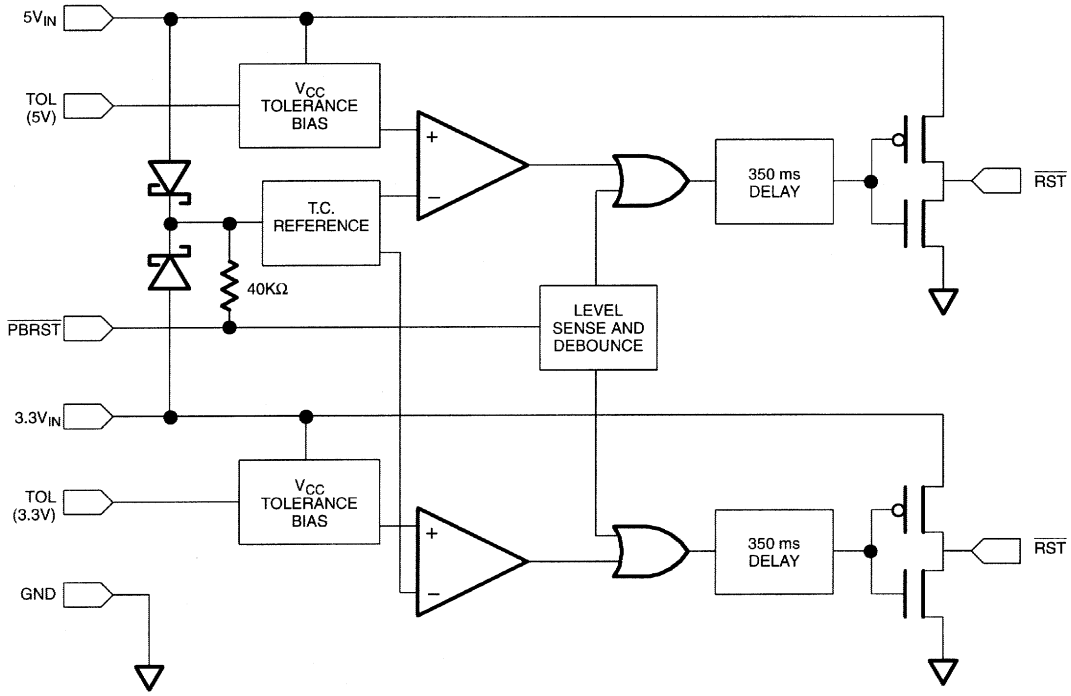
Power Monitor

The DS1834 provides the functions of detecting out-of-tolerance conditions on a 3.3-volt and 5-volt power supply and warning a processor-based system of impending power failure. When an input is detected as out of tolerance on either voltage input the RST for that supply will be forced active. When that input returns to a valid state the RST will remain active for about 350 ms and then return to an inactive state until the next input out-of-tolerance condition.

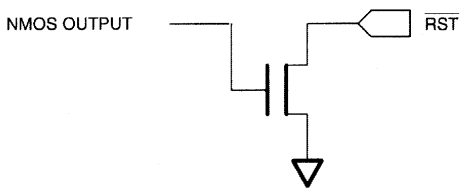
On power-up both resets are kept active for approximately 350 ms after the power supply inputs have reached the selected tolerance. This allows the power supply and system power to stabilize before RST is released.

All internal operating current for the DS1834 will be drawn from the input with the highest voltage level. The outputs will draw current only from the controlling input (5V IN or 3.3V IN).

DS1834 BLOCK DIAGRAM Figure 1



DS1834A BLOCK DIAGRAM OUTPUT Figure 2



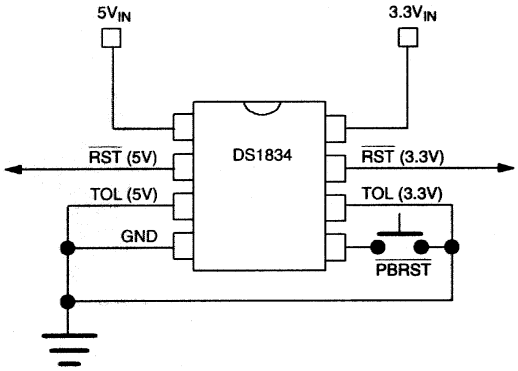
Tolerance Select

The DS1834 provides two TOL inputs for individual customization of the DS1834 to specific application requirements. If the TOL for the 5-volt supply is tied to the 5-volt input a 10% tolerance is selected for the 5 volt supply. If the TOL for the 3.3-volt supply is tied to the 3.3-volt input, a 20% tolerance is selected for the 3.3-volt supply. If TOL inputs are tied to ground, the 5-volt input will be set at a 5% tolerance and the 3.3-volt input would be set to a 10% tolerance.

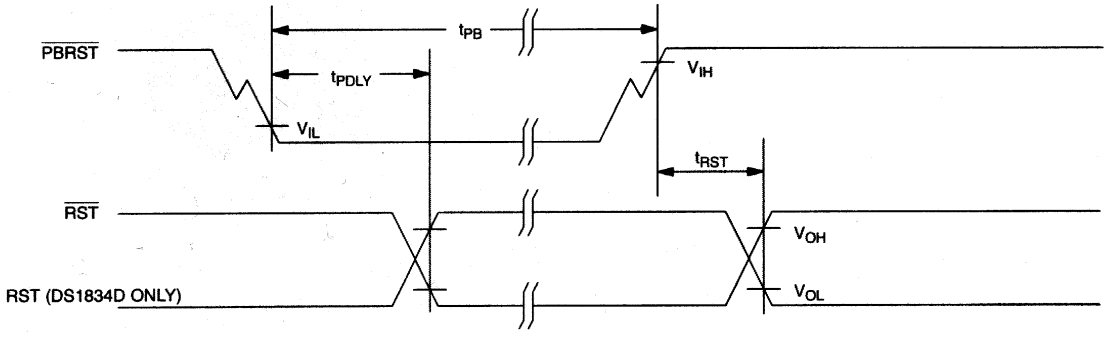
Pushbutton Reset

The DS1834 provides a pushbutton switch for manual reset control. When at least one of the DS1834 resets are not in a reset cycle, a pushbutton reset can be generated by pulling the $\overline{\text{PBRST}}$ pin low for at least 2 ms. When the pushbutton is held low, both resets are forced active and will remain active for about 350 ms after the pushbutton is released. The pushbutton input is pulled high through an internal 40 kΩ pull-up resistor and debounced via internal circuitry. See Figure 3 for an application example and Figure 4 for the timing diagram.

PUSHBUTTON RESET Figure 3



TIMING DIAGRAM: PUSHBUTTON RESET Figure 4

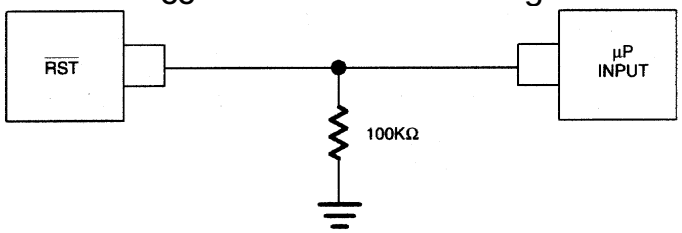


OUTPUT VALID CONDITIONS

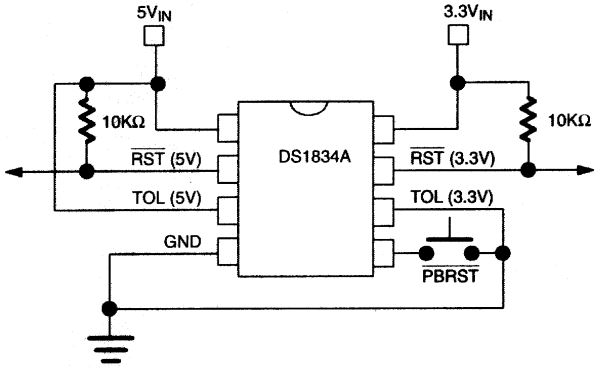
All versions of the DS1834 can maintain valid outputs as long as one input remains above 1.2 volts. However, the $\overline{RST}$ outputs on the DS1834 use a push-pull output structure which can maintain a valid output below 1.2 volts. To sink current below 1.2 volts a resistor can be connected from $\overline{RST}$ to GND (see Figure 5). This arrangement will maintain a valid value on the $\overline{RST}$ outputs even if all inputs are at 0 volts. During both power-up and power-down this arrangement will draw current when $\overline{RST}$ is in the high state. A value of about 100 kΩ should be adequate to maintain a valid condition.

The DS1834A requires pull-up resistors on the outputs to maintain a valid output. The value of the resistors is not critical in most cases but must be set low enough to pull the output to a high state. A common value used is 10 kΩs (see Figure 6 and Figure 7).

APPLICATION DIAGRAM: $\overline{RST}$ VALID TO 0 VOLTS V_{CC} ON THE DS1834 Figure 5

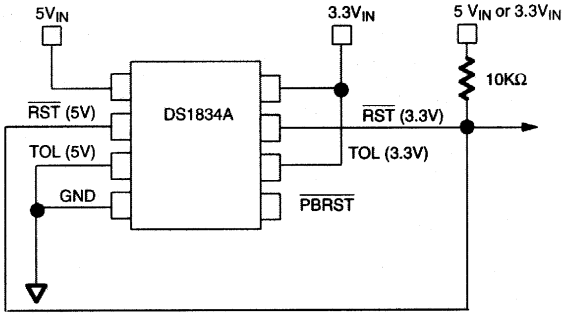


APPLICATION DIAGRAM: DS1834A NMOS OUTPUTS Figure 6

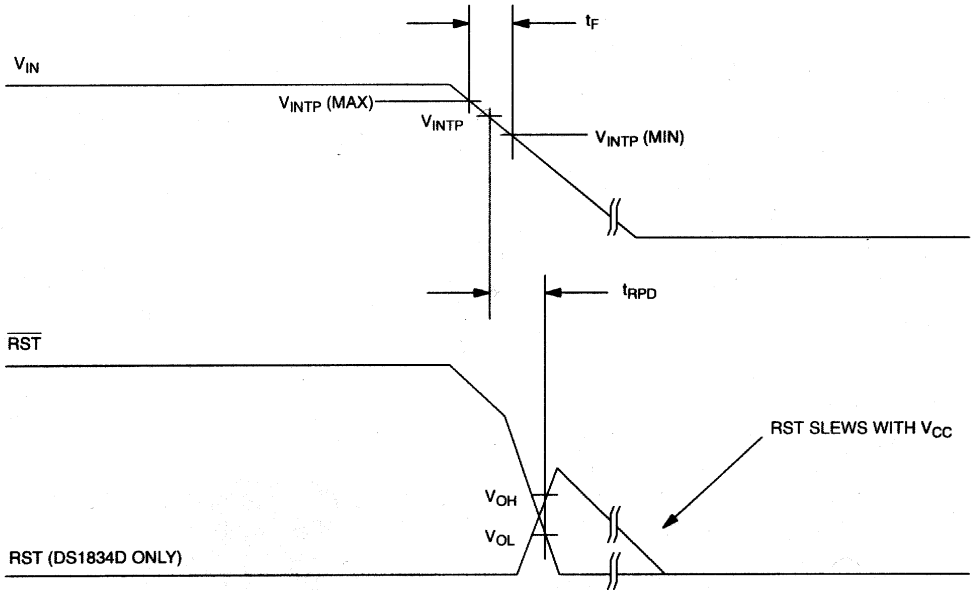


Note: If outputs are pulled-up to different voltages the outputs can not be connected to form a wired "AND".

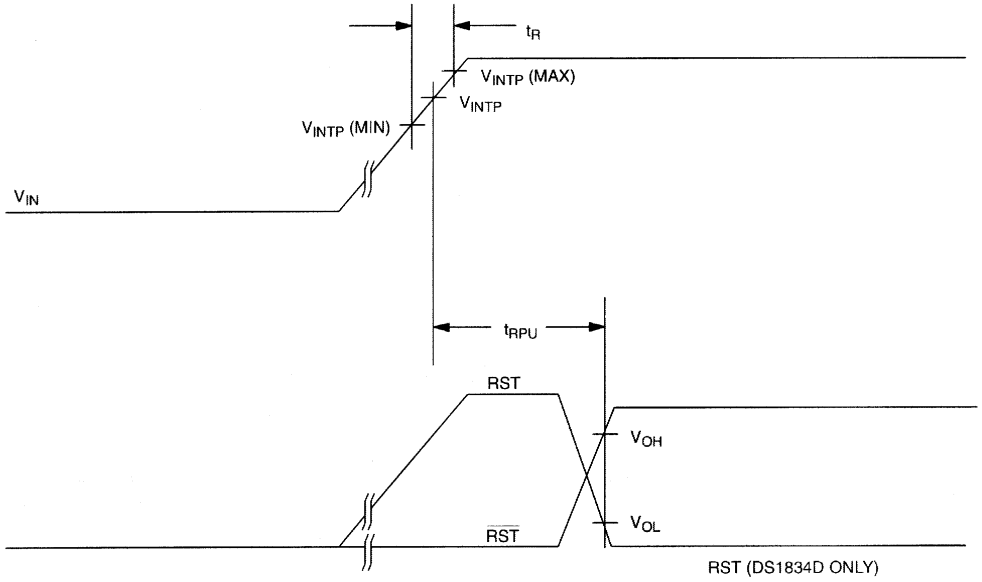
APPLICATION DIAGRAM: DS1834A WIRED "AND" OUTPUT Figure 7



TIMING DIAGRAM: POWER-DOWN Figure 8



TIMING DIAGRAM: POWER-UP Figure 9



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{IN} Pin Relative to Ground	-0.5V to +7.0V
Voltage on RST (5V) Pin Relative to Ground	-0.5V to +0.5V_{IN} + 0.5V (DS1834 & DS1834D)
Voltage on RST (3.3V) Pin Relative to Ground	-0.5V to +3.3V_{IN} + 0.5V (DS1834 & DS1834D)
Voltage on $\overline{\text{PBRST}}$ & RST (DS1834A) Pin Relative to Ground	-0.5 to the greater of 0.5V_{IN} + 0.5V or 3V_{IN} + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
5V_{IN} (Supply Voltage)	V_{IN}	1.2		5.5	V	1
3V_{IN} (Supply Voltage)	V_{IN}	1.2		5.5	V	1
$\overline{\text{PBRST}}$ Input High Level	V_{IH}	2 $V_{IN(MAX)}$ -0.4		$V_{IN(MAX)}$ +0.3	V V	1 1, 3
$\overline{\text{PBRST}}$ Input Low Level	V_{IL}	-0.3		0.5	V	1

DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_{OH}		V_{IN} -0.1V		V	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	4
Output Current @ 2.4V	I_{OH}		350		µA	5
Output Current @ 0.4V	I_{OL}	+10			mA	5
Operating Current @ ≦ 5.5V_{IN}	I_{CC}			50	µA	6
Operating Current @ ≦ 3.6V_{IN}	I_{CC}			35	µA	7
5V_{IN} Trip Point (TOL=GND)	V_{INTP}	4.50	4.63	4.75	V	1
5V_{IN} Trip Point (TOL=5V_{IN})	V_{INTP}	4.25	4.38	4.49	V	1
3.3V_{IN} Trip Point (TOL=GND)	V_{INTP}	2.80	2.88	2.97	V	1
3.3V_{IN} Trip Point (TOL=3.3V_{IN})	V_{INTP}	2.47	2.55	2.64	V	1
Output Capacitance	C_{OUT}			10	pF	

AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; V_{CC}=1.2V to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{PBRST}$ = V_{IL}	t_{PB}	2			ms	
$\overline{PBRST}$ Stable Low to Reset Active	t_{PDLY}			2	ms	
Reset Active Time	t_{RST}	200	350	500	ms	
V_{CC} Detect to $\overline{RST}$ (or RST)	t_{RPD}			2	µs	8
V_{CC} Slew Rate ($V_{INTP(MAX)}$ to $V_{INTP(MIN)}$)	t_F	300			µs	
V_{CC} Slew Rate ($V_{INTP(MIN)}$ to $V_{INTP(MAX)}$)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$ (or RST)	t_{RPU}	200	350	500	ms	9

NOTES:

1. All voltages are referenced to ground.
2. Measured with both $3.3V_{IN}$ and $5V_{IN}$ 2.7V.
3. Measured with both $3.3V_{IN}$ and $5V_{IN} \leq 2.7V$.
4. $\overline{PBRST}$ is internally pulled up to $V_{IN(MAX)}$ input with an internal impedance of approximately 40 kΩ.
5. Measured with either $3.3V_{IN}$ or $5V_{IN}$ 2.7V (valid for DS1834 and DS1834D only).
6. Measured with outputs open and both $3.3V_{IN}$ and $5V_{IN} \leq 5.5V$.
7. Measured with outputs open and both $3.3V_{IN}$ and $5V_{IN} \leq 3.6V$.
8. Noise immunity - pulses < 2 µs @ V_{CCTP} minimum will not generate a reset.
9. t_R =5 µs.

MARKING:

	DS1834	DS1834A	DS1834D
8-pin DIP	DS1834	DS1834A	DS1834D
8-pin SOIC	DS1834	DS1834A	DS1834D
8-pin µ-SOP	834	834A	834D