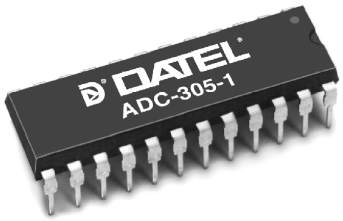
ADC-305
8-Bit, 20MHz CMOS A/D Converters

FEATURES

- **8-bit resolution, 20MHz min. sampling rate**
- **±½LSB max. differential nonlinearity error**
- **18MHz input signal bandwidth**
- **Subranging, S&H enclosed**
- **+5V single power, low 85mW max. dissipation**
- **CMOS compatible logic input**
- **3-State TTL compatible output**



GENERAL DESCRIPTION

DATEL's ADC-305 is an 8-bit, 20MHz sampling, CMOS, subranging (two-pass) A/D converter. It processes signals at speeds comparable to a full flash converter by using a sub-ranging conversion technique with multiple comparator blocks, each containing a sample and hold amplifier.

The ADC-305 features CMOS low power dissipation (60mW typical) and a wide 18MHz (–1dB) input signal bandwidth. The ADC-305-1 is packaged in 400 mil 24-pin DIP and the ADC-305-3 in 300 mil 24-pin SOP.

Other features are CMOS compatible input logic, 3-state TTL compatible output logic, +5V single power operation, self bias mode and low cost.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$)	24	DGND
2	DGND	23	REF. BOTTOM (V_{RB})
3	BIT 8 (LSB)	22	SELF BIAS 1 (V_{RBS})
4	BIT 7	21	AGND
5	BIT 6	20	AGND
6	BIT 5	19	ANALOG INPUT (V_{IN})
7	BIT 4	18	+AVS (+5V)
8	BIT 3	17	REFERENCE TOP (V_{RT})
9	BIT 2	16	SELF BIAS 2 (V_{RTS})
10	BIT 1 (MSB)	15	+AVS (+5V)
11	+DVS (+5V)	14	+AVS (+5V)
12	CLOCK INPUT (A/D CLK)	13	+DVS (+5V)

Both the ADC-305-1 and the ADC-305-3 have the same pin assignment.

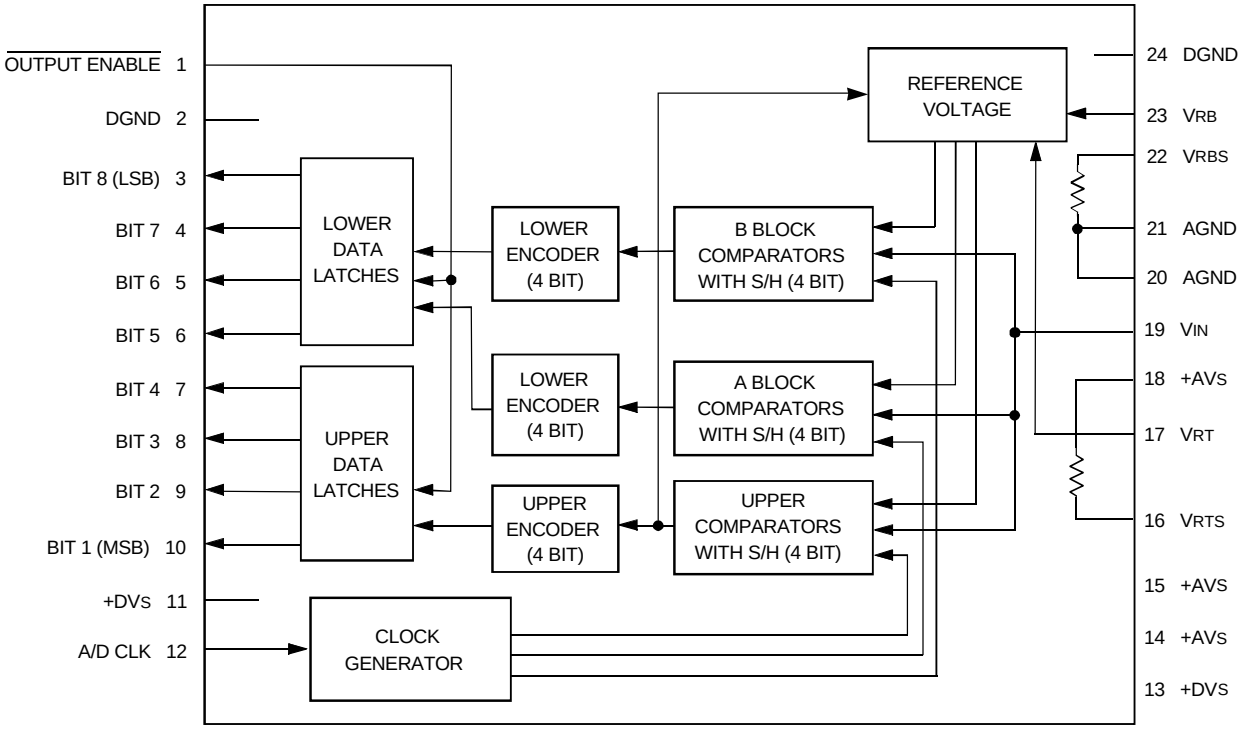


Figure 1. Functional Block Diagram

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

PARAMETERS	MIN	MAX	UNITS
Power Supply Voltage (+AVs, +DVs)	–0.5	+7	Volts
Analog Input Voltage (V_{IN})	–0.5	+AVs +0.5	Volts
Reference Input Voltage (V_{RT}, V_{RB})	–0.5	+AVs +0.5	Volts
Digital Input Voltage (V_{IH}, V_{IL})	–0.5	+DVs +0.5	Volts
Digital Output Voltage (V_{OH}, V_{OL})	–0.5	+DVs +0.5	Volts

FUNCTIONAL SPECIFICATIONS

(Specification are typical at T_A = +25°C, +V_{RT} = +2.5V, V_{RB} = +0.5V, +AVs = +DVs = +5v, fs = 20MHz sampling unless otherwise specified.)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range (V_{IN}) ①	—	+0.5 to +2.5	—	Volts
Input Capacitance	—	11	—	pF
(V_{IN} = 1.5Vdc+0.07V_{RMS})				
Input Impedance	—	12.5	—	kΩ
Input Signal Bandwidth	—	18	—	MHz
(V_{IN}-2Vp-p, –1dB)				
REFERENCE INPUTS				
Ref. Resitance V_{RT} to V_{RB}	230	300	450	Ω
Ref. Current	4.5	6.6	8.7	mA
Ref. Voltage ① V_{RT}	+1.8	—	+2.8	Volts
V_{RB}	0	—	V_{RT}	Volts
Offset Voltage V_{RT}	–10	–35	–60	mV
V_{RB}	0	+15	+45	mV
Self Bias I ① ② V_{RBS}	+0.6	+0.64	+0.68	Volts
V_{RTS}-V_{RBS}	+1.96	+2.09	+2.21	Volts
Self Bias II ① ③ V_{RTS}	+2.25	+2.39	+2.53	Volts
DIGITAL INPUTS				
Input Voltage (CMOS)				
Logic Levels (V_{IH}) "1"	+4	—	—	Volts
Logic Level (V_{IL}) "0"	—	—	+1	Volts
Input Current (@V_{IH}=+DVs)"1"	—	—	5	µA
(@V_{IL}=0) "0"	—	—	5	µA
Clock Pulse Width T_{PW1}	25	—	—	ns
(A/D CLK) T_{PW0}	25	—	—	ns
DIGITAL OUTPUTS				
Output Data	8-bit Binary Parallel			
Output Voltage	3-State TTL compatible			
Output Current ④				
Logic Level "1"	–1.1	—	—	mA
Logic Level "0"	+3.7	—	—	mA
Output Current ⑤				
Logic Level "1"	—	—	16	µA
Logic Level "0"	—	—	16	µA
Output Data Delay, Td	—	18	30	ns
PERFORMANCE				
Resolution	8	—	—	Bit
Maximum Sampling Rate	20	—	—	MHz
Minimum Sampling Rate	—	—	0.5	MHz
Aperature Delay, T_A	—	4	—	ns
Aperature Jitter	—	30	—	ps
Differential Linearity Error	—	±0.3	±0.5	LSB
Integral Linearity Error	—	+0.5	+1.3	LSB
Differential Gain Error ⑥	—	1	—	%
Differential Phase Error ⑥	—	0.5	—	deg

Footnotes:

① See Technical Note 4
② Short V_{RB} (pin 23) to V_{RBS} (pin 22). Short V_{RT} (pin 17) to V_{RTS} (pin 16).
③ Short V_{RB} (pin 23) to A GND. Short V_{RT} (pin 17) to V_{RTS} (pin 16).
④ $\overline{OE}$=OV, V_{OH}=+DVs–0.5V, V_{OL}=+0.4V
⑤ $\overline{OE}$=+DVs, V_{OH}=+DVs, V_{OL}=0V
⑥ NTSC 40IRE mode ramp, 14.3MHz sampling

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply (+AVs, +DVs)	+4.75	+5.0	+5.25	Volts
I A GND - D GND I	—	—	100	mV
Power Supply Current	—	12	17	mA
Power Dissipation	—	60	85	mW

PHYSICAL/ENVIRONMENTAL		
Operating Temp. Range		–40 to +85°C
Storage Temp. Range		–55 to +150°C
Package Type	ADC-305-1	24-pin Plastic DIP
	ADC-305-3	24-pin Plastic SOP
Weight	ADC-305-1	2.0 grams
	ADC-305-3	0.3 grams

TECHNICAL NOTES

1. The ADC-305 has separate +AVs and +DVs pins. It is recommended that both +AVs and +DVs be powered from a single supply since a time lag between start up of separate supplies could induce latch up. Other external logic circuits must be powered from a separate digital supply. +DVs (pins 11 and 13) and +AVs (pins 14, 15 and 18) should be tied together externally. DGND (pins 2 and 24) and AGND (pins 20 and 21) should also be tied together externally. Power supply grounds must be connected at one point to the ground plane directly beneath the device. Digital returns should not flow through analog grounds.
2. Bypass all power lines to ground with a 0.1µF ceramic chip capacitor in parallel with a 47µF electrolytic capacitor. Locate the bypass capacitor as close to the unit as possible.
3. Even though the analog input capacitance is a low 15pF, it is recommended that high frequency input be provided via a high speed buffer amplifier. A parasitic oscillation may be generated when a high speed amplifier is used. A 75 ohm resister inserted between the output of an amplifier and the analog input of the ADC-305 will improve the situation. A resistor larger than 100 ohms may degrade linearity.
4. The input voltage range is determined by voltages applied to V_{RB} (Reference Bottom) and V_{RT} (Reference Top). Keep to the following equations;

   $0V \le V_{RB} \le V_{RT} \le 2.8V$
   $1.8V \le V_{RT} - V_{RB} \le 2.8V$

   The analog input range is normally 2Vp-p.

Self Bias Mode

a. Tie V_{RB} to V_{RBS}, and tie V_{RT} to V_{RTS} respectively. The analog input range in this case is +0.64V to +2.73V nominal.
b. Tie V_{RB} to AGND, and tie V_{RT} to V_{RTS} respectively. The analog input voltage range is 0 to +2.39V in this case.

Table 1. Digital Output Coding

V_{IN}	CODE	STEP DEC	STEP HEX	DATA BITS OUT MSB	DATA BITS OUT LSB
Ov	Zero	0	00	0 0 0 0	0 0 0 0
↓	↓	↓	↓	↓	↓
+0.9922V	+1/2FS –1LSB	127	7F	0 1 1 1	1 1 1 1
+1.000V	+1/2FS	128	80	1 0 0 0	0 0 0 0
↓	↓	↓	↓	↓	↓
+1.9922V	+FS	255	FF	1 1 1 1	1 1 1 1

These values may differ from one device to another. Voltage changes on the +5V supply have a direct influence on the performance of the device. The use of external references is recommended for applications sensitive to gain error.

External Reference Mode

Tie V_{RB} to AGND, and apply +2V to V_{RT} to use at 0 to +2V input voltage range. The reference resistance between V_{RB} and V_{RT} is about 300 ohms. It is important to make the output impedance of the reference source small enough while, at the same time, keeping sufficient drive capacity. Insert a 0.1µF bypass ceramic chip capacitor between V_{RT} and GND to minimize the effect of the 20MHz clock running nearby. See Figure 5.

5. Logic inputs are CMOS compatible. Normally a series 74HC is used as a driver. It is recommended to pull up to +5V if the device is driven with TTL.
6. The start convert (A/D CLK) pulse can be a 50% duty cycle clock. Both T_{PW1} and T_{PW0} are 25ns minimum. A slightly longer T_{PW1} will improve linearity of the system for higher frequency input signals.
7. The digital data outputs are 3-state and TTL compatible. To enable the 3-state outputs, connect the $\overline{\text{OUTPUT ENABLE}}$ (pin 1) to GND. To disable, connect it to +5V. It is recommended that the data outputs be latched and buffered through output registers.
8. Maximum 30ns (18ns typical) after the rising edge of the Nth conversion pulse, the result of the (N-3) conversion can be obtained. Data is stored firmly in an output register, such as an 74LS574, using the rising edge of a start convert pulse as a trigger. The (N–4) data is stored in this case. See the timing diagrams, Figure 2 and 4.
9. The 20MHz sampling rate is guaranteed. It is not recommended to use this device at sampling rates slower than 500kHz because the droop characteristics of the internal sample and holds will then exceed the limit required to maintain the specified accuracy of the device.

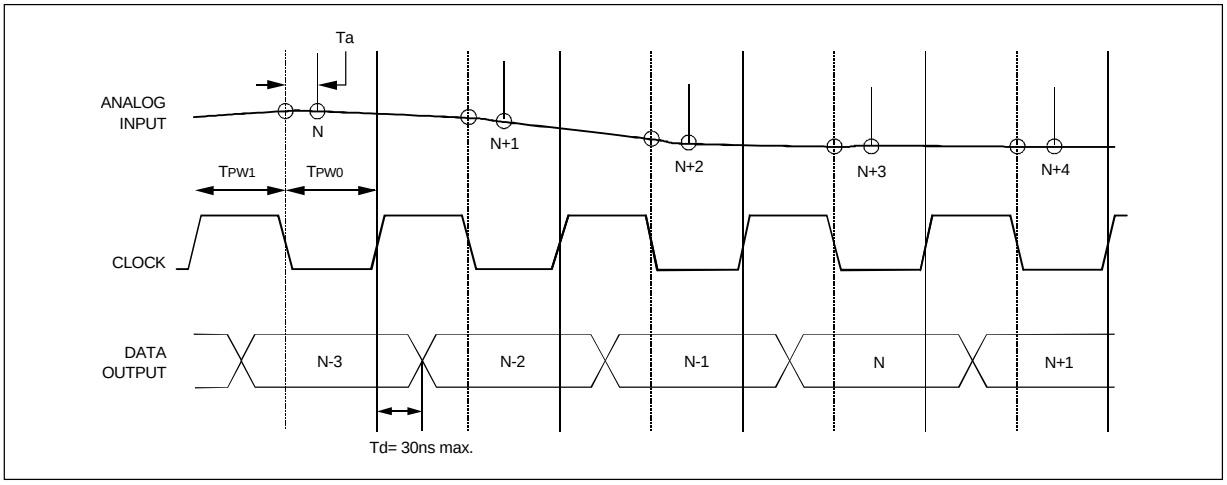


Figure 2. Timing Diagram

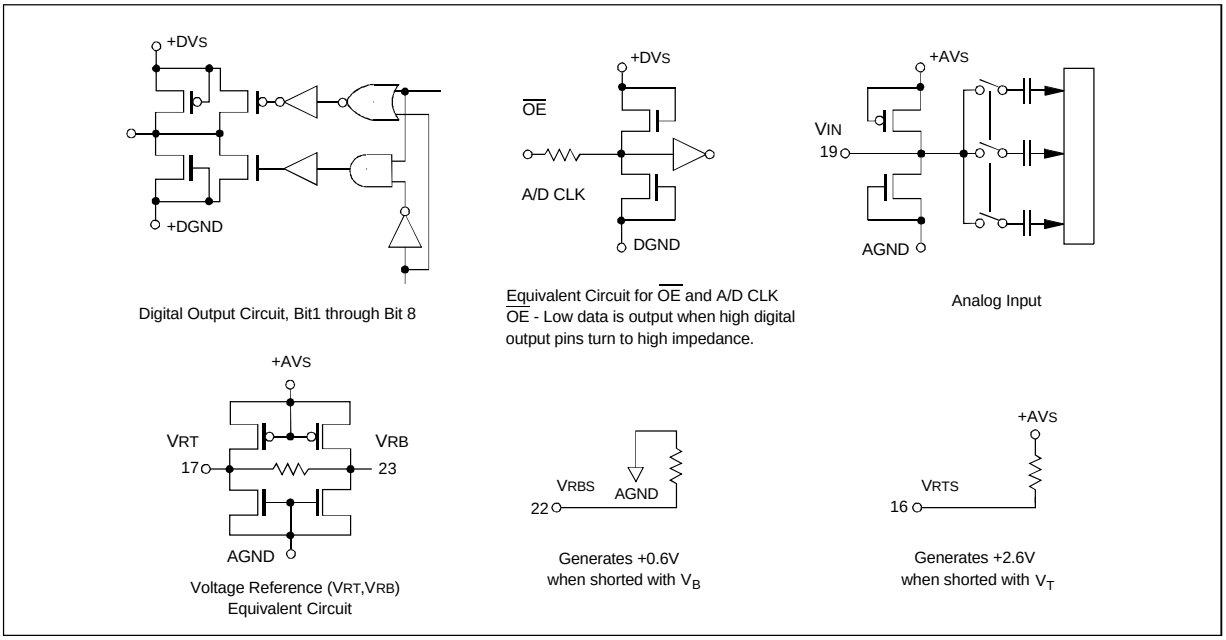


Figure 3. Equivalent Circuits

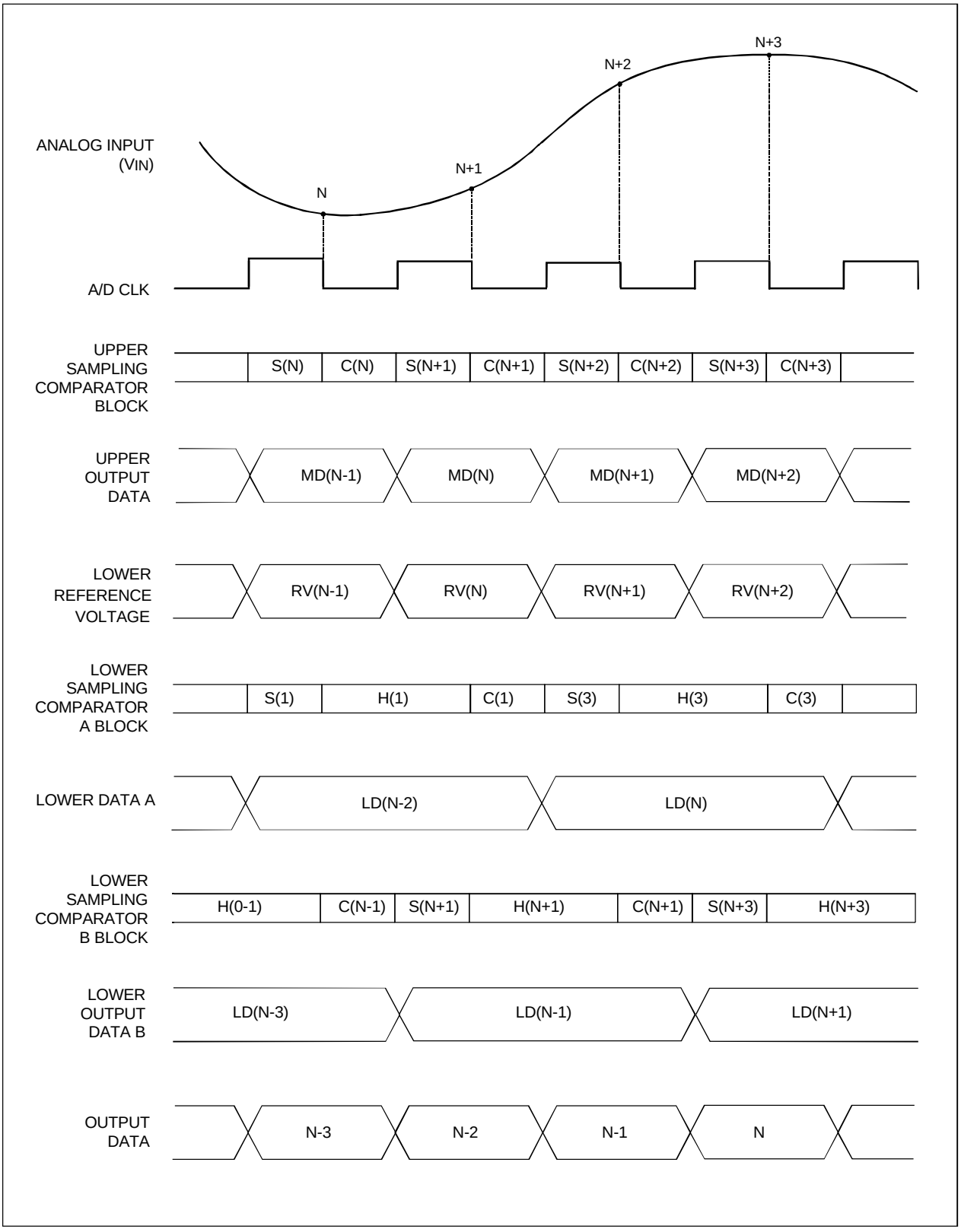


Figure 4. Timing Chart

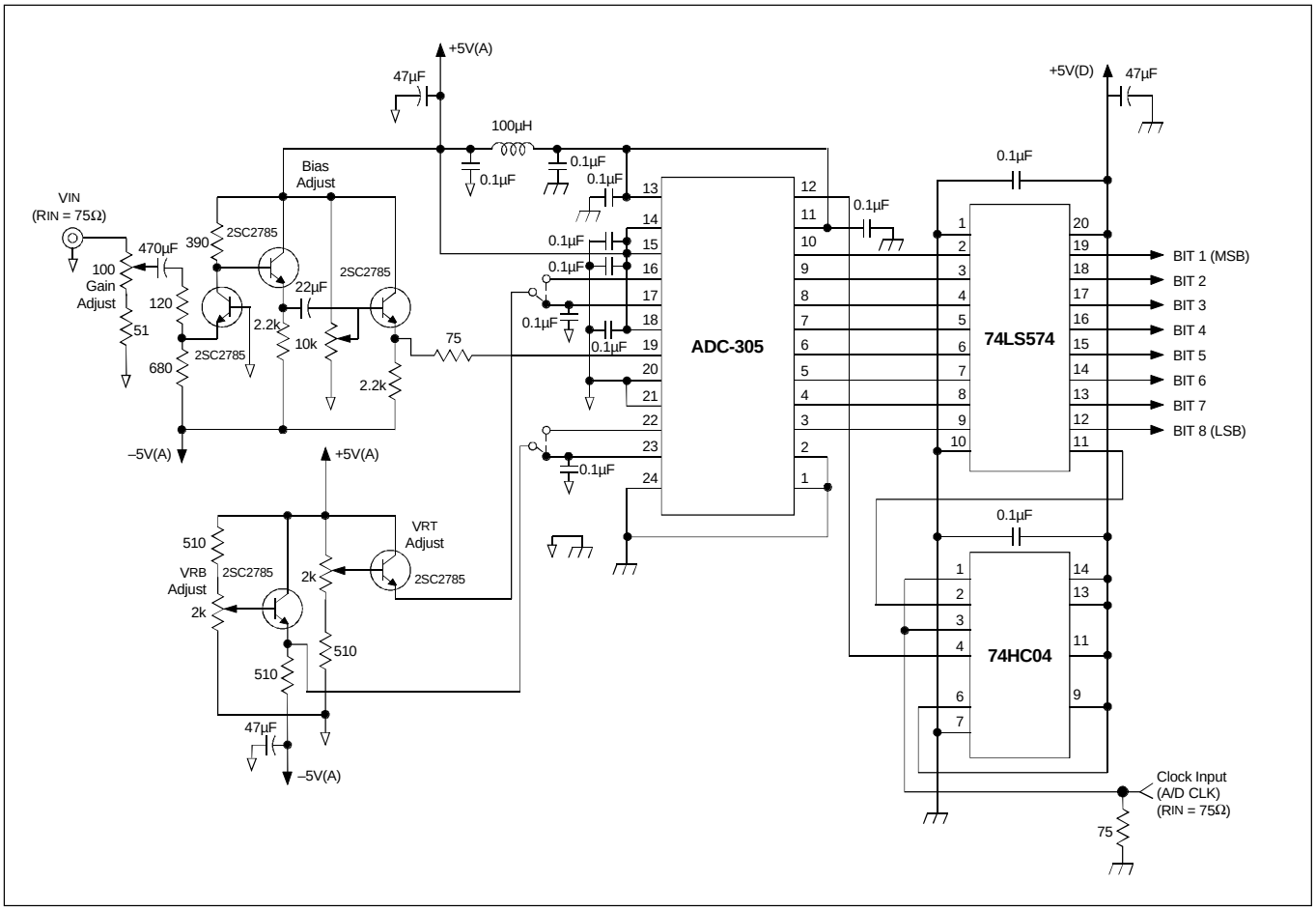


Figure 5. Typical Connection Diagram

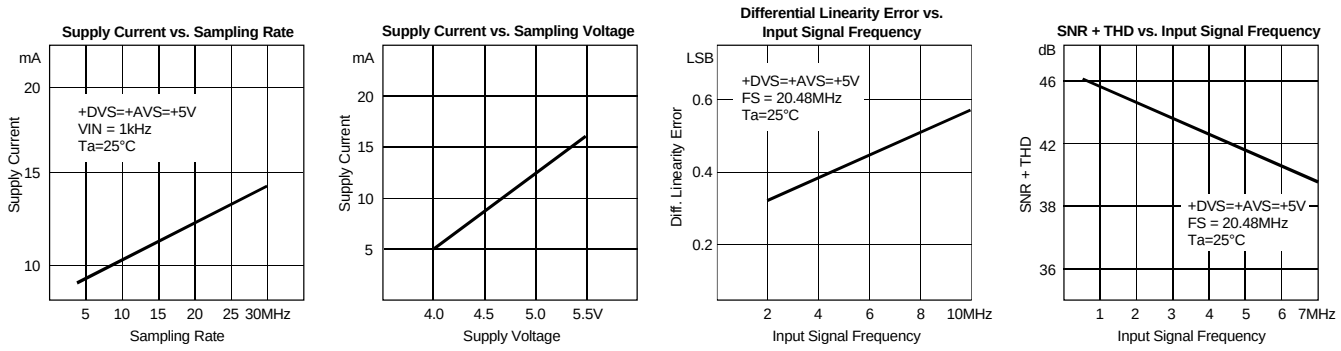
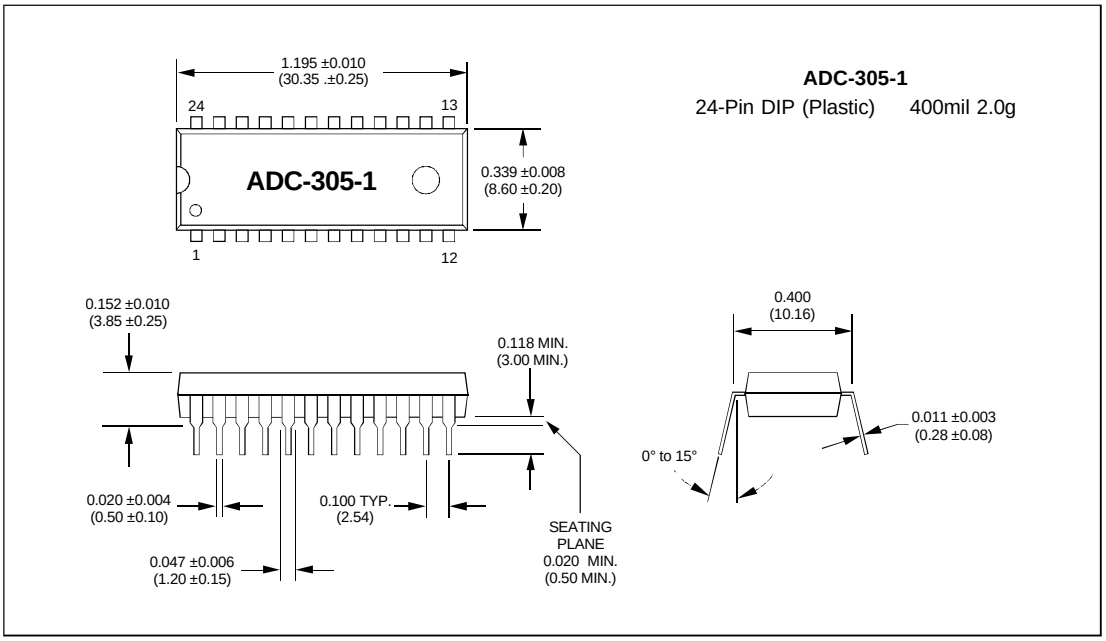
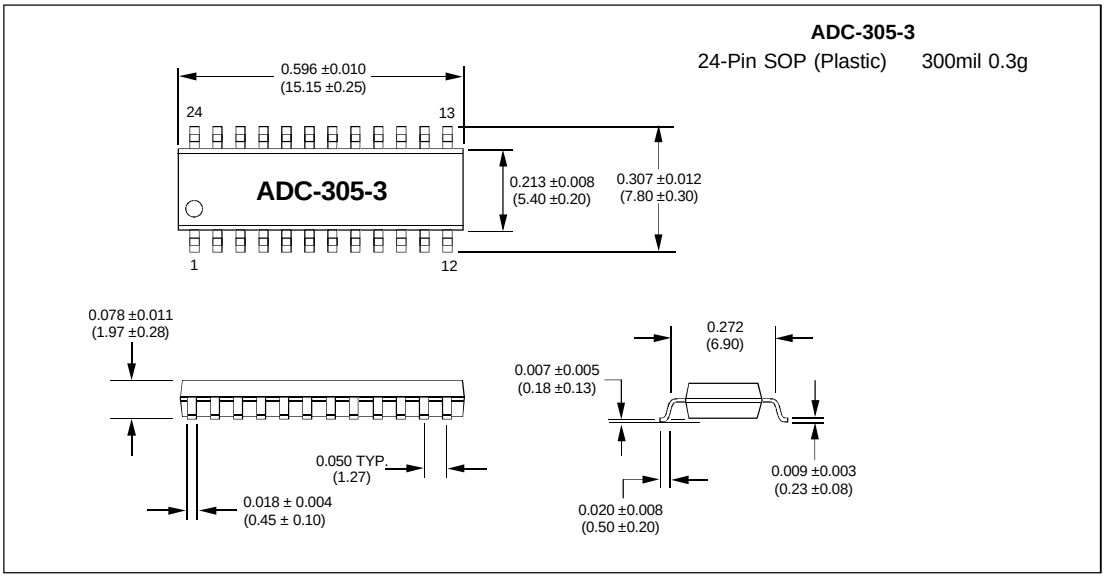


Figure 6. Typical Performance Curves

MECHANICAL DIMENSIONS INCHES (MM)



ADC-305-1
24-Pin DIP (Plastic) 400mil 2.0g



ADC-305-3
24-Pin SOP (Plastic) 300mil 0.3g

ORDERING INFORMATION

MODEL NUMBER	PACKAGE
ADC-305-1	24-Pin Plastic DIP 400 mil
ADC-305-3	24-Pin Plastic SOP 300 mil

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