élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7155C

High-Performance Pin Driver

Features

- Clocking Speeds up to 40MHz
- 15ns tr/tf at 2000pF C_{LOAD}
- 0.5ns Rise and Fall Times Mismatch
- 0.5ns T_{ON}-T_{OFF} Prop Delay Mismatch
- 3.5pF Typical Input Capacitance
- 3.5A Peak Drive
- Low on Resistance of 3.5Ω
- High Capacitive Drive Capability
- Operates from 4.5V up to 18V

Applications

- ATE/Burn-in Testers
- Level Shifting
- IGBT Drivers
- CCD Drivers

Ordering Information

Part No.	Package	Tape & Reel	Outline #
EL7155CN	8-Pin DIP	-	MDP0031
EL7155CS	8-Pin SOIC	-	MDP0027
EL7155CS-T7	8-Pin SOIC	7"	MDP0027
EL7155CS-T13	8-Pin SOIC	13"	MDP0027

General Description

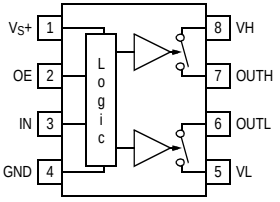
The EL7155C high-performance pin driver with tri-state is suited to many ATE and level-shifting applications. The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads.

Output pins OUTH and OUTL are connected to input pins VH and VL respectively, depending on the status of the IN pin. One of the output pins is always in tri-state, except when the OE pin is active low, in which case both outputs are in tri-state mode. The isolation of the output FETs from the power supplies enables VH and VL to be set independently, enabling level-shifting to be implemented.

This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and on-resistance characteristics.

Available in the 8-Pin SOIC and 8-Pin PDIP packages, the EL7155C is specified for operation over the -40°C to +85°C temperature range.

Pin Layout Diagram



8-Pin PDIP/SOIC

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Absolute Maximum Ratings (T_A = 25°C)

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_S+ to VL)	+18V
Input Voltage	VL -0.3V, VL+ +0.3V
Continuous Output Current	200mA
Storage Temperature Range	-65°C to +150°C
Ambient operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	see curves
Maximum ESD	2kV

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

V_S+ = +15V, VH = +15V, VL = 0V, T_A = 25°C, unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Unit
Input						
V_{IH}	Logic '1' Input Voltage		2.4			V
I_{IH}	Logic '1' Input Current	$V_{IH} = V_S$+		0.1	10	µA
V_{IL}	Logic '0' Input Voltage				0.8	V
I_{IL}	Logic '0' Input Current	V_{IL} = 0V		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
Output						
R_{OVH}	ON Resistance VH to OUTH	I_{OUT} = -200 mA		2.7	4.5	Ω
R_{OVL}	ON Resistance VL to OUTL	I_{OUT} = +200 mA		3.5	5.5	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUTH = VL, OUTL = V_S+		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
Power Supply						
I_S	Power Supply Current	Inputs = V_S+		1.3	3	mA
I_{VH}	Off Leakage at VH	VH = 0V		4	10	µA
Switching Characteristics						
t_R	Rise Time	C_L =2000 pF		14.5		ns
t_F	Fall Time	C_L = 2000 pF		15		ns
$t_{RFdelta}$	t_R, t_F Mismatch	C_L = 2000 pF		0.5		ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000 pF		9.5		ns
t_{D-2}	Turn-On Delay Time	C_L = 2000 pF		10		ns
t_{Ddelta}	t_{D-1}-t_{D-2} Mismatch	C_L = 2000 pF		0.5		ns
t_{D-3}	Tri-State Delay Enable			10		ns
t_{D-4}	Tri-State Delay Disable			10		ns

Electrical Characteristics

V_S+ = +5V, VH = +5V, VL = -5V, T_A = 25°C, unless otherwise specified.

Parameter	Description	Condition	Min	Typ	Max	Unit
Input						
V_{IH}	Logic '1' Input Voltage		2.0			V
I_{IH}	Logic '1' Input Current	$V_{IH} = V_S$+		0.1	10	µA
V_{IL}	Logic '0' Input Voltage				0.8	V
I_{IL}	Logic '0' Input Current	V_{IL} = 0V		0.1	10	µA
C_{IN}	Input Capacitance			3.5		pF
R_{IN}	Input Resistance			50		MΩ
Output						
R_{OVH}	ON Resistance VH to OUTH	I_{OUT} = -200 mA		3.4	5	Ω
R_{OVL}	ON Resistance VL to OUTL	I_{OUT} = +200 mA		4	6	Ω
I_{OUT}	Output Leakage Current	OE = 0V, OUTH = VL, OUTL = V_S+		0.1	10	µA
I_{PK}	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
I_{DC}	Continuous Output Current	Source/Sink	200			mA
Power Supply						
I_S	Power Supply Current	Inputs = V_S+		1	2.5	mA
I_{VH}	Off Leakage at VH	VH = 0V		4	10	µA
Switching Characteristics						
t_R	Rise Time	C_L =2000 pF		17		ns
t_F	Fall Time	C_L = 2000 pF		17		ns
$t_{RFdelta}$	t_R, t_F Mismatch	C_L = 2000 pF		0		ns
t_{D-1}	Turn-Off Delay Time	C_L = 2000 pF		11.5		ns
t_{D-2}	Turn-On Delay Time	C_L = 2000 pF		12		ns
t_{Ddelta}	t_{D-1}-t_{D-2} Mismatch	C_L = 2000 pF		0.5		ns
t_{D-3}	Tri-State Delay Enable			11		ns
t_{D-4}	Tri-State Delay Disable			11		ns

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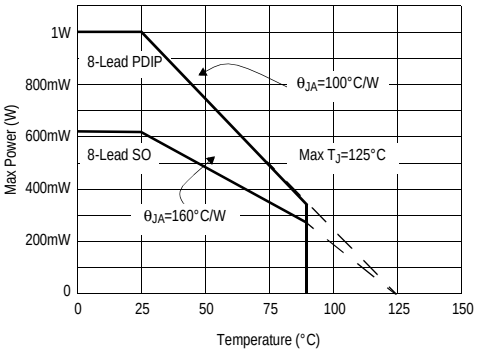
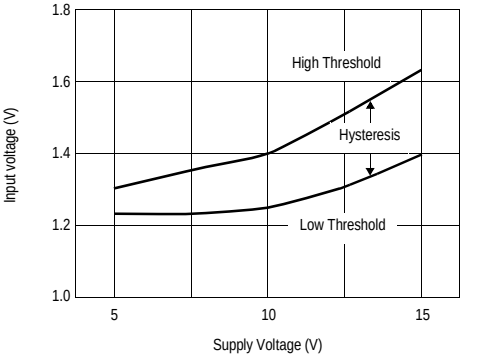
Typical Performance Curves

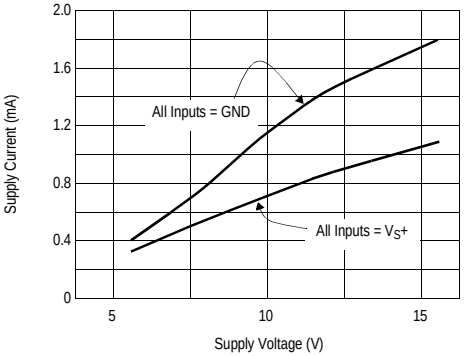
Max Power/Derating Curves



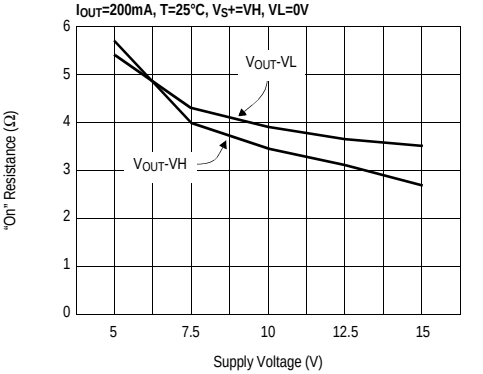
Input Threshold vs Supply Voltage
T=25°C



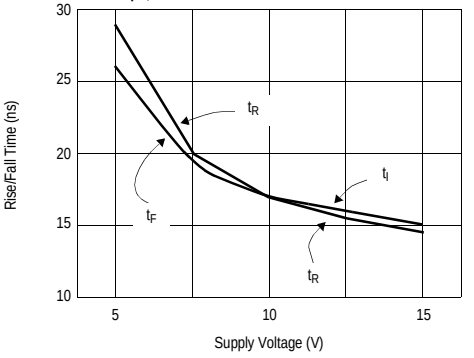
Quiescent Supply Current vs Supply Voltage
T=25°C



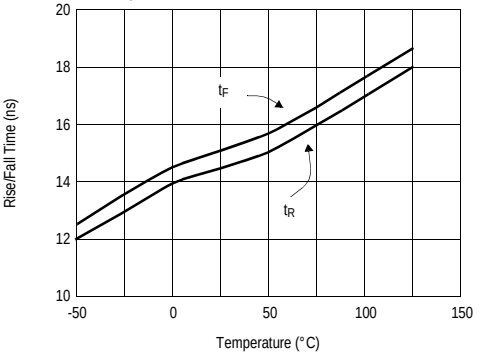
"On" Resistance vs Supply Voltage
I_{OUT}=200mA, T=25°C, V_S+=VH, VL=0V



Rise/Fall Time vs Supply Voltage
C_L=2000pF, T=25°C

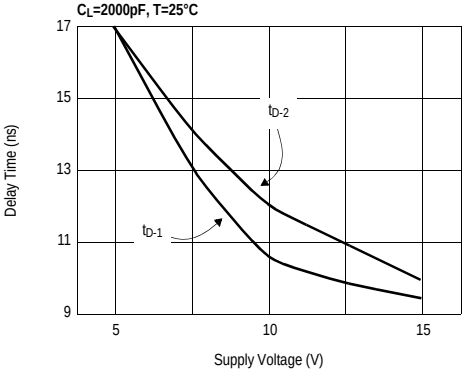


Rise/Fall Time vs Temperature
C_L=2000pF, V_S+=15V

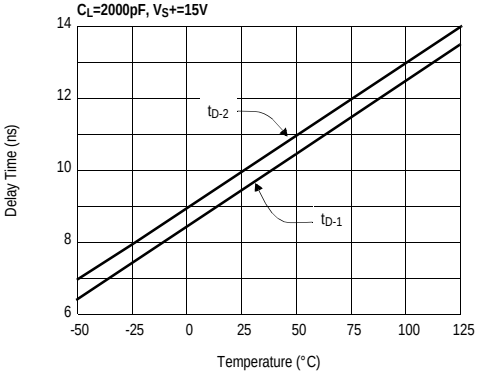


Typical Performance Curves (cont.)

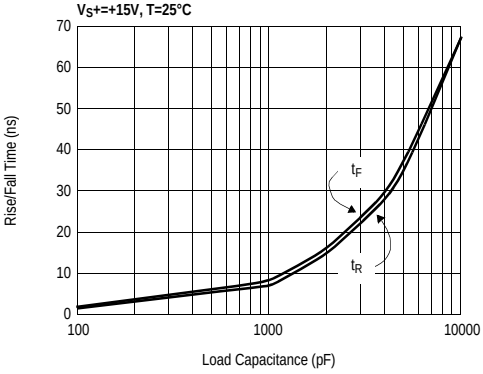
Propagation Delay vs Supply Voltage
C_L=2000pF, T=25°C



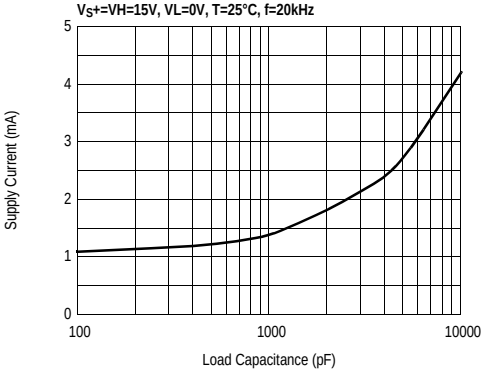
Propagation Delay vs Temperature
C_L=2000pF, V_S+=15V



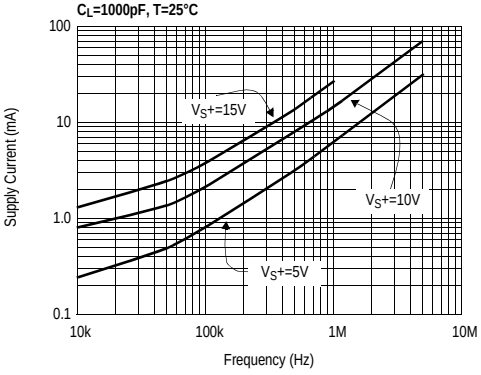
Rise/Fall Time vs Load Capacitance
V_S+=+15V, T=25°C



Supply Current vs Load Capacitance
V_S+=VH=15V, VL=0V, T=25°C, f=20kHz



Supply Current vs Frequency
C_L=1000pF, T=25°C



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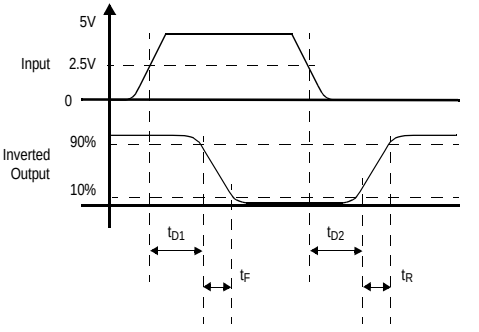
Truth Table

OE	IN	VH to OUTH	OUTL to VS-
0	0	Open	Open
0	1	Open	Open
1	0	Closed	Open
1	1	Open	Closed

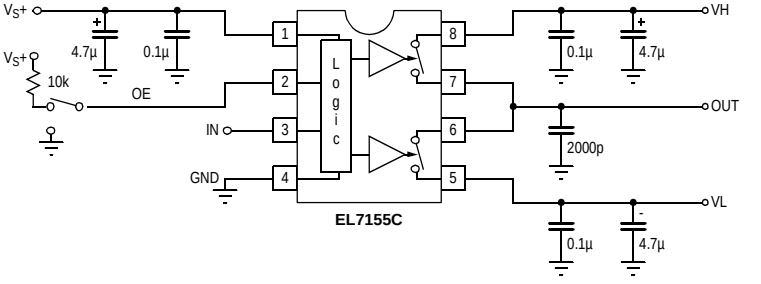
Operating Voltage Range

PIN	MIN	MAX
GND - VL	-5	0
V_S+ - VL	5	18
VH - VL	0	18
V_S+ - VH	0	18
V_S+ - GND	5	18

Timing Diagrams



Standard Test Configuration



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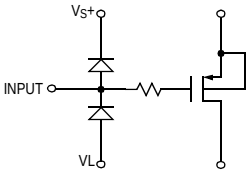
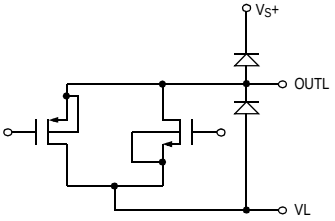
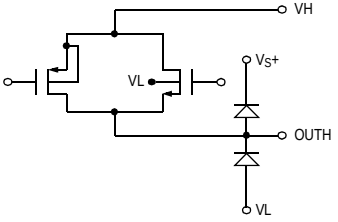
Pin Descriptions

Pin	Name	Function	Equivalent Circuit
1	V_S+	Positive Supply Voltage	
2	OE	Output Enable	 Circuit 1
3	IN	Input	Same as Circuit 1
4	GND	Ground	
5	VL	Negative Supply Voltage	
6	OUTL	Lower Switch Output	 Circuit 2
7	OUTH	Upper Switch Output	 Circuit 3
8	VH	Upper Output Voltage	

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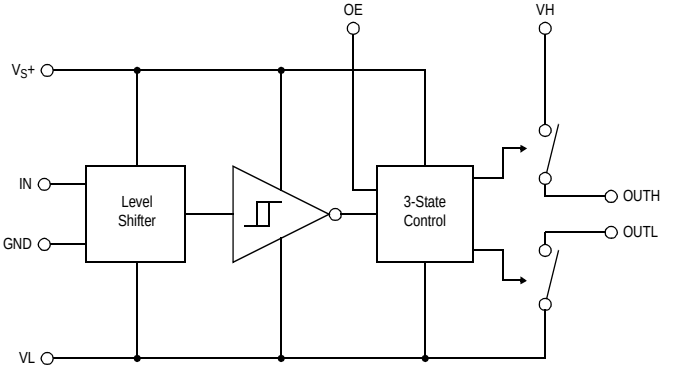
Block Diagram



Application Information

Product Description

The EL7155C is a high performance 40MHz pin driver. It contains two analog switches connecting VH to OUTH and VL to OUTL. Depending on the value of the IN pin, one of the two switches will be closed and the other switch open. An output enable (OE) is also supplied which opens both switches simultaneously.

Due to the topology of the EL7155C, VL should always be connected to a voltage equal to, or lower than GND. VH can be connected to any voltage between VL and the positive supply, V_S+.

The EL7155C is available in both the 8-pin SOIC and the 8-pin PDIP packages. The relevant package should be chosen depending on the calculated power dissipation.

Supply Voltage Range and Input Compatibility

The EL7155C is designed for operation on supplies from 5V to 15V (4.5V to 18V maximum). The table on page 6 shows the specifications for the relationship between the V_S+, VH, VL, and GND pins.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (V_S+) of 5V, the EL7155C is also compatible with TTL inputs.

Power Supply Bypassing

When using the EL7155C, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7155C necessitate the use of a bypass capacitor between the V_S+ and GND pins. It is recommended that a 2.2µF tantalum capacitor be used in parallel with a 0.1µF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the VH and VL pins have some level of bypassing, especially if the EL7155C is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL7155C drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below T_{jmax} (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

- V_S is the total power supply to the EL7155C (from V_S+ to GND),
- V_{out} is the swing on the output (VH - VL),
- C_L is the load capacitance,
- C_{INT} is the internal load capacitance (50pF max.),
- I_S is the quiescent supply current (3mA max.) and
- f is frequency

Having obtained the application's power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T_{jmax}:

$$\theta_{ja} = \frac{(T_{jmax} - T_{max})}{PD}$$

where:

- T_{jmax} is the maximum junction temperature (125°C),
- T_{max} is the maximum operating temperature,
- PD is the power dissipation calculated above,
- θ_{ja} thermal resistance on junction to ambient.

θ_{ja} is 160°C/W for the SO8 package and 100°C/W for the PDIP8 package when using a standard JEDEC JESD51-3 single-layer test board. If T_{jmax} is greater than 125°C when calculated using the equation above, then one of the following actions must be taken:

- Reduce θ_{ja} the system by designing more heat-sinking into the PCB (as compared to the standard JEDEC JESD51-3)
- Use the PDIP8 instead of the SO8 package
- De-rate the application either by reducing the switching frequency, the capacitive load, or the maximum operating (ambient) temperature (T_{max})

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General Disclaimer

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