EL2004/EL2004C
350 MHz FET Buffer

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Features

- Slew rate—2500 V/μs
- Rise time—1 ns
- Bandwidth—350 MHz
- ELH0033—pin compatible
- ±5 to ±15V operation
- 100 mA output current
- MIL-STD-883B Rev. C devices manufactured in U.S.A.

Applications

- Coaxial cable driver
- Fast op amp booster
- Flash converter driver
- Video line driver
- High-speed sample and hold
- Pulse transformer driver
- A.T.E. pin driver

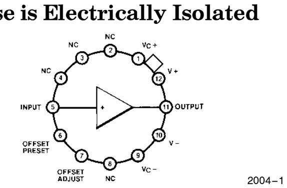
Ordering Information

Part No.	Temp. Range	Package	Outline#
EL2004CG	−25°C to +85°C	TO-8	MDP0002
EL2004G	−55°C to +125°C	TO-8	MDP0002
EL2004L	−55°C to +125°C	52-Pad LCC	MDP0013
EL2004L/MIL	−55°C to +125°C	52-Pad LCC	MDP0013

5962-89659 is the SMD version of this device.

Connection Diagram

Case is Electrically Isolated



Top View

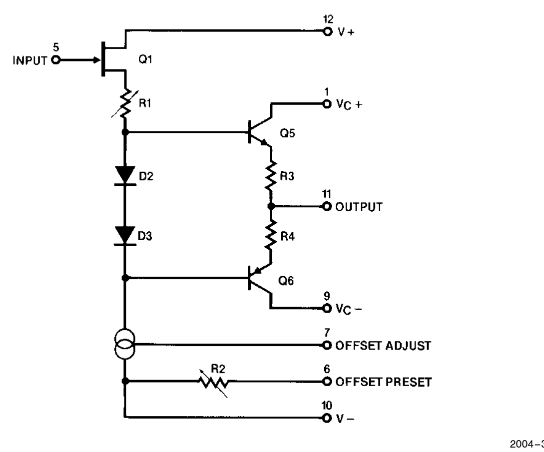
General Description

The EL2004 is a very high-speed, FET input buffer/line driver designed for unity gain applications at both high current (up to 100 mA) and at frequencies up to 350 MHz. The 2500 V/μs slew rate and wide bandwidth ensures the stability of the circuit when the EL2004 is used inside op amp feedback loops.

Applications for the EL2004 include line drivers, video buffers, wideband instrumentation, and high-speed drivers for inductive and capacitive loads. The performance of the EL2004 makes it an ideal buffer for video applications including input buffers for flash A/D converters, and output buffers for video DACs. Its excellent phase linearity is particularly advantageous in digital signal processing applications.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2004	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2004C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

±15V DC Electrical Characteristics

V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$, V_{IN} = 0V, R_L = 1 kΩ unless otherwise specified (Note 1)

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le$ 100 kΩ, T_J = 25°C		5	10	I		12	20	I	mV
		$R_S \le$ 100 kΩ			15	I			25	III	mV
A_V	Voltage Gain	V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_L = 100Ω, V_{IN} = ±10V	0.92	0.95	0.98	I	0.90	0.95	0.98	II	V/V
R_{IN}	Input Impedance	T_J = 25°C, V_{IN} = ±1V	10^8	10^{11}		I	10^8	10^{11}		I	Ω
R_{OUT}	Output Impedance	V_{IN} = ±1 V_{DC}, ΔR_L = 100Ω to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±14V	±12	±13		I	±12	±13		II	V
		V_{IN} = ±10.5V, R_L = 100Ω T_A = 25°C	±9	±9.8		I	±9	±9.8		I	V
I_{IN}	Input Current	T_J = 25°C (Note 2)			0.25	I			2.0	I	nA
		T_A = 25°C (Note 3)			2.5	IV			20	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			50	III	nA
		V_{IN} = −10V		20		V		20		V	nA
I_S	Supply Current			20	24	I		20	24	II	mA

TD is 3.2in

$\pm$5V DC Electrical Characteristics

$V_S = \pm 5V$, $T_{MIN} < T_A < T_{MAX}$, $V_{IN} = 0V$, $R_L = 50\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \leq 100\ k\Omega$, $T_J = 25°C$		10	30	I		10	30	I	mV
		$R_S \leq 100\ k\Omega$			35	I			35	III	mV
A_V	Voltage Gain	$V_{IN} = \pm 1V$, $R_L = 1\ k\Omega$	0.90	0.95	1.0	I	0.90	0.95	1.0	II	V/V
		$V_{IN} = \pm 1V$	0.80	0.88	0.95	I	0.80	0.88	0.95	II	V/V
R_{IN}	Input Impedance	$T_J = 25°C$, $V_{IN} = \pm 1V$	10^8	10^{11}		I	10^{10}	10^{11}		I	Ω
R_{OUT}	Output Impedance	$V_{IN} = \pm 1\ V_{DC}$, $\Delta R_L = 50\Omega$ to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	$V_{IN} = \pm 4V$	$\pm$2.0	$\pm$2.9		I	$\pm$2.0	$\pm$2.9		III	V
I_{IN}	Input Current	$T_J = 25°C$ (Note 2)			250	I			500	I	pA
		$T_A = 25°C$ (Note 3)			2.5	IV			5	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			20	III	nA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$, $R_L = 1\ k\Omega$		60		V		60		V	dB
I_S	Supply Current	$R_L = 1\ k\Omega$		17.5	20	I		17.5	20	II	mA

Note 1: When operating at elevated temperatures the power dissipation of the EL2004 must be limited to the values shown in the typical performance curve "Maximum Power Dissipation vs Temperature". Junction to case thermal resistance is 31°C/W when dissipation is spread among the transistors in a normal AC steady-state condition. In special conditions where heat is concentrated in one output device, junction temperature should be calculated using a thermal resistance of 70°C/W.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J = 25°C$. When supply voltages are $\pm 15V$, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_{IN} will change significantly during warm-up. Refer to I_{IN} vs Temperature graph for expected values.

Note 3: Measured in still air seven minutes after application of power. See graph of Input Current During Warm-up for further information.

Note 4: Bandwidth is calculated from the rise time. The EL2004 has a single pole gain and phase response up to the -3 dB frequency.

Note 5: Slew rate is measured between $V_{OUT} = +2.5V$ and $-2.5V$ for this test.

Note 6: Slew rate is measured between $V_{OUT} = +1V$ and $-1V$ for this test. Pulse repetition rate is $<$50 MHz.

$\pm$15V AC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 1\ k\Omega$, $R_S = 50\Omega$, $T_J = 25°C$ unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	(Note 4)	200	350		I	200	350		I	MHz
		$R_L = 50\Omega$	140	200		I	140	200		I	MHz
t_s	Settling Time to 1%	$\Delta V_{IN} = 1V$, $t_r = 3$ ns		6		V		6		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF

TD is 3.2in

TD is 1.3in

±15V AC Electrical Characteristics

V_S = ±15V, R_L = 1 kΩ, R_S = 50Ω, T_J = 25°C unless otherwise specified — Contd.

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	V_{IN} = ±5V (Note 5)	2000	2500		I	2000	2500		I	V/µs
		C_L = 100 pF, V_{IN} = ±5V (Note 5)		1200		V		1200		V	V/µs
t_r	Rise Time Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	1.7	I		1.0	1.7	I	ns
		ΔV_{IN} ∿ 0.6V, R_L = 50Ω		1.7	2.5	I		1.7	2.5	I	ns
t_p	Propagation Delay Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	2.0	I		1.0	2.0	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S− = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB

±5V AC Electrical Characteristics

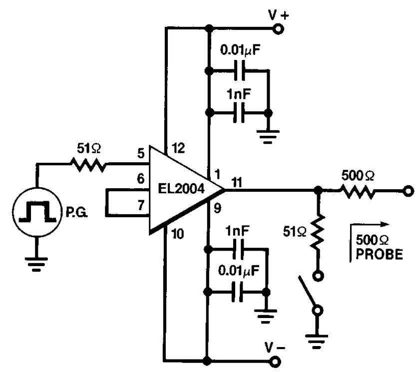
V_S = ±5V, R_L = 50Ω, R_S = 50Ω, T_J = 25°C unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	R_L = 1 kΩ	175	220		I	175	220		I	MHz
		(Note 4)	125	150		IV	125	150		IV	MHz
t_s	Settling Time to 1%	ΔV_{IN} = 1V, t_r = 3 ns		8		V		8		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF
SR	Slew Rate	V_{IN} = ±2V (Note 6)	900	1200		I	900	1200		I	V/µs
		C_L = 100 pF, V_{IN} = ±2V R_L = 1 kΩ (Note 6)		500		V		500		V	V/µs
t_r	Rise Time Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.6	2.0	I		1.6	2.0	I	ns
		R_L = 50Ω, ΔV_{IN} ∿ 0.6V		2.3	2.8	IV		2.3	2.8	IV	ns
t_p	Propagation Delay Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.2	2.4	I		1.2	2.4	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S− = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB

TD is 2.7in

TD is 3.4in

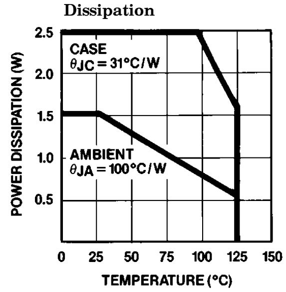
AC Test Circuit



2004–4

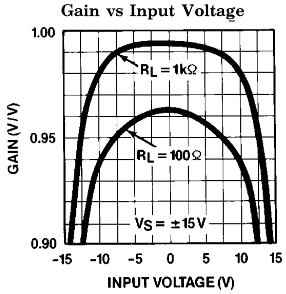
Typical Performance Curves

TO-8
Maximum Power
Dissipation

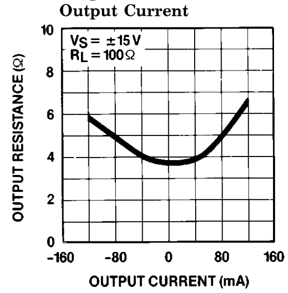


2004–5

Gain vs Input Voltage



Output Resistance vs
Output Current



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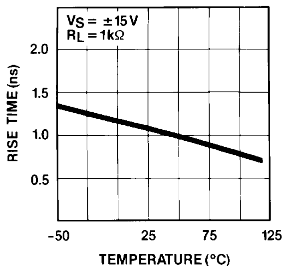
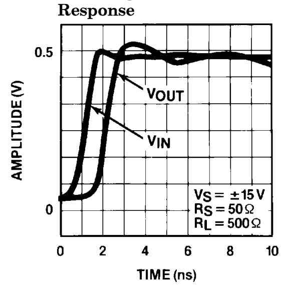
Typical Performance Curves — Contd.

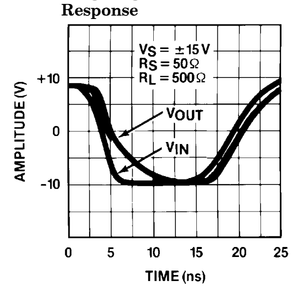
Rise Time vs Temperature



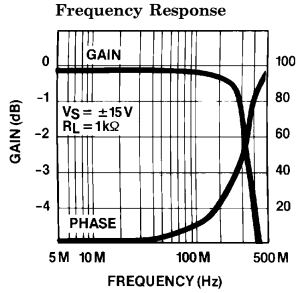
Small Signal Pulse Response



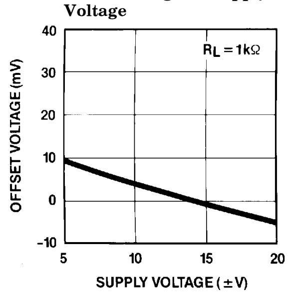
Large Signal Pulse Response



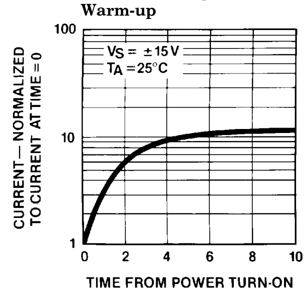
Frequency Response



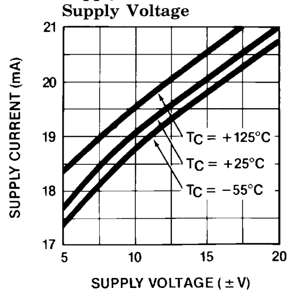
Offset Voltage vs Supply Voltage



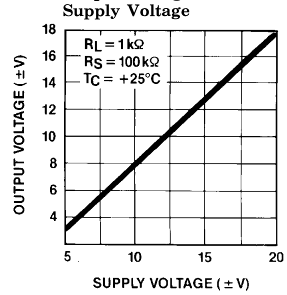
Normalized Input Bias Current During Warm-up



Supply Current vs Supply Voltage



Output Voltage vs Supply Voltage



2004–8

Applications Information

The EL2004 is one member of a family of high performance buffers manufactured by Elantec. The 2004 is optimized for speed while others offer choices of input DC parameters or output drive or cost. The following table illustrates those members available at the time of this printing. Consult the factory for the latest capabilities in this developing line.

Elantec's Buffer Family

Part #	Slew Rate V/μs	Bandwidth MHz	Input Current (Warm)	Peak I_{OUT} mA	Rise Time ns
ELH0002	200	50	6 μA	400	7
ELH0033	1500	100	2.5 nA	250	2.9
EL2004	2500	350	2.5 nA	250	1.0
EL2005	1500	140	0.1 nA	250	2.5

Recommended Layout Precautions

The very high-speed performance of the EL2004 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.1 μF or more should be connected with the shortest practical lead lengths between the device supply leads and a ground plane. In addition, it can be helpful to parallel these with 4.7 μF electrolytics (Tantalum preferred). Failure to follow these precautions can result in oscillation.

Circuit Operation

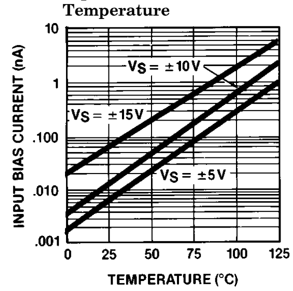
The EL2004 is effectively an ideal unity gain amplifier with almost infinite input impedance and about 6Ω output impedance.

Input Characteristics

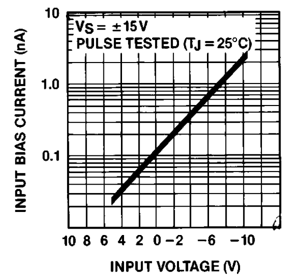
The input impedance of a junction FET is a strong function of temperature and input voltage. Nominal input resistance of EL2004 is 10^{12} at 25°C junction, but as I_B doubles every 11°C in the JFET, the input resistance falls. During warm-up, self-heating raises the junction temperature up to 60°C or more (without heatsink) so operating I_B will be much higher than the data sheet 25°C specification.

Another factor which can increase bias current is input voltage. If the input voltage is more than 20V below the positive supply, the input current rises exponentially. (See Curve.)

Input Bias Current vs Temperature



Input Bias Current vs Input Voltage



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In applications such as sample and hold circuits where it is important to maintain low input bias current over input voltage range, the EL2005 High Accuracy Fast Buffer is recommended.

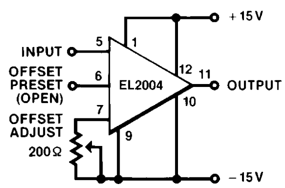
The input capacitance of EL2004 comprises the FET device gate-to-source capacitance (which is a function of input voltage) and stray capacitance to the case. Effective input capacitance can be minimized by connecting the case to the output since it is electrically isolated. Or, for reduced radiation, the case may be grounded. The AC characteristics specified in this data sheet were obtained with the case floating.

Offset Voltage Adjustment

The EL2004's offset voltages have been actively laser trimmed at ±15V supplies to meet specified limits when the offset adjust pin is shorted to the offset preset pin. If external offset null is required, the offset adjust pin should be connected to a 200Ω trim pot connected to the negative supply.

Circuit Operation — Contd.

Offset Zero Adjust



2004-10

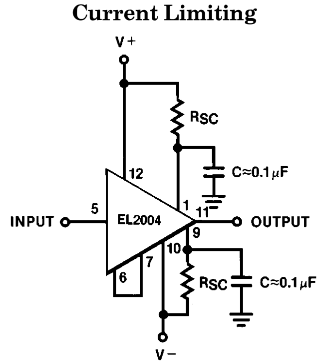
Capacitive Loading

The EL2004 is designed to drive capacitive loads up to several thousand picofarads without oscillation. However, peak current resulting from charging currents on fast edges should be limited below the absolute maximum peak current rating of 250 mA. In some cases it may be necessary to employ one of the current limit schemes shown below.

Short Circuit Protection

Dynamic response of the EL2004 was preserved by excluding current limit circuits which are not needed in most applications. However, in situations where operating conditions are not controlled, short circuit protection can be added by inserting resistors between the output device collectors and supplies as illustrated.

Using Resistor Current Limiting



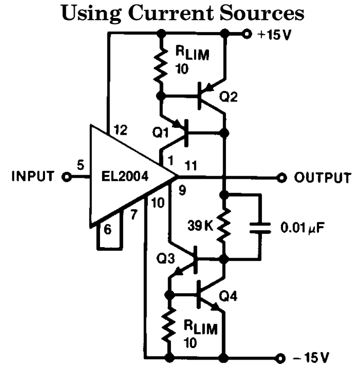
2004-11

Suitable resistor values can be calculated as follows:

$$R_{SC} = \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where $I_{SC} \leq 100$ mA for EL2004.

Current Limiting Using Current Sources



2004-12

The inclusion of limiting resistors in the collectors of the output devices will reduce the output voltage swing and speed. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses.

An alternate active current limit technique that retains full DC output swing is shown above. Here the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as the current source reaches its limit.

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6\text{V}}{100\text{ mA}} = 6\Omega$$

Power Supplies

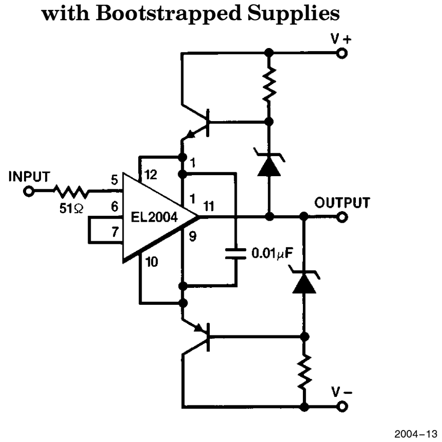
The EL2004 has been characterized for both ±15 and ±5V dual supply operation, but other combinations can also be useful. For example, in many video applications it is only necessary for the output to swing ±2V or less, but speed and distortion are important. In this situation, the input stage can be operated at the full ±15V supply while the output collectors are returned to ±5V. The speed and distortion will be almost as good as if the whole circuit was operating at ±15V, but the dissipation is substantially reduced and higher load currents can be safely accommodated.

Circuit Operation — Contd.

Increasing Operating Voltage and Reducing Thermal Tail

When driving heavy loads, the changing dissipation in the output transistors can sometimes cause temperature gradients in the circuit which cause a shift in offset voltage and the phenomenon known as "thermal tail". Bootstrapping the output as illustrated substantially reduces the power in the output transistors and mitigates the effect.

High Voltage Inputs can be Accommodated with Bootstrapped Supplies



Hardware

In order to utilize the full drive capabilities of the EL2004, it should be mounted with a heatsink, particularly for extended temperature operation. Suitable heatsinks include Thermalloy 2240A (33°C/W), Wakefield 215CB (30°C/W) and IERC-UP-TO-848CB (15°C/W).

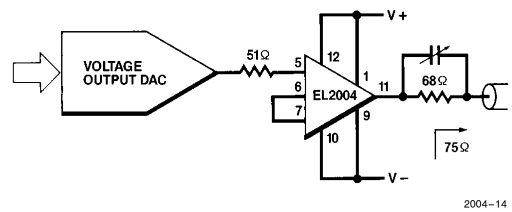
The case is isolated from the circuit and may be connected to system chassis. Sockets are not recommended as they add substantial inductance and capacitance which impair the performance of the device. However, for test purposes they are unavoidable and precautions such as shielding input from output are suggested.

General Application Suggestions

Video DAC Buffer

Many of the available video D to A converters are unable to directly drive 50Ω or 75Ω cables. The EL2004's excellent phase linearity at video frequencies make it an ideal solution. In critical applications or where line termination is not controlled, a matching pad should be used as shown. The capacitor should be adjusted for optimum pulse response. If properly layed out this circuit will not overshoot.

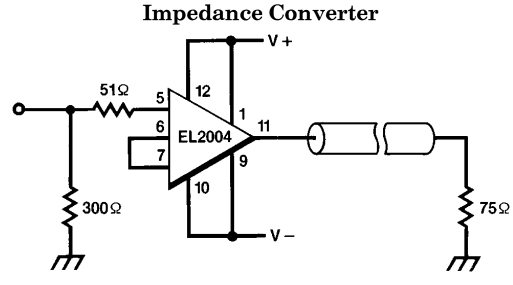
Video DAC Buffer



Impedance Matching

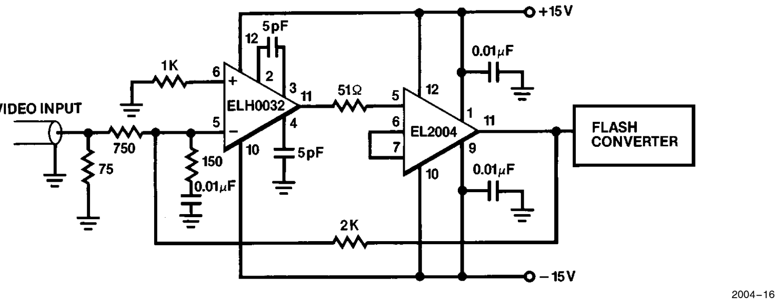
The EL2004 provides power gain and isolation between source and load when used as an active tap or impedance matching device as illustrated here. In this example, there is no output matching pad between the 2004 and the 75Ω line. Such matching is not needed when the distant end of the cable is properly terminated as there is no reflected signal to worry about and the 2004 isolates the source. This technique allows the full output voltage of the EL2004 to be applied to the load.

Impedance Converter



General Application Suggestions — Contd.

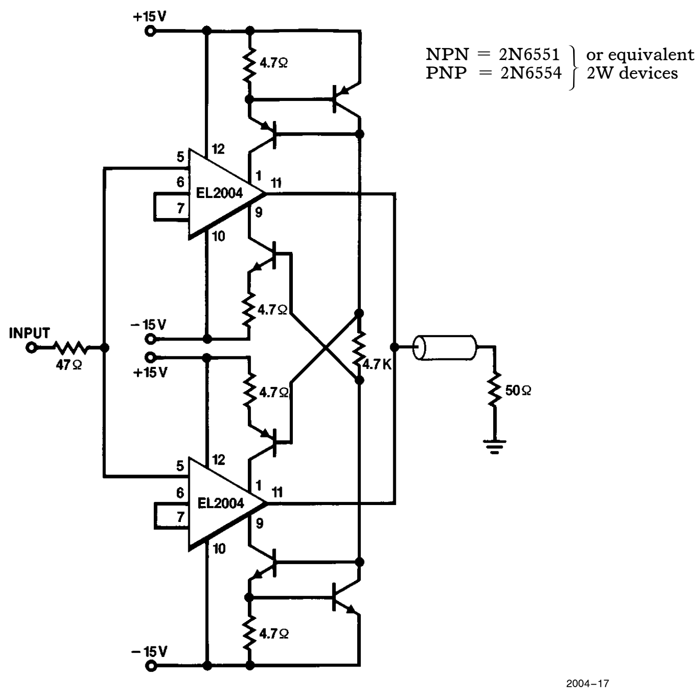
Inverting Amplifier for 20 MHz Flash Converter



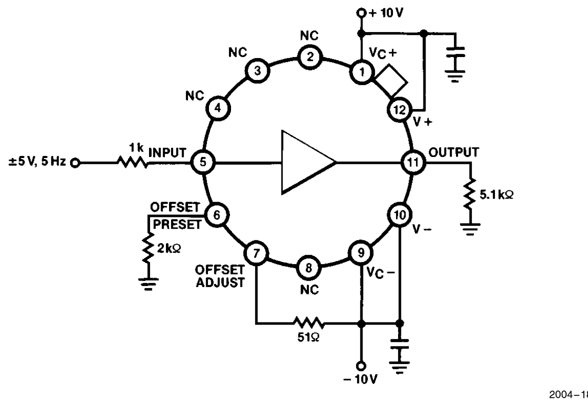
Boosting the Output

Unlike most integrated cicuits, two or more EL2004's can be paralleled for increased output drive. This capability results from the finite output resistance and low output mismatch of the EL2004. For example, a 50Ω cable driver with ±10V capability can be made by using two EL2004's. A short-circuit protected version is shown below.

50Ω Cable Driver with Short Circuit Protection



Burn-In Circuit



Pin numbers are for TO-8 package.
LCC uses the same schematic.

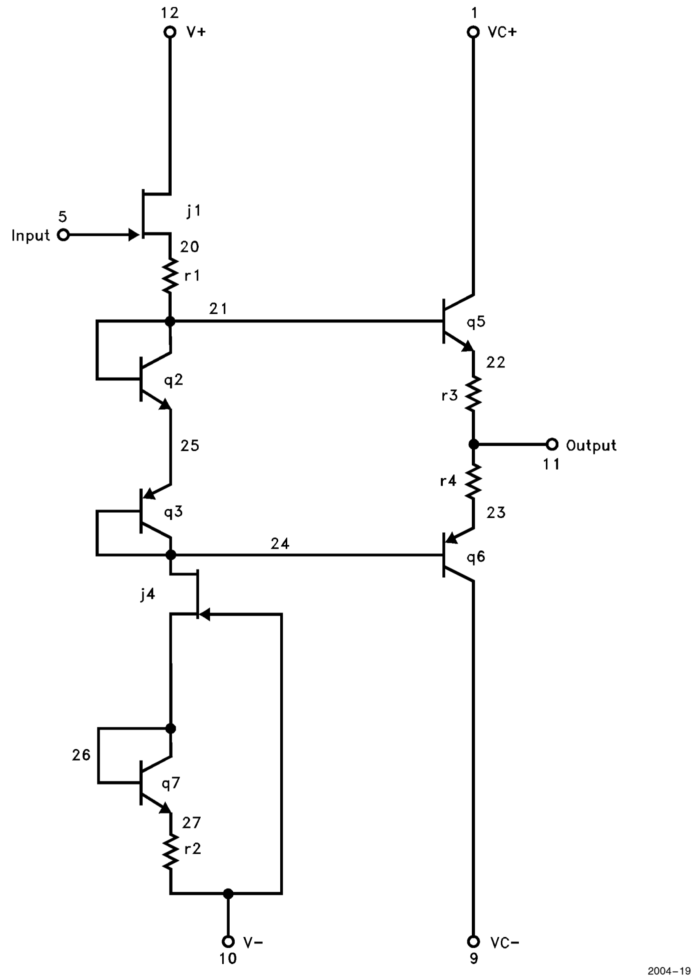
EL2004 Macromodel

```
* Connections:  input
*               |     V+
*               |     |     Vc+
*               |     |     |     V-
*               |     |     |     |     Vc-
*               |     |     |     |     |     output
*               |     |     |     |     |     |
.subckt M2004   5     12    1     10    9     11
* Models
.model qn npn (is=5e-14 bf=150 vaf=100 rc=1 rb=5 re=1 ikf=200mA
+cje=5pF cjc=5pF mje=.42 mjc=.23 tf=.3nS tr=200nS br=5 vtf=0)
.model qp pnp (is=5e-14 bf=150 vaf=100 rc=2 rb=3 re=1 ikf=100mA
+cje=5.7pF cjc=4pF tf=.3nS mje=.32 mjc=.43 tr=170nS br=5 vtf=0)
.model qf njf (vto=-3V beta=4.0e-3 cgd=4pF cgs=10pF lambda=671.0e-6)
* Resistors
r1 20 21 58.33
r2 27 10 58.33
r3 22 11 2
r4 11 23 2
* Transistors
j1 12 5 20 qf
j4 24 10 26 qf
q2 21 21 25 qn
q3 24 24 25 qp
q5 1 21 22 qn
q6 9 24 23 qp
q7 26 26 27 qn
.ends
```

TAB WIDE

TD is 3.8in

EL2004 Macromodel — Contd.



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EL2004/EL2004C

350 MHz FET Buffer

General Disclaimer

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