

EL7412C

High Speed, Four Channel Power MOSFET Drivers

EL7412C

Features

- Excellent response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Full bridge drivers
- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

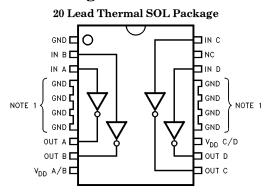
Ordering Information

Part No. Temp. Range Outline # Pkg. EL7412CM -40°C to +85°C MDP0027 20 Lead Thermal SOL Manufactured under U.S. Patent Nos. 5,334,883, #5,331,047

General Description

The EL7412C contains (4) high performance matched drivers. These very high speed drivers are capable of delivering peak currents of 2.0 amps into highly capacitive loads and are ideally suited for "Full bridge" and ultrasound applications. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. The matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.





Note 1: Pins 4-7 and 14-17 are electrically connected.



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Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication: however, this data sheet cannot be a "controlled document". Current revisions, if any, to these pecifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation

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Absolute Maximum Ratings

Supply (V+ to Gnd) Input Pins – Combined Peak Output Current Storage Temperature Range Ambient Operating Temperature

16.5V -0.3V to +0.3V above V⁺ 8A -65°C to +150°C -40°C to +85°C Operating Junction Temperature Power Dissipation 20-Pin "Batwing" SOIC 125°C

1500 mW

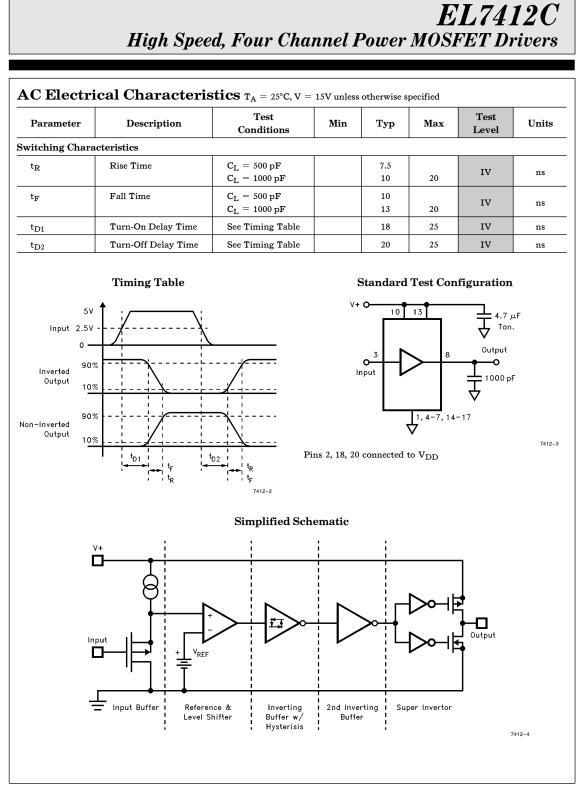
Important Note:

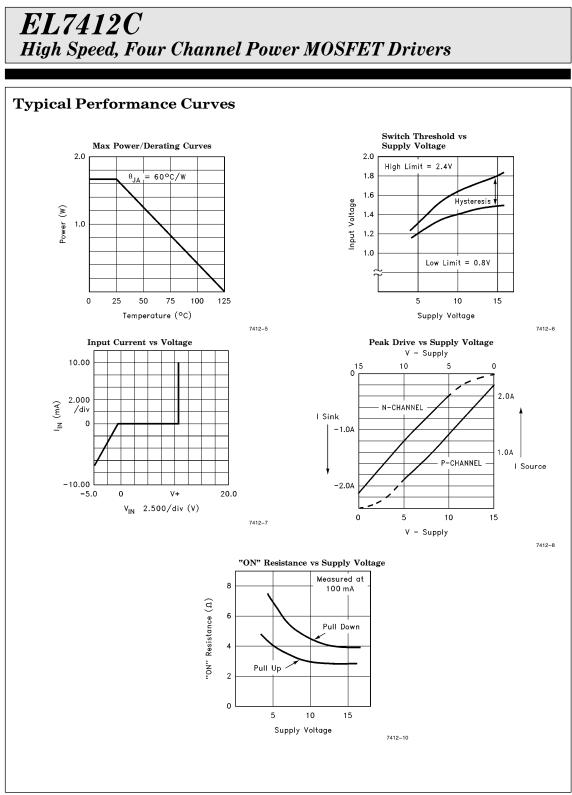
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

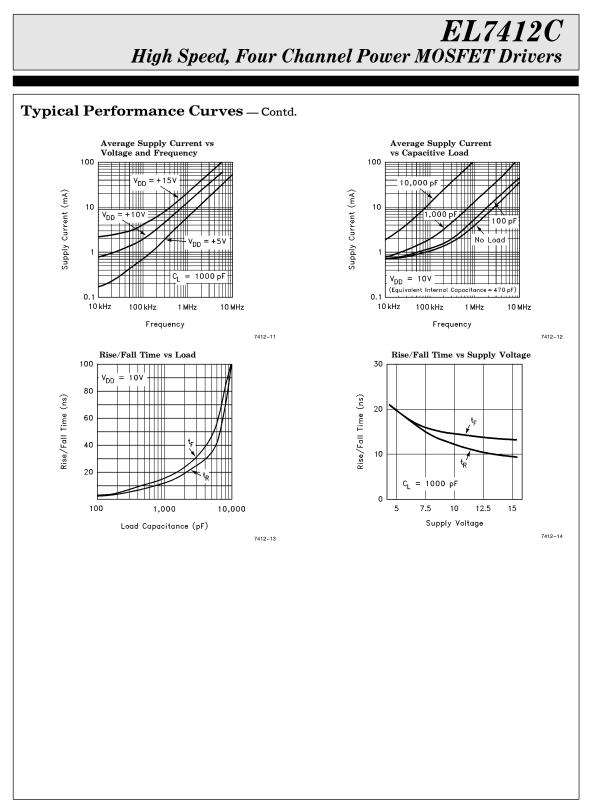
Test Level	Test Procedure
Ι	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_{\rm A}=25^{\circ}{\rm C}$ and QA sample tested at $T_{\rm A}=25^{\circ}{\rm C}$,
	T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
v	Parameter is typical value at $T_A = 25^{\circ}$ C for information purposes only.

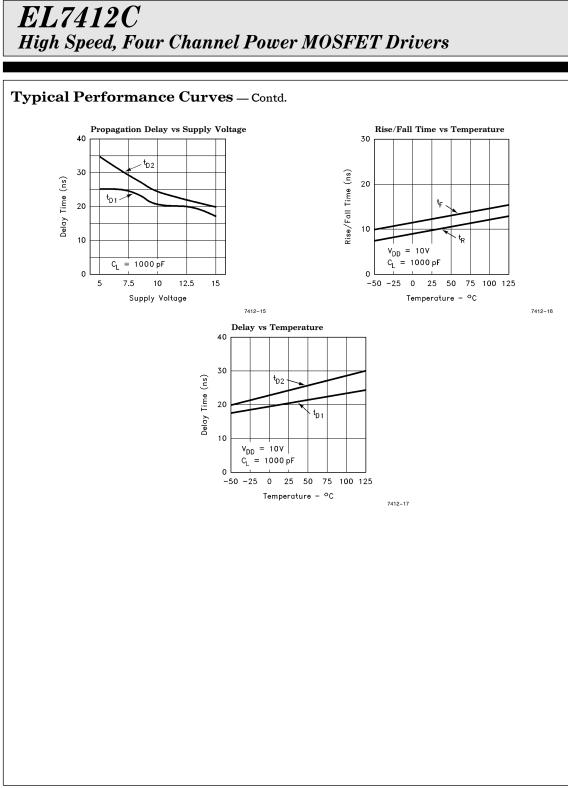
DC Electrical Characteristics $T_A = 25^{\circ}$ C, $V_{DD} = 15$ V unless otherwise specified

Parameter	Description	Test Conditions	Min	Тур	Max	Test Level	Units
Input							
VIH	Logic "1" Input Voltage		2.4			I	v
I _{IH}	Logic "1" Input Current	@V _{DD}		0.1	10	I	μΑ
V _{IL}	Logic "0" Input Voltage				0.8	I	v
I _{IL}	Logic "0" Input Current	@0V		0.1	10	I	μΑ
V _{HVS}	Input Hysteresis			0.3		v	v
Output							
R _{OH}	Pull-Up Resistance	$I_{OUT} = -100 \text{ mA}$		3	6	I	Ω
R _{OL}	Pull-Down Resistance	$I_{OUT} = +100 \text{ mA}$		4	6	I	Ω
I _{PK}	Peak Output Current	Source Sink		2 2		IV	А
I _{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply	•	•					
IS	Power Supply Current	Inputs High		2	5	I	mA
Vs	Operating Voltage		4.5		15	I	v









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General Disclaimer

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