DATA SHEET

ELPIDA

MOS INTEGRATED CIRCUIT

MC-4R128FKE6D

Direct Rambus DRAM RIMM™ Module
128M-BYTE (64M-WORD x 16-BIT)

Description

The Direct Rambus RIMM module is a general-purpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

MC-4R128FKE6D modules consists of four 288M Direct Rambus DRAM (Direct RDRAM) devices (μPD488588). These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz, 711MHz or 800MHz transfer rates while using conventional system and board design technologies.

Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per sixteen bytes).

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95 % bus efficiency. The Direct RDRAM's 32 banks support up to four simultaneous transactions per device.

Features

- 184 edge connector pads with 1mm pad spacing
- 128 MB Direct RDRAM storage
- Each RDRAM® has 32 banks, for 128 banks total on module
- Gold plated contacts
- RDRAMs use Chip Scale Package (CSP)
- Serial Presence Detect support
- Operates from a 2.5 V supply
- Powerdown self refresh modes
- Separate Row and Column buses for higher efficiency
- Over Drive Factor (ODF) support

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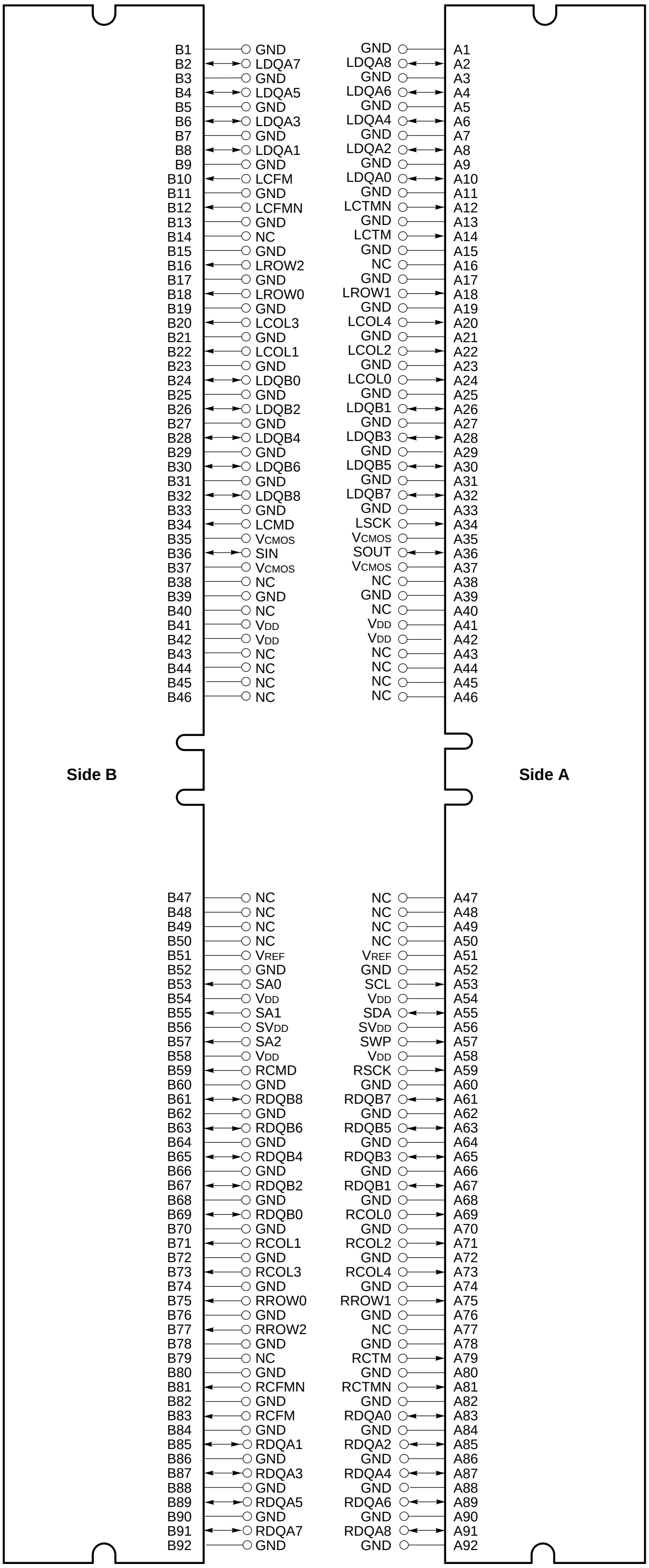
Order information

Part number	Organization	I/O Freq. MHz	RAS access time ns	Package	Mounted devices
MC-4R128FKE6D - 845	64M x 16	800	45	184 edge connector pads RIMM	4 pieces of
MC-4R128FKE6D - 745		711	45	with heat spreader	μPD488588FF
MC-4R128FKE6D - 653		600	53	Edge connector : Gold plated	FBGA (μBGA®) package

Module Pad Configuration



LCFM, LCFMN,
RCFM, RCFMN : Clock from master
LCTM, LCTMN,
RCTM, RCTMN : Clock to master
LCMD, RCMD : Serial Command Pad
LROW2 - LROW0,
RROW2 - RROW0 : Row bus
LCOL4 - LCOL0,
RCOL4 - RCOL0 : Column bus
LDQA8 - LDQA0,
RDQA8 - RDQA0 : Data bus A
LDQB8 - LDQB0,
RDQB8 - RDQB0 : Data bus B
LSCK, RSCK : Clock input
SA0 - SA2 : Serial Presence Detect Address
SCL, SDA : Serial Presence Detect Clock
SIN, SOUT : Serial I/O
SVDD : SPD Voltage
SWP : Serial Presence Detect Write Protect
VCMOS : Supply voltage for serial pads
VDD : Supply voltage
VREF : Logic threshold
GND : Ground reference
NC : These pads are not connected

Module Pad Names

Pad	Signal Name	Pad	Signal Name
A1	GND	B1	GND
A2	LDQA8	B2	LDQA7
A3	GND	B3	GND
A4	LDQA6	B4	LDQA5
A5	GND	B5	GND
A6	LDQA4	B6	LDQA3
A7	GND	B7	GND
A8	LDQA2	B8	LDQA1
A9	GND	B9	GND
A10	LDQA0	B10	LCFM
A11	GND	B11	GND
A12	LCTMN	B12	LCFMN
A13	GND	B13	GND
A14	LCTM	B14	NC
A15	GND	B15	GND
A16	NC	B16	LROW2
A17	GND	B17	GND
A18	LROW1	B18	LROW0
A19	GND	B19	GND
A20	LCOL4	B20	LCOL3
A21	GND	B21	GND
A22	LCOL2	B22	LCOL1
A23	GND	B23	GND
A24	LCOL0	B24	LDQB0
A25	GND	B25	GND
A26	LDQB1	B26	LDQB2
A27	GND	B27	GND
A28	LDQB3	B28	LDQB4
A29	GND	B29	GND
A30	LDQB5	B30	LDQB6
A31	GND	B31	GND
A32	LDQB7	B32	LDQB8
A33	GND	B33	GND
A34	LSCK	B34	LCMD
A35	V_{CMOS}	B35	V_{CMOS}
A36	SOUT	B36	SIN
A37	V_{CMOS}	B37	V_{CMOS}
A38	NC	B38	NC
A39	GND	B39	GND
A40	NC	B40	NC
A41	V_{DD}	B41	V_{DD}
A42	V_{DD}	B42	V_{DD}
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

Pad	Signal Name	Pad	Signal Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	V_{REF}	B51	V_{REF}
A52	GND	B52	GND
A53	SCL	B53	SA0
A54	V_{DD}	B54	V_{DD}
A55	SDA	B55	SA1
A56	SV_{DD}	B56	SV_{DD}
A57	SWP	B57	SA2
A58	V_{DD}	B58	V_{DD}
A59	RSCK	B59	RCMD
A60	GND	B60	GND
A61	RDQB7	B61	RDQB8
A62	GND	B62	GND
A63	RDQB5	B63	RDQB6
A64	GND	B64	GND
A65	RDQB3	B65	RDQB4
A66	GND	B66	GND
A67	RDQB1	B67	RDQB2
A68	GND	B68	GND
A69	RCOL0	B69	RDQB0
A70	GND	B70	GND
A71	RCOL2	B71	RCOL1
A72	GND	B72	GND
A73	RCOL4	B73	RCOL3
A74	GND	B74	GND
A75	RROW1	B75	RROW0
A76	GND	B76	GND
A77	NC	B77	RROW2
A78	GND	B78	GND
A79	RCTM	B79	NC
A80	GND	B80	GND
A81	RCTMN	B81	RCFMN
A82	GND	B82	GND
A83	RDQA0	B83	RCFM
A84	GND	B84	GND
A85	RDQA2	B85	RDQA1
A86	GND	B86	GND
A87	RDQA4	B87	RDQA3
A88	GND	B88	GND
A89	RDQA6	B89	RDQA5
A90	GND	B90	GND
A91	RDQA8	B91	RDQA7
A92	GND	B92	GND

Module Connector Pad Description

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Signal	I/O	Type	Description
GND	–	–	Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	I	VCMOS	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4..LCOL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8..LDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices.
LDQB8..LDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2..LROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	I	VCMOS	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC	–	–	These pads are not connected. These 24 connector pads are reserved for future use.
RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
RCMD	I	VCMOS	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4..RCOL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8..RDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8..RDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2..RROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.

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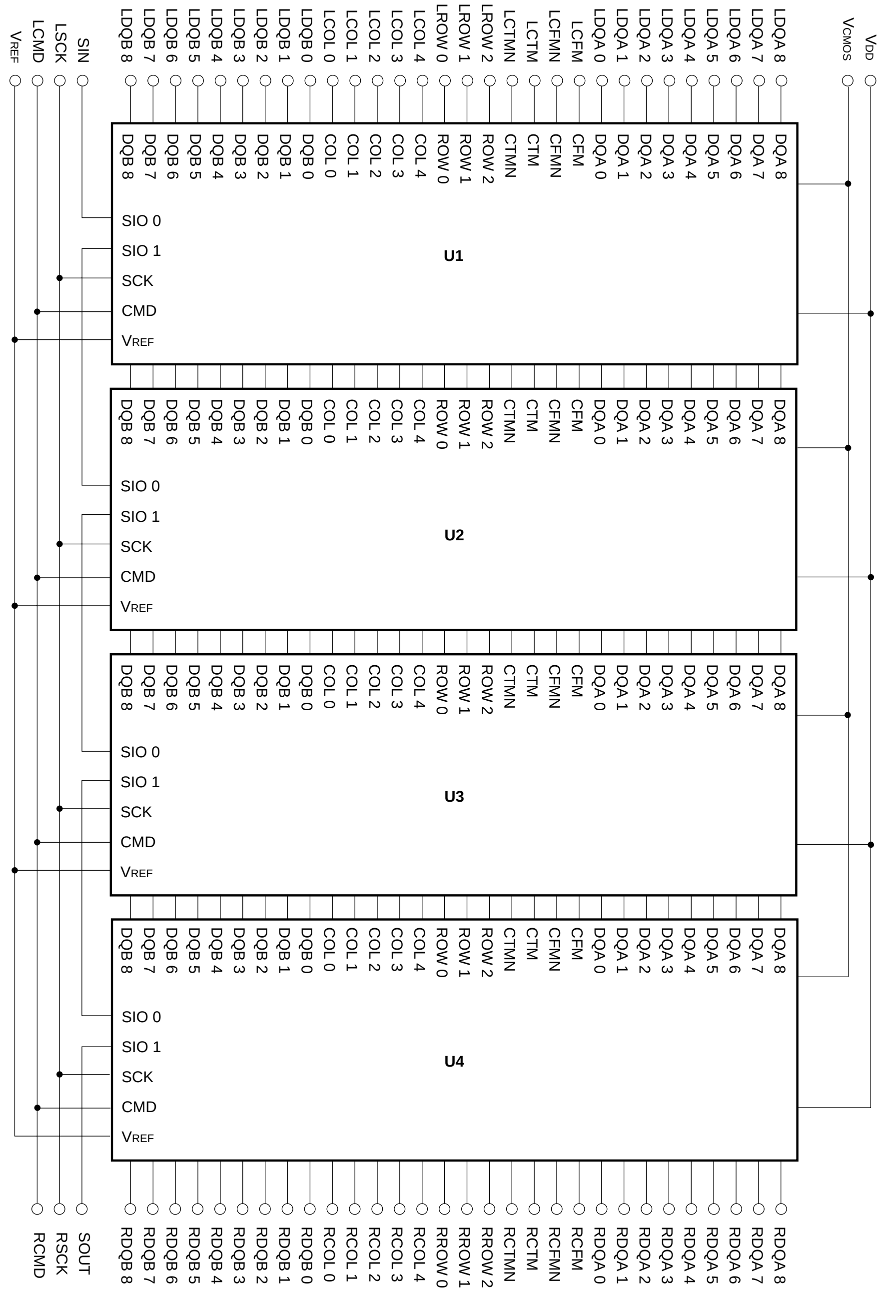
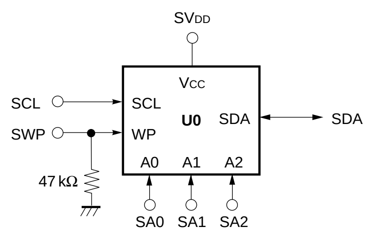
Signal	I/O	Type	Description
RSCK	I	V_{CMOS}	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	I	SV_{DD}	Serial Presence Detect Clock.
SDA	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	—	—	SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.
SWP	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	—	—	CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
V_{DD}	—	—	Supply voltage for the RDRAM core and interface logic.
V_{REF}	—	—	Logic threshold reference voltage for RSL signals.

Block Diagram





SERIAL PD

Remarks **1.** Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.

2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	MIN.	MAX.	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to GND	–0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on V_{DD} with respect to GND	–0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	–50	+100	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Recommended Electrical Conditions

Symbol	Parameter and conditions		MIN.	MAX.	Unit
V_{DD}	Supply voltage		2.50 – 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad	2.5V controllers	2.5 – 0.13	2.5 + 0.25	V
		1.8V controllers	1.8 – 0.1	1.8 + 0.2	
V_{REF}	Reference voltage		1.4 – 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage		V_{REF} – 0.5	V_{REF} – 0.2	V
V_{IH}	RSL input high voltage		V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage		–0.3	0.5V_{CMOS} – 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage		0.5V_{CMOS}+0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage, $I_{OL,CMOS}$ = 1 mA		—	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage, $I_{OH,CMOS}$ = –0.25 mA		V_{CMOS} – 0.3	—	V
I_{REF}	V_{REF} current, $V_{REF,MAX}$		–40.0	+40.0	μA
$I_{SCK,CMD}$	CMOS input leakage current, ($0 \le V_{CMOS} \le V_{DD}$)		–40.0	+40.0	μA
$I_{SIN,SOUT}$	CMOS input leakage current, ($0 \le V_{CMOS} \le V_{DD}$)		–10.0	+10.0	μA

AC Electrical Specifications

Symbol	Parameter and Conditions		MIN.	TYP.	MAX.	Unit
Z	Module Impedance of RSL signals		25.2	28.0	30.8	Ω
	Module Impedance of SCK and CMD signals		23.8	28.0	32.2	
T_{PD}	Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN,CFM, and CFMN)				1.28	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to TPD Note1,2		–21		+21	ps
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK signal with respect to an average clock delay Note1		–250		+250	ps
$\Delta T_{PD\text{-}SCK,CMD}$	Propagation delay variation of CMD signal with respect to SCK signal		–200		+200	ps
V_{α}/V_{IN}	Attenuation Limit	-845			12.0	%
		-745			12.0	
		-653			10.5	
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time 20% - 80%)	-845			2.0	%
		-745			2.0	
		-653			2.0	
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time 20% - 80%)	-845			1.5	%
		-745			1.5	
		-653			1.5	
R_{DC}	DC Resistance Limit	-845			0.6	Ω
		-745			0.6	
		-653			0.6	

Notes 1. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

2. If the RIMM module meets the following specification, then it is compliant to the specification.
If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table.

Adjusted ΔT_{PD} Specification

Symbol	Parameter and conditions	Adjusted MIN./MAX.	Absolute		Unit
			MIN.	MAX.	
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}	+/– [17+(18*N*ΔZ0)] Note	–30	+30	ps

Note N = Number of RDRAM devices installed on the RIMM module.
ΔZ0 = delta Z0% = (MAX. Z0 – MIN. Z0) / (MIN. Z0)
(MAX. Z0 and MIN. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

RIMM Module Current Profile

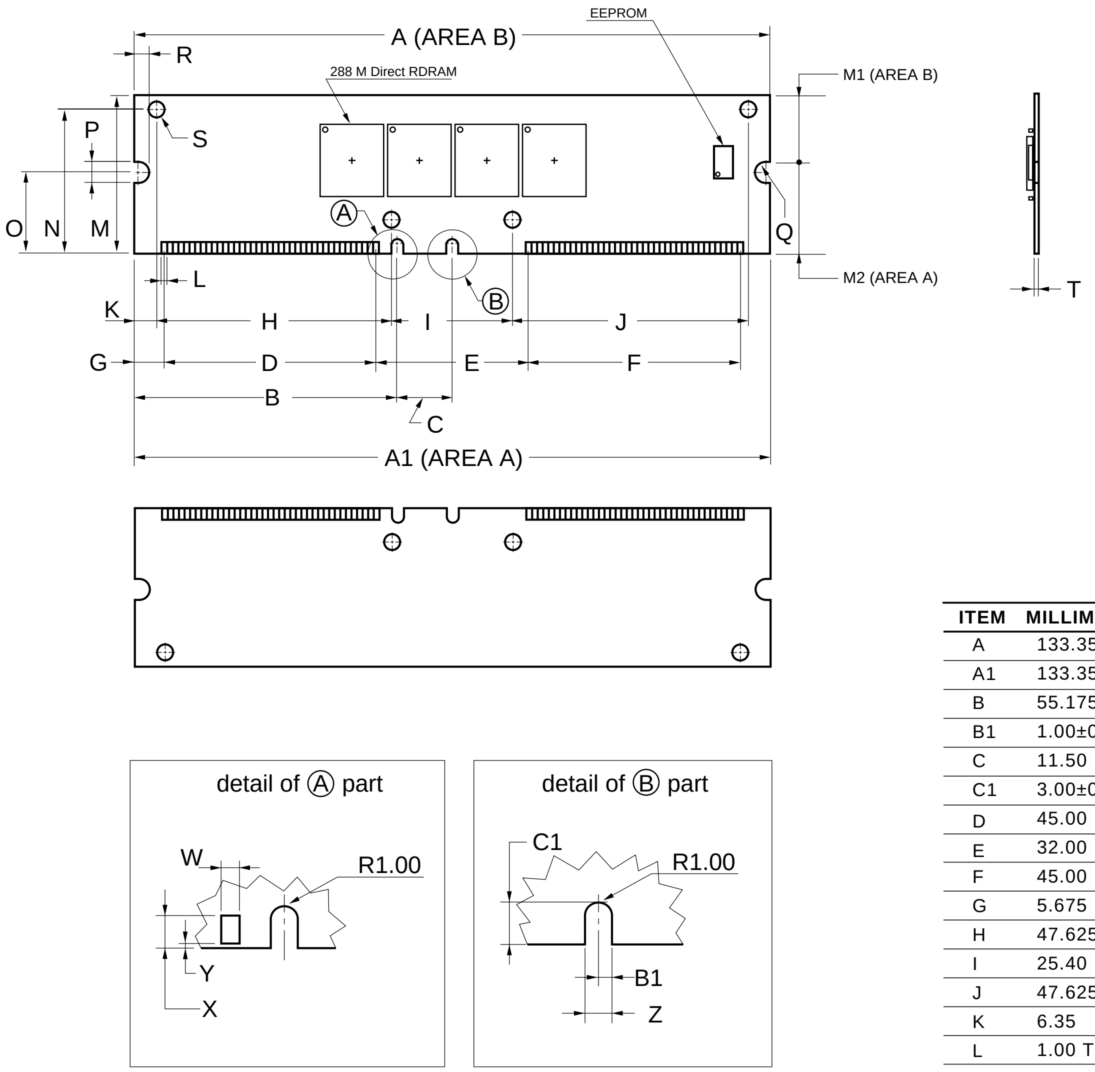
I_{DD}	RIMM module power conditions Note1		MAX.	Unit
I_{DD1}	One RDRAM in Read Note2, balance in NAP mode	-845	642.6	mA
		-745	592.6	
		-653	532.6	
I_{DD2}	One RDRAM in Read Note2, balance in Standby mode	-845	900	mA
		-745	820	
		-653	730	
I_{DD3}	One RDRAM in Read Note2, balance in Active mode	-845	1035	mA
		-745	955	
		-653	865	
I_{DD4}	One RDRAM in Write, balance in NAP mode	-845	732.6	mA
		-745	682.6	
		-653	632.6	
I_{DD5}	One RDRAM in Write, balance in Standby mode	-845	990	mA
		-745	910	
		-653	830	
I_{DD6}	One RDRAM in Write, balance in Active mode	-845	1125	mA
		-745	1045	
		-653	965	

Notes 1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x16 need to add 257 mA or 290 mA for x18 ECC module for the following : V_{DD} = 2.5 V, V_{TERM} = 1.8 V, V_{REF} = 1.4 V and V_{DIL} = V_{REF} – 0.5 V.

Package Drawings

184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (1/2)



ITEM	MILLIMETERS
A	133.35 TYP.
A1	133.35±0.13
B	55.175
B1	1.00±0.10
C	11.50
C1	3.00±0.10
D	45.00
E	32.00
F	45.00
G	5.675
H	47.625
I	25.40
J	47.625
K	6.35
L	1.00 TYP.
M	34.925±0.13
M1	15.145
M2	19.78
N	29.21
O	17.78
P	4.00±0.10
Q	R 2.00
R	3.00±0.10
S	φ2.44
T	1.27±0.10
W	0.80±0.05
X	2.99
Y	0.30
Z	2.00±0.10

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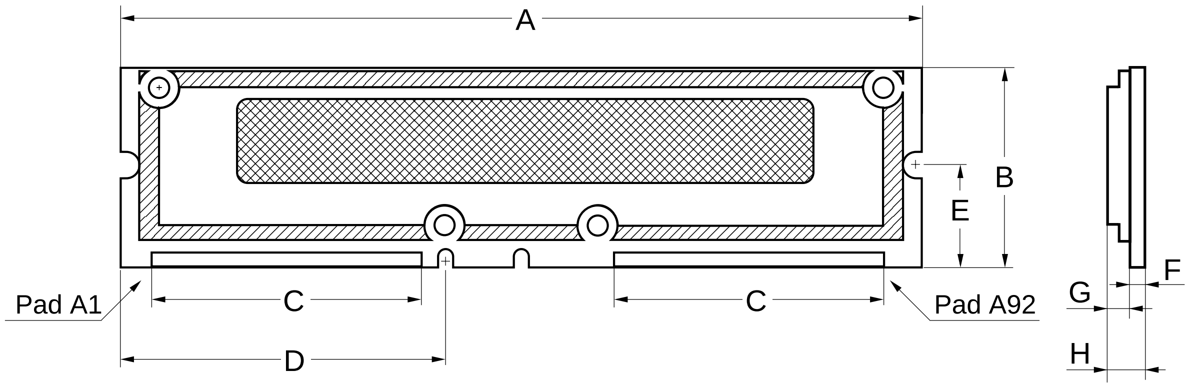
184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (2/2)



ITEM	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
A	PCB length	133.22	133.35	133.48	mm
B	PCB height	34.795	34.925	35.055	mm
C	Center-center pad width from pad A1 to A46, A47 to A92, B1 to B46 or B47 to B92	44.95	45.00	45.05	mm
D	Spacing from PCB left edge to connector key notch	-	55.175	-	mm
E	Spacing from contact pad PCB edge to side edge retainer notch	-	17.78	-	mm
F	PCB thickness	1.17	1.27	1.37	mm
G	Heat spreader thickness from PCB surface (one side) to heat spreader top surface	-	-	3.09	mm
H	RIMM thickness	-	-	4.46	mm

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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