# DATA SHEET



# MOS INTEGRATED CIRCUIT

# Direct Rambus DRAM RIMM<sup>™</sup> Module 128M-BYTE (64M-WORD x 16-BIT)

#### Description

The Direct Rambus RIMM module is a general-purpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

MC-4R128FKE6D modules consists of four 288M Direct Rambus DRAM (Direct RDRAM) devices (µPD488588). These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz, 711MHz or 800MHz transfer rates while using conventional system and board design technologies.

Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per sixteen bytes).

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95 % bus efficiency. The Direct RDRAM's 32 banks support up to four simultaneous transactions per device.

#### Features

- 184 edge connector pads with 1mm pad spacing
- 128 MB Direct RDRAM storage
- Each RDRAM® has 32 banks, for 128 banks total on module
- · Gold plated contacts
- RDRAMs use Chip Scale Package (CSP)
- Serial Presence Detect support
- Operates from a 2.5 V supply
- Powerdown self refresh modes
- Separate Row and Column buses for higher efficiency
- Over Drive Factor (ODF) support

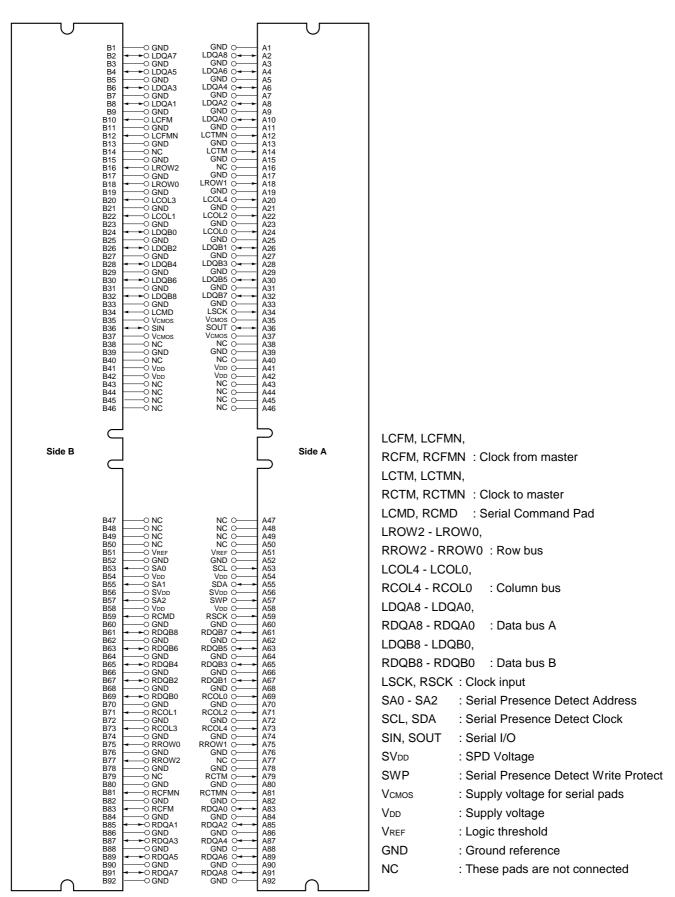
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### Order information

Part number	Organization	I/O Freq.	RAS access time	Package	Mounted devices
		MHz	ns		
MC-4R128FKE6D - 845	64M x 16	800	45	184 edge connector pads RIMM	4 pieces of
MC-4R128FKE6D - 745		711	45	with heat spreader	μPD488588FF
MC-4R128FKE6D - 653		600	53	Edge connector : Gold plated	FBGA (µBGA®) package

#### **Module Pad Configuration**



## **Module Pad Names**

PadSignal NamePadSignal NameA1GNDB1GNDA2LDQA8B2LDQA7A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMNB12LCFMNA13GNDB13GNDA14LCTMB14NCA15GNDB15GNDA16NCB16LROW2A17GNDB17GNDA18LROW1B18LROW0A19GNDB21GNDA20LCOL4B20LCOL3A21GNDB23GNDA22LCOL2B22LCOL1A23GNDB23GNDA24LCOL0B24LDQB0A25GNDB27GNDA26LDQB3B28LDQB4A29GNDB29GNDA30LDQB5B30LDQB6A31GNDB31GND
A2LDQA8B2LDQA7A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMNB12LCFMNA13GNDB13GNDA14LCTMB14NCA15GNDB15GNDA16NCB16LROW2A17GNDB17GNDA18LROW1B18LROW0A19GNDB21GNDA20LCOL4B20LCOL3A21GNDB23GNDA24LCOL0B24LDQB0A25GNDB25GNDA26LDQB1B26LDQB2A27GNDB27GNDA30LDQB5B30LDQB6A31GNDB31GND
A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMNB12LCFMNA13GNDB13GNDA14LCTMB14NCA15GNDB15GNDA16NCB16LROW2A17GNDB17GNDA18LROW1B18LROW0A19GNDB21GNDA20LCOL2B22LCOL1A23GNDB23GNDA24LCOL0B24LDQB0A25GNDB25GNDA26LDQB1B26LDQB2A27GNDB29GNDA30LDQB5B30LDQB6A31GNDB31GND
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A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMNB12LCFMNA13GNDB13GNDA14LCTMB14NCA15GNDB15GNDA16NCB16LROW2A17GNDB17GNDA18LROW1B18LROW0A20LCOL4B20LCOL3A21GNDB21GNDA22LCOL2B22LCOL1A23GNDB23GNDA24LCOL0B24LDQB0A25GNDB25GNDA26LDQB1B26LDQB2A27GNDB27GNDA30LDQB5B30LDQB6A31GNDB31GND
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A26 LDQB1 B26 LDQB2   A27 GND B27 GND   A28 LDQB3 B28 LDQB4   A29 GND B29 GND   A30 LDQB5 B30 LDQB6   A31 GND B31 GND
A27 GND B27 GND   A28 LDQB3 B28 LDQB4   A29 GND B29 GND   A30 LDQB5 B30 LDQB6   A31 GND B31 GND
A28 LDQB3 B28 LDQB4   A29 GND B29 GND   A30 LDQB5 B30 LDQB6   A31 GND B31 GND
A29 GND B29 GND   A30 LDQB5 B30 LDQB6   A31 GND B31 GND
A30 LDQB5 B30 LDQB6   A31 GND B31 GND
A31 GND B31 GND
A32 LDQB7 B32 LDQB8
A33 GND B33 GND
A34 LSCK B34 LCMD
A35 Vcmos B35 Vcmos
A36 SOUT B36 SIN
A37 Vcmos B37 Vcmos
A38 NC B38 NC
A39 GND B39 GND
A40 NC B40 NC
A41 VDD B41 VDD
A41 V <sub>DD</sub> B41 V <sub>DD</sub>
A41 VDD B41 VDD   A42 VDD B42 VDD   A43 NC B43 NC   A44 NC B44 NC
A41 VDD B41 VDD   A42 VDD B42 VDD   A43 NC B43 NC

-			
Pad	Signal Name	Pad	Signal Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	GND	B52	GND
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVDD	B56	SVDD
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	GND	B60	GND
A61	RDQB7	B61	RDQB8
A62	GND	B62	GND
A63	RDQB5	B63	RDQB6
A64	GND	B64	GND
A65	RDQB3	B65	RDQB4
A66	GND	B66	GND
A67	RDQB1	B67	RDQB2
A68	GND	B68	GND
A69	RCOL0	B69	RDQB0
A70	GND	B70	GND
A71	RCOL2	B71	RCOL1
A72	GND	B72	GND
A73	RCOL4	B73	RCOL3
A74	GND	B74	GND
A75	RROW1	B75	RROW0
A76	GND	B76	GND
A77	NC	B77	RROW2
A78	GND	B78	GND
A79	RCTM	B79	NC
A80	GND	B80	GND
A81	RCTMN	B81	RCFMN
A82	GND	B82	GND
A83	RDQA0	B83	RCFM
A84	GND	B84	GND
A85	RDQA2	B85	RDQA1
A86	GND	B86	GND
A87	RDQA4	B87	RDQA3
A88	GND	B88	GND
A89	RDQA6	B89	RDQA5
A90	GND	B90	GND
A91	RDQA8	B91	RDQA7
A92	GND	B92	GND

# Module Connector Pad Description

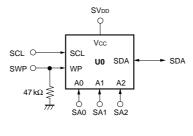
(1/2)

Signal	I/O	Туре	Description	
GND	_	_	Ground reference for RDRAM core and interface. 72 PCB connector pads.	
LCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	
LCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	
LCMD	I	Vcmos	Serial Command used to read from and write to the control registers. Also used for power management.	
LCOL4LCOL0	Ι	RSL	Column bus. 5-bit bus containing control and address information for column accesses.	
LCTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.	
LCTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.	
LDQA8LDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices.	
LDQB8LDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.	
LROW2LROW0	Ι	RSL	Row bus. 3-bit bus containing control and address information for row accesses.	
LSCK	I	Vcmos	Serial clock input. Clock source used to read from and write to the RDRAM control registers.	
NC	-	-	These pads are not connected. These 24 connector pads are reserved for future use.	
RCFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.	
RCFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.	
RCMD	I	Vcmos	Serial Command Input used to read from and write to the control registers. Also used for power management.	
RCOL4RCOL0	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.	
RCTM	Ι	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.	
RCTMN	Ι	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.	
RDQA8RDQA0	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.	
RDQB8RDQB0	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.	
RROW2RROW0	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.	

Signal	I/O	Туре	(2/2) Description
RSCK	Ι	Vcmos	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	I	SVDD	Serial Presence Detect Address 0.
SA1	I	SVDD	Serial Presence Detect Address 1.
SA2	Ι	SVDD	Serial Presence Detect Address 2.
SCL	I	SVDD	Serial Presence Detect Clock.
SDA	I/O	SVDD	Serial Presence Detect Data (Open Collector I/O).
SIN	I/O	Vcmos	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	I/O	Vcmos	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SVDD	_	_	SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.
SWP	I	SVDD	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
Vcmos	_	_	CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	_	_	Supply voltage for the RDRAM core and interface logic.
VREF	_	_	Logic threshold reference voltage for RSL signals.

### **Block Diagram**

SIN O LSCK O VREF O	Voto Voto Voto Voto Voto Voto Voto Voto
	SIO 0 SIO 1 SCK CMD VREF U1 SCK CMD VREF DO 08 8 0 0 - 1 2 3 4 0 1 2 3 4 5 5 6 7 8
•	SIO 0 SIO 1 SCK U2 CMD VREF DD D D D D D D D D D D D D D D D D D D
	SIO 0 SIO 1 SCK CMD VREF D D D D D D D D D D D D D D D D D D D
	- SIO 0 - SIO 1 - SCK - CMD - VREF
-0 SOUT RSCK	





Remarks 1. Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Data Sheet E0093N20 (Ver. 2.0)

## **Electrical Specification**

#### Absolute Maximum Ratings

Symbol	Parameter	MIN.	MAX.	Unit
VI,ABS	Voltage applied to any RSL or CMOS signal pad with respect to GND	-0.3	Vdd + 0.3	V
Vdd,abs	Voltage on VDD with respect to GND	-0.5	Vdd + 1.0	V
TSTORE	Storage temperature	-50	+100	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Symbol	Parameter and conditions		MIN.	MAX.	Unit
Vdd	Supply voltage		2.50 – 0.13	2.50 + 0.13	V
Vcmos	CMOS I/O power supply at pad	2.5V controllers	2.5 – 0.13	2.5 + 0.25	V
		1.8V controllers	1.8 – 0.1	1.8 + 0.2	
Vref	Reference voltage		1.4 – 0.2	1.4 + 0.2	V
VIL	RSL input low voltage		Vref – 0.5	Vref - 0.2	V
Vін	RSL input high voltage		Vref + 0.2	Vref + 0.5	V
VIL,CMOS	CMOS input low voltage		-0.3	0.5Vсмоs – 0.25	V
VIH,CMOS	CMOS input high voltage		0.5Vсмоs+0.25	Vсмоs + 0.3	V
Vol,cmos	CMOS output low voltage, IoL,CMOS = 1 mA		_	0.3	V
Vон,смоs	CMOS output high voltage, Іон,смоs = -0.25 mA		Vсмоs – 0.3	_	V
IREF	VREF current, VREF,MAX		-40.0	+40.0	μA
Isck,cmd	CMOS input leakage current, ( $0 \le V CMOS \le V DD$ )	CMOS input leakage current, ( $0 \le VCMOS \le VDD$ )			μA
Isin,sout	CMOS input leakage current, ( $0 \le VCMOS \le VDD$ )		-10.0	+10.0	μA

#### **DC Recommended Electrical Conditions**

#### **AC Electrical Specifications**

Symbol	Parameter and Conditions		MIN.	TYP.	MAX.	Unit
z	Module Impedance of RSL signals		25.2	28.0	30.8	Ω
	Module Impedance of SCK and CMD signals		23.8	28.0	32.2	
Tpd	Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN,CFM, and CFMN)				1.28	ns
ΔTpd	Propagation delay variation of RSL signals with respect to TPD Note1,2		-21		+21	ps
$\Delta T$ PD-CMOS	Propagation delay variation of SCK signal with respect to an average delay <sup>Note1</sup>	clock	-250		+250	ps
$\Delta T$ PD- SCK,CMD	Propagation delay variation of CMD signal with respect to SCK signal		-200		+200	ps
Vα/Vin	Attenuation Limit	-845			12.0	%
		-745			12.0	
		-653			10.5	
Vxf/Vin	Forward crosstalk coefficient	-845			2.0	%
	(300ps input rise time 20% - 80%)	-745			2.0	
		-653			2.0	
Vxb/Vin	Backward crosstalk coefficient	-845			1.5	%
	(300ps input rise time 20% - 80%)	-745			1.5	
		-653			1.5	
RDC	DC Resistance Limit	-845			0.6	Ω
		-745			0.6	
		-653			0.6	

**Notes 1.** TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

 If the RIMM module meets the following specification, then it is compliant to the specification. If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔTPD Specification" table.

#### Adjusted $\Delta T_{PD}$ Specification

Symbol	Parameter and conditions	Adjusted MIN./MAX.	Abso	olute	Unit
			MIN.	MAX.	r
$\Delta T_{PD}$	Propagation delay variation of RSL signals with respect to $T_{PD}$	+/- [17+(18*N*∆Z0)] <sup>Note</sup>	-30	+30	ps

**Note** N = Number of RDRAM devices installed on the RIMM module.

 $\Delta$ Z0 = delta Z0% = (MAX. Z0 – MIN. Z0) / (MIN. Z0)

(MAX. Z0 and MIN. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

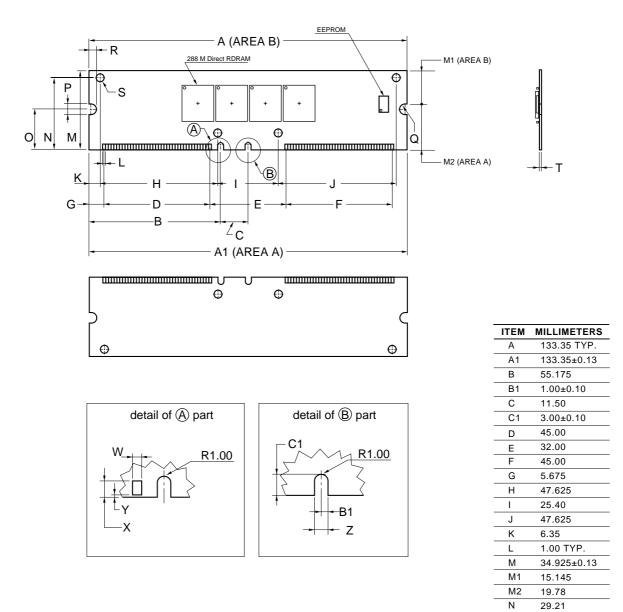
ldd	RIMM module power conditions Note1		MAX.	Unit
IDD1	One RDRAM in Read <sup>Note2</sup> , balance in NAP mode	-845	642.6	mA
		-745	592.6	
		-653	532.6	
DD2	One RDRAM in Read <sup>Note2</sup> , balance in Standby mode	-845	900	mA
		-745	820	
		-653	730	
Гооз	One RDRAM in Read <sup>Note2</sup> , balance in Active mode	-845	1035	mA
		-745	955	
		-653	865	
IDD4	One RDRAM in Write, balance in NAP mode	-845	732.6	mA
		-745	682.6	
		-653	632.6	
DD5	One RDRAM in Write, balance in Standby mode	-845	990	mA
		-745	910	
		-653	830	
DD6	One RDRAM in Write, balance in Active mode	-845	1125	mA
		-745	1045	
		-653	965	

**Notes 1.** Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x16 need to add 257 mA or 290 mA for x18 ECC module for the following : VDD = 2.5 V, VTERM = 1.8 V, VREF = 1.4 V and VDIL = VREF - 0.5 V.

#### **Package Drawings**

# 184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (1/2)



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17.78

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0.30

ECA-TS2-0012-02

4.00±0.10

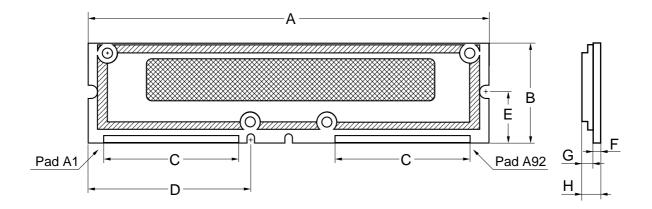
3.00±0.10

1.27±0.10

0.80±0.05

2.00±0.10

# 184 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (2/2)



ITEM	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
А	PCB length	133.22	133.35	133.48	mm
В	PCB height	34.795	34.925	35.055	mm
С	Center-center pad width from pad A1 to A46,	44.95	45.00	45.05	mm
	A47 to A92, B1 to B46 or B47 to B92				
D	Spacing from PCB left edge to connector key notch	-	55.175	-	mm
E	Spacing from contact pad PCB edge	-	17.78	-	mm
	to side edge retainer notch				
F	PCB thickness	1.17	1.27	1.37	mm
G	Heat spreader thickness from PCB surface (one side) to	-	-	3.09	mm
	heat spreader top surface				
Н	RIMM thickness	-	-	4.46	mm

ECA-TS2-0012-02

## CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

#### NOTES FOR CMOS DEVICES -

#### **①** PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

#### **③** STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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#### [Usage environment]

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