### DATA SHEET

# ΕLΡΙDΛ

# MOS INTEGRATED CIRCUIT MC-4R256FKE8S-840

## Direct Rambus DRAM SO-RIMM<sup>™</sup> Module 256M-BYTE (128M-WORD x 18-BIT)

### Description

The Direct Rambus SO-RIMM module is a general-purpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, mobile personal computers, networking systems, and other applications where high bandwidth and low latency are required.

MC-4R256FKE8S modules consists of eight 288M Direct Rambus DRAM (Direct RDRAM) devices (µPD488588). These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 800MHz transfer rates while using conventional system and board design technologies.

Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per 16 bytes).

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions. The separate control and data buses with independent row and column control yield high bus efficiency. The Direct RDRAM's multi-bank architecture supports up to four simultaneous transactions per device.

### Features

- 160 edge connector pads with 0.65mm pad spacing
- 256 MB Direct RDRAM storage
- Each RDRAM® has 32 banks, for 256 banks total on module
- · Gold plated contacts
- RDRAMs use Chip Scale Package (CSP)
- Serial Presence Detect support
- Operates from a 2.5 V supply
- Powerdown self refresh modes
- Separate Row and Column buses for higher efficiency

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### Order information

| Part number         | Organization | I/O Freq. | RAS access time | Package  | Mounted devices  |
|---------------------|--------------|-----------|-----------------|--|--|
|                     |              | MHz       | ns              |  |  |
| MC-4R256FKE8S - 840 | 128M x 18    | 800       | 40              | 160 edge connector pads<br>SO-RIMM with heat spreader<br>Edge connector: Gold plated | 8 pieces of μPD488588FF<br>FBGA (μBGA <sup>®</sup> ) package |

### Module Pad Configuration

### **Module Pad Names**

| A1GNDB1GNDA2LDQA8B2LDQA7A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB23GNDA22LCOL0B22LDQB1A23GNDB25GNDA24LDQ80B24LDQ83A25GNDB27GNDA26LDQ84B28LDQB7A29GNDB29GNDA30LDQ86B30LDQ88A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VooB35VooA36NCB36NCA39VCMOSB39VCMOS   | Pad | Signal Name | Pad | Signal Name |
|---|-----|-------------|-----|-------------|
| A2LDQA8B2LDQA7A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB10LCFMA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL2B20LCOL1A20LCOL2B20LCOL1A21GNDB23GNDA22LCOL0B22LDQB1A23GNDB25GNDA24LDQB0B24LDQB3A25GNDB27GNDA26LDQB4B28LDQB7A29GNDB31GNDA30LDQB6B30LDQB8A31GNDB33GNDA33GNDB33GNDA34SOUTB34SINA35VooB35VooA36NCB36NCA39VCMOSB39VCMOS   |     | -           |     |             |
| A3GNDB3GNDA4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB22LDQB1A20LCOLB22LDQB1A21GNDB23GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB27GNDA26LDQB4B28LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS  |     |             |     |             |
| A4LDQA6B4LDQA5A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB21GNDA20LCOL2B20LCOL1A21GNDB23GNDA22LCOL0B22LDQB1A23GNDB25GNDA26LDQB2B26LDQB3A25GNDB27GNDA26LDQB4B28LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VcmosB39Vcmos   |     |             |     |             |
| A5GNDB5GNDA6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL2B20LCOL1A20LCOL2B20LCOL1A21GNDB23GNDA22LCOL0B22LDQB1A23GNDB25GNDA24LDQB0B24LDQB3A25GNDB27GNDA26LDQB2B26LDQB5A27GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NC   |     |             | -   |             |
| A6LDQA4B6LDQA3A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB22LDQB1A20LCOL2B20LCOL1A21GNDB23GNDA22LCOL0B22LDQB3A24LDQB0B24LDQB3A25GNDB27GNDA26LDQB2B26LDQB5A27GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS   |     |             |     |             |
| A7GNDB7GNDA8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB21GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB4B28LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VD0B35VD0A36NCB36NCA39VCM0SB39VCM0S   |     |             |     |             |
| A8LDQA2B8LDQA1A9GNDB9GNDA10LDQA0B10LCFMA11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB21GNDA20LCOL2B20LCOL1A21GNDB23GNDA22LCOL0B22LDQB1A23GNDB25GNDA24LDQB0B24LDQB3A25GNDB27GNDA26LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS   |     |             |     |             |
| A9     GND     B9     GND       A10     LDQA0     B10     LCFM       A11     GND     B11     GND       A12     LCTM     B12     LCFMN       A13     GND     B13     GND       A14     LCTMN     B14     LROW2       A15     GND     B15     GND       A16     LROW1     B16     LROW0       A17     GND     B17     GND       A18     LCOL4     B18     LCOL3       A19     GND     B19     GND       A20     LCOL2     B20     LCOL1       A21     GND     B23     GND       A22     LCOL0     B22     LDQB1       A23     GND     B23     GND       A24     LDQB0     B24     LDQB3       A25     GND     B27     GND       A26     LDQB4     B28     LDQB7       A29     GND     B31     GND       A30     LDQB6   |     |             |     |             |
| A10     LDQA0     B10     LCFM       A11     GND     B11     GND       A12     LCTM     B12     LCFMN       A13     GND     B13     GND       A14     LCTMN     B14     LROW2       A15     GND     B15     GND       A16     LROW1     B16     LROW0       A17     GND     B17     GND       A18     LCOL4     B18     LCOL3       A19     GND     B19     GND       A20     LCOL2     B20     LCOL1       A21     GND     B23     GND       A22     LCOL0     B22     LDQB1       A23     GND     B23     GND       A24     LDQB0     B24     LDQB3       A25     GND     B27     GND       A26     LDQB4     B28     LDQB7       A29     GND     B29     GND       A30     LDQB6     B30     LDQB8       A31     GND <td></td> <td></td> <td></td> <td></td> |     |             |     |             |
| A11GNDB11GNDA12LCTMB12LCFMNA13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB20LCOL1A20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS  |     |             |     |             |
| A12     LCTM     B12     LCFMN       A13     GND     B13     GND       A14     LCTMN     B14     LROW2       A15     GND     B15     GND       A16     LROW1     B16     LROW0       A17     GND     B17     GND       A18     LCOL4     B18     LCOL3       A19     GND     B19     GND       A20     LCOL2     B20     LCOL1       A21     GND     B21     GND       A22     LCOL0     B22     LDQB1       A23     GND     B23     GND       A24     LDQB0     B24     LDQB3       A25     GND     B27     GND       A26     LDQB2     B26     LDQB5       A27     GND     B29     GND       A30     LDQB6     B30     LDQB8       A31     GND     B31     GND       A33     GND     B33     GND       A34     SOUT   | A10 |             | B10 |             |
| A13GNDB13GNDA14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB22LDQB1A22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS   | A11 | GND         | B11 | GND         |
| A14LCTMNB14LROW2A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA30LDQB6B30LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB38NCA39VCMOSB39VCMOS   | A12 | LCTM        | B12 | LCFMN       |
| A15GNDB15GNDA16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA30LDQB6B30LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB38NCA39VCMOSB39VCMOS   | A13 | GND         | B13 | GND         |
| A16LROW1B16LROW0A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA36NCB36NCA37GNDB37GNDA38NCB38NCA39VCMOSB39VCMOS   | A14 | LCTMN       | B14 | LROW2       |
| A17GNDB17GNDA18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB6B30LDQB8A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB37GNDA36NCB38NCA39VCMOSB39VCMOS   | A15 | GND         | B15 | GND         |
| A18LCOL4B18LCOL3A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB29GNDA28LDQB6B30LDQB8A30LDQB6B31GNDA31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB37GNDA36NCB38NCA39VCMOSB39VCMOS   | A16 | LROW1       | B16 | LROW0       |
| A19GNDB19GNDA20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB29GNDA28LDQB6B30LDQB8A30LDQB6B31GNDA31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB37GNDA36NCB38NCA39VCMOSB39VCMOS   | A17 | GND         | B17 | GND         |
| A20LCOL2B20LCOL1A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB6B30LDQB8A30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS   | A18 | LCOL4       | B18 | LCOL3       |
| A21GNDB21GNDA22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB6B30LDQB8A30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB37GNDA36NCB38NCA39VCMOSB39VCMOS   | A19 | GND         | B19 | GND         |
| A22LCOL0B22LDQB1A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB4B28LDQB7A29GNDB30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA39VCMOSB39VCMOS   | A20 | LCOL2       | B20 | LCOL1       |
| A23GNDB23GNDA24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB4B28LDQB7A30LDQB6B30LDQB8A31GNDB31GNDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB38NCA39VCMOSB39VCMOS   | A21 | GND         | B21 | GND         |
| A24LDQB0B24LDQB3A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB35VDDA36NCB36NCA37GNDB37GNDA38NCB39VCMOS  | A22 | LCOL0       | B22 | LDQB1       |
| A25GNDB25GNDA26LDQB2B26LDQB5A27GNDB27GNDA28LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA38NCB38NCA39VCMOSB39VCMOS   | A23 | GND         | B23 | GND         |
| A26LDQB2B26LDQB5A27GNDB27GNDA28LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA36NCB36NCA37GNDB37GNDA38NCB38NCA39VcmosB39Vcmos   | A24 | LDQB0       | B24 | LDQB3       |
| A27GNDB27GNDA28LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VcmosB39Vcmos   | A25 | GND         | B25 | GND         |
| A28LDQB4B28LDQB7A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB37GNDA38NCB38NCA39VcmosB39Vcmos  | A26 | LDQB2       | B26 | LDQB5       |
| A29GNDB29GNDA30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VcmosB39Vcmos   | A27 | GND         | B27 | GND         |
| A30LDQB6B30LDQB8A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VcmosB39Vcmos   | A28 | LDQB4       | B28 | LDQB7       |
| A31GNDB31GNDA32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VCMOSB39VCMOS   | A29 | GND         | B29 | GND         |
| A32LSCKB32LCMDA33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VCMOSB39VCMOS   | A30 | LDQB6       | B30 | LDQB8       |
| A33GNDB33GNDA34SOUTB34SINA35VDDB35VDDA36NCB36NCA37GNDB37GNDA38NCB38NCA39VCMOSB39VCMOS   | A31 | GND         | B31 | GND         |
| A34     SOUT     B34     SIN       A35     VDD     B35     VDD       A36     NC     B36     NC       A37     GND     B37     GND       A38     NC     B38     NC       A39     Vcmos     B39     Vcmos  | A32 | LSCK        | B32 | LCMD        |
| A34     SOUT     B34     SIN       A35     VDD     B35     VDD       A36     NC     B36     NC       A37     GND     B37     GND       A38     NC     B38     NC       A39     Vcmos     B39     Vcmos  | A33 | GND         | B33 | GND         |
| A36     NC     B36     NC       A37     GND     B37     GND       A38     NC     B38     NC       A39     Vcmos     B39     Vcmos   | A34 |             | B34 | SIN         |
| A36     NC     B36     NC       A37     GND     B37     GND       A38     NC     B38     NC       A39     Vcmos     B39     Vcmos   | A35 | Vdd         | B35 | Vdd         |
| A37     GND     B37     GND       A38     NC     B38     NC       A39     Vcmos     B39     Vcmos   |     | NC          |     |             |
| A38     NC     B38     NC       A39     Vcmos     B39     Vcmos   |     |             | B37 |             |
| A39 Vcmos B39 Vcmos   |     | NC          |     |             |
|   |     |             |     |             |
|   | A40 | NC          | B40 | NC          |

| Pad | Signal Name | Pad | Signal Name |
|-----|-------------|-----|-------------|
| A41 | NC          | B41 | NC          |
| A42 | VREF        | B42 | Vref        |
| A43 | SCL         | B43 | SA0         |
| A44 | Vdd         | B44 | Vdd         |
| A45 | SDA         | B45 | SA1         |
| A46 | Vdd         | B46 | Vdd         |
| A47 | SVDD        | B47 | SWP         |
| A48 | GND         | B48 | GND         |
| A49 | RSCK        | B49 | RCMD        |
| A50 | GND         | B50 | GND         |
| A51 | RDQB8       | B51 | RDQB6       |
| A52 | GND         | B52 | GND         |
| A53 | RDQB7       | B53 | RDQB4       |
| A54 | GND         | B54 | GND         |
| A55 | RDQB5       | B55 | RDQB2       |
| A56 | GND         | B56 | GND         |
| A57 | RDQB3       | B57 | RDQB0       |
| A58 | GND         | B58 | GND         |
| A59 | RDQB1       | B59 | RCOL0       |
| A60 | GND         | B60 | GND         |
| A61 | RCOL1       | B61 | RCOL2       |
| A62 | GND         | B62 | GND         |
| A63 | RCOL3       | B63 | RCOL4       |
| A64 | GND         | B64 | GND         |
| A65 | RROW0       | B65 | RROW1       |
| A66 | GND         | B66 | GND         |
| A67 | RROW2       | B67 | RCTMN       |
| A68 | GND         | B68 | GND         |
| A69 | RCFMN       | B69 | RCTM        |
| A70 | GND         | B70 | GND         |
| A71 | RCFM        | B71 | RDQA0       |
| A72 | GND         | B72 | GND         |
| A73 | RDQA1       | B73 | RDQA2       |
| A74 | GND         | B74 | GND         |
| A75 | RDQA3       | B75 | RDQA4       |
| A76 | GND         | B76 | GND         |
| A77 | RDQA5       | B77 | RDQA6       |
| A78 | GND         | B78 | GND         |
| A79 | RDQA7       | B79 | RDQA8       |
| A80 | GND         | B80 | GND         |

### **Module Connector Pad Description**

(1/2)

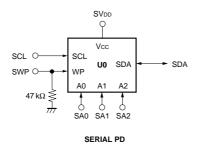
| Signal     | I/O | Туре  | Description   |
|------------|-----|-------|---|
| GND        | -   | _     | Ground reference for RDRAM core and interface.  |
| LCFM       | I   | RSL   | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.  |
| LCFMN      | I   | RSL   | Clock from master. Interface clock used for receiving RSL signals from the<br>Channel. Negative polarity.   |
| LCMD       | I   | Vcmos | Serial Command used to read from and write to the control registers. Also used for power management.  |
| LCOL4LCOL0 | I   | RSL   | Column bus. 5-bit bus containing control and address information for column accesses.   |
| LCTM       | Ι   | RSL   | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.   |
| LCTMN      | Ι   | RSL   | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.   |
| LDQA8LDQA0 | I/O | RSL   | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices. |
| LDQB8LDQB0 | I/O | RSL   | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices. |
| LROW2LROW0 | I   | RSL   | Row bus. 3-bit bus containing control and address information for row accesses.   |
| LSCK       | I   | Vcmos | Serial clock input. Clock source used to read from and write to the RDRAM control registers.  |
| NC         | _   | _     | These pads are not connected. These 8 connector pads are reserved for future use.   |
| RCFM       | I   | RSL   | Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.  |
| RCFMN      | I   | RSL   | Clock from master. Interface clock used for receiving RSL signals from the<br>Channel. Negative polarity.   |
| RCMD       | I   | Vcmos | Serial Command Input used to read from and write to the control registers. Also used for power management.  |
| RCOL4RCOL0 | I   | RSL   | Column bus. 5-bit bus containing control and address information for column accesses.   |
| RCTM       | Ι   | RSL   | Clock to master. Interface clock used for transmitting RSL signals to the<br>Channel. Positive polarity.  |
| RCTMN      | Ι   | RSL   | Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.   |
| RDQA8RDQA0 | I/O | RSL   | Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices. |
| RDQB8RDQB0 | I/O | RSL   | Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices. |
| RROW2RROW0 | Т   | RSL   | Row bus. 3-bit bus containing control and address information for row accesses.   |

| -      |     |       | (2/2)  |
|--------|-----|-------|--|
| Signal | I/O | Туре  | Description  |
| RSCK   | Ι   | Vсмоs | Serial clock input. Clock source used to read from and write to the RDRAM control registers.                         |
| SA0    | I   | SVDD  | Serial Presence Detect Address 0.  |
| SA1    | I   | SVDD  | Serial Presence Detect Address 1.  |
| SCL    | I   | SVDD  | Serial Presence Detect Clock.  |
| SDA    | I/O | SVDD  | Serial Presence Detect Data (Open Collector I/O).  |
| SIN    | I/O | Vcmos | Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module. |
| SOUT   | I/O | Vсмоs | Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.  |
| SVDD   | _   | _     | SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.   |
| SWP    | Ι   | SVDD  | Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.                |
| Vcmos  | _   | _     | CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.  |
| Vdd    | _   | _     | Supply voltage for the RDRAM core and interface logic.   |
| Vref   |     | _     | Logic threshold reference voltage for RSL signals.   |

### **Block Diagram**

| SIN OLIVEF | Vor     Vor       Vorwos     Daa       LDaa     Daa       LCAM     Daa       LCAM     Daa       LCAM     Daa       LCAM     Daa       LCAM     Daa       LCAM     CHM       LCAM     CHM       LCAN     CHM       LCAN     CHM       LCAN     CHM       LCAN     CHM       LCAN     CHM       LCAN     CHM  |
|------------|--|
|            | SIO 0<br>SIO 1<br>U1<br>SCK<br>CMD<br>VREF   |
|            | D D D D D D D D D D D D D D D D D D D  |
|            | SIO 1<br>SCK U2<br>CMD<br>VREF   |
|            | DQB 5 4<br>SIO 0   |
|            | SIO 1 U3<br>SCK CMD<br>VREF  |
|            | DQBB 2<br>DQBB 2<br>DQBB 5<br>COLL 2<br>DQBB 5<br>COLL 2<br>COLL 2<br>CO |
|            | SIO 0<br>- SIO 1<br>- SCK<br>- CMD<br>- VREF   |
| O RSCK     | RECOL 1<br>RECOL 2<br>RECOL 2<br>REC   |

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- **Remarks 1.** Rambus Channel signals form a loop through the SO-RIMM module, with the exception of the SIO chain.
  - 2. See Serial Presence Detection Specification for information on the SPD device and its contents.

### **Electrical Specification**

### Absolute Maximum Ratings

| Symbol  | Parameter   | MIN. | MAX.      | Unit |
|---------|---|------|-----------|------|
| VI,ABS  | Voltage applied to any RSL or CMOS signal pad with respect to GND | -0.3 | VDD + 0.3 | V    |
| Vdd,abs | Voltage on VDD with respect to GND                                | -0.5 | Vdd + 1.0 | V    |
| TSTORE  | Storage temperature   | -50  | +100      | °C   |

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

| Symbol    | Parameter and conditions                                    |  | MIN.                   | MAX.                   | Unit |
|-----------|---|--|------------------------|------------------------|------|
| Vdd       | Supply voltage  | y voltage                                |                        | 2.50 + 0.13            | V    |
| Vсмоs     | CMOS I/O power supply at pad 2.5V controllers               |  | Vdd                    | Vdd                    | V    |
|           |   | 1.8V controllers                         | 1.8 – 0.1              | 1.8 + 0.2              |      |
| Vref      | Reference voltage   |  | 1.4 – 0.2              | 1.4 + 0.2              | V    |
| VSPD      | Serial presence detector-positive power supply              |  | 2.2                    | 3.6                    | V    |
| VIL       | RSL input low voltage                                       |  | Vref - 0.5             | Vref - 0.2             | V    |
| Vн        | RSL input high voltage                                      |  | V <sub>REF</sub> + 0.2 | V <sub>REF</sub> + 0.5 | V    |
| VIL,CMOS  | CMOS input low voltage                                      |  | -0.3                   | 0.5Vсмоя – 0.25        | V    |
| VIH,CMOS  | CMOS input high voltage                                     |  | 0.5Vсмоs+0.25          | Vсмоs + 0.3            | V    |
| Vol,cmos  | CMOS output low voltage, IOL,CMOS = 1 mA                    | CMOS output low voltage, IoL,CMOS = 1 mA |                        | 0.3                    | V    |
| Vон,смоs  | CMOS output high voltage, Іон,смоs = -0.25 mA               |  | Vсмоs – 0.3            | _                      | V    |
| IREF      | VREF current, VREF,MAX                                      |  | -80.0                  | +80.0                  | μA   |
| Isck,смd  | CMOS input leakage current, (0 ≤ Vcмos ≤ Vbb)               |  | -80.0                  | +80.0                  | μA   |
| Isin,sout | CMOS input leakage current, ( $0 \le V_{CMOS} \le V_{DD}$ ) |  | -10.0                  | +10.0                  | μA   |

### **DC Recommended Electrical Conditions**

### **AC Electrical Specifications**

| Symbol                 | Parameter and Conditions  |      | MIN. | TYP. | MAX. | Unit |
|------------------------|---|------|------|------|------|------|
| z                      | Module Impedance of RSL signals   |      | 25.2 | 28.0 | 30.8 | Ω    |
|                        | Module Impedance of SCK and CMD signals   |      | 23.8 | 28.0 | 32.2 |      |
| Tpd                    | Average clock delay from finger to finger of all RSL clock nets                                   |      |      |      | 1.32 | ns   |
|                        | (CTM, CTMN,CFM, and CFMN)   |      |      |      |      |      |
| $\Delta T_{PD}$        | Propagation delay variation of RSL signals with respect to TPD Note1,2                            |      | -21  |      | +21  | ps   |
| $\Delta T$ PD-CMOS     | Propagation delay variation of SCK signal with respect to an average clock delay <sup>Note1</sup> |      | -250 |      | +250 | ps   |
| $\Delta T$ PD- SCK,CMD | Propagation delay variation of CMD signal with respect to SCK signal                              |      | -200 |      | +200 | ps   |
| Vα/VIN                 | Attenuation Limit   | -840 |      |      | 16.0 | %    |
| Vxf/Vin                | Forward crosstalk coefficient   | -840 |      |      | 4.0  | %    |
| Vxb/Vin                | Backward crosstalk coefficient  | -840 |      |      | 2.0  | %    |
| RDC                    | DC Resistance Limit   | -840 |      |      | 1.4  | Ω    |

**Notes 1.** TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

 If the SO-RIMM module meets the following specification, then it is compliant to the specification. If the SO-RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔTPD Specification" table.

### Adjusted $\Delta T_{PD}$ Specification

| Symbol          | Parameter and conditions  | Adjusted MIN./MAX.                 | Absolute |      | Unit |
|-----------------|---|------------------------------------|----------|------|------|
|                 |   |                                    | MIN.     | MAX. |      |
| $\Delta T_{PD}$ | Propagation delay variation of RSL signals with respect to $T_{PD}$ | +/- [17+(18*N*∆Z0)] <sup>№te</sup> | -30      | +30  | ps   |

**Note** N = Number of RDRAM devices installed on the SO-RIMM module.

 $\Delta$ Z0 = delta Z0% = (MAX. Z0 – MIN. Z0) / (MIN. Z0)

(MAX. Z0 and MIN. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

### **SO-RIMM Module Current Profile**

| lod  | RIMM module power conditions Note1                           |      | MAX.  | Unit |
|------|--|------|-------|------|
| IDD1 | One RDRAM in Read <sup>Note2</sup> , balance in NAP mode     | -840 | 734.4 | mA   |
| Idd2 | One RDRAM in Read <sup>Note2</sup> , balance in Standby mode | -840 | 1335  | mA   |
| Іддз | One RDRAM in Read <sup>Note2</sup> , balance in Active mode  | -840 | 1650  | mA   |
| Idd4 | One RDRAM in Write, balance in NAP mode                      | -840 | 794.4 | mA   |
| Idd5 | One RDRAM in Write, balance in Standby mode                  | -840 | 1395  | mA   |
| Idd6 | One RDRAM in Write, balance in Active mode                   | -840 | 1710  | mA   |

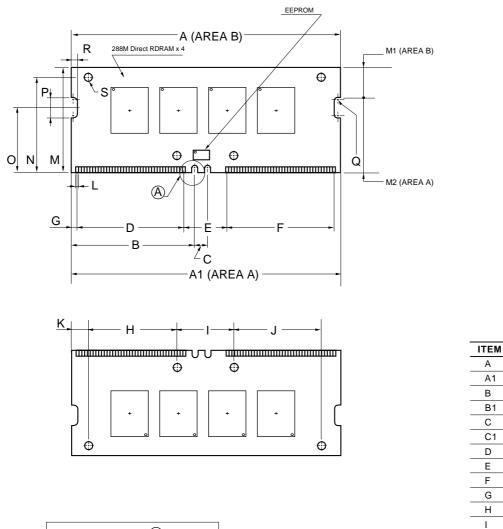
**Notes 1.** Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x16 need to add 257 mA or 290 mA for x18 ECC module for the following : VDD = 2.5 V, VTERM = 1.8 V, VREF = 1.4 V and VDIL = VREF - 0.5 V.

Data Sheet E0257N20 (Ver. 2.0)

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### Package Drawings



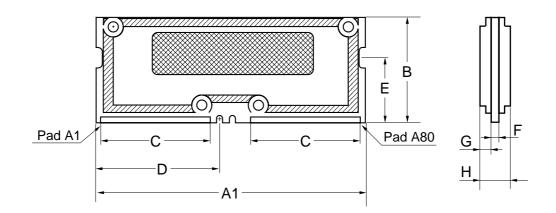
160 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (1/2)

# detail of $\bigcirc$ part C1 W R0.75 $\bigcirc$ V B1 X - Z

| ITEM          | MILLIMETERS      |  |  |
|---------------|------------------|--|--|
| A             | 67.60 TYP.       |  |  |
| A1            | 67.60 ± 0.15     |  |  |
| В             | 30.00            |  |  |
| B1            | 0.75 ± 0.10      |  |  |
| С             | 4.00             |  |  |
| C1            | 4.00 ± 0.10      |  |  |
| D             | 25.35            |  |  |
| E             | 13.60            |  |  |
| F             | 25.35            |  |  |
| G             | 1.65             |  |  |
| н             | 21.00            |  |  |
| I             | 17.00            |  |  |
| J             | 21.00            |  |  |
| к             | 4.30             |  |  |
| L             | 0.65 TYP.        |  |  |
| М             | $31.25 \pm 0.15$ |  |  |
| M1            | 8.75             |  |  |
| M2            | 22.50            |  |  |
| N             | 29.25            |  |  |
| 0             | 20.00            |  |  |
| Р             | $5.00\pm0.10$    |  |  |
| Q             | R1.00            |  |  |
| R             | 1.00 ± 0.10      |  |  |
| S             | φ2.00            |  |  |
| Т             | 1.0 ± 0.10       |  |  |
| W             | $0.43\pm0.03$    |  |  |
| <u>Х</u><br>Ү | 2.55 MIN.        |  |  |
| Y             | 0.25 MAX.        |  |  |
| Z             | $1.50 \pm 0.10$  |  |  |
|               |                  |  |  |

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### 160 EDGE CONNECTOR PADS RIMM (SOCKET TYPE) (2/2)



| - |      |  |       |       |       |      |
|---|------|--|-------|-------|-------|------|
| _ | ITEM | DESCRIPTION  | MIN.  | TYP.  | MAX.  | UNIT |
|   | A1   | PCB length   | 67.45 | 67.60 | 67.75 | mm   |
| _ |      |  |       |       |       |      |
|   | В    | PCB height   | 31.10 | 31.25 | 31.40 | mm   |
| _ |      |  |       |       |       |      |
|   | С    | Center-center pad width from pad A1 to A40,            | -     | 25.35 | -     | mm   |
| _ |      | A41 to A80, B1 to B40 or B41 to B80                    |       |       |       |      |
|   | D    | Spacing from PCB left edge to connector key notch      | -     | 30.00 | -     | mm   |
|   |      |  |       |       |       |      |
|   | Е    | Spacing from contact pad PCB edge                      | -     | 20.00 | -     | mm   |
|   |      | to side edge retainer notch                            |       |       |       |      |
|   | F    | PCB thickness  | 0.90  | 1.00  | 1.10  | mm   |
|   |      |  |       |       |       |      |
| - | G    | Heat spreader thickness from PCB surface (one side) to | -     | 1.35  | -     | mm   |
|   |      | heat spreader top surface                              |       |       |       |      |
|   | Н    | RIMM thickness   | -     | 3.70  | -     | mm   |
|   |      |  |       |       |       |      |

ECA-TS2-0035-02

### CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

### - NOTES FOR CMOS DEVICES -

### **①** PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### **②** HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### **③** STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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