EM83010 I/O expander

I General Description

The EM83010 is a I/O expander with 14 bi-directional I/O pins and 144 bytes SRAM. Low power design permits operation down to 2.5 volts. R-option pins are used for chip addressing. Two wires serial interface is used to communicate with the master chip.

II Features

- Operating voltage range: 2.5V ~ 5.5V
- Available in temperature range: 0°C ~ 70°C
- 144 × 8 on chip RAM
- Two I/O registers, two I/O control registers
- Up to 14 bi-directional I/O pins
- Two wires serial interface
- Three R-options for chip addressing
- Up to 8 devices available on the same bus
- Low power consumption
- 18-pin DIP

III Pin Configurations

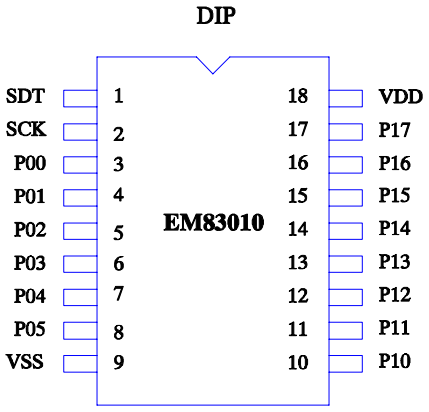


Fig. 1 Pin assignment

IV Functional Block Diagram

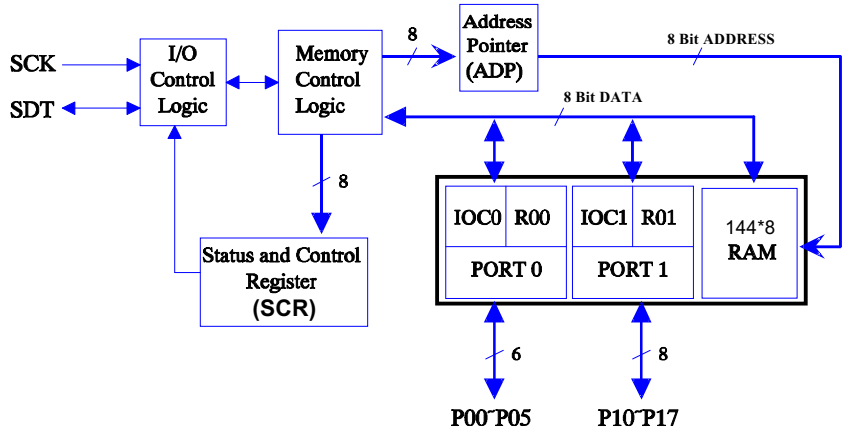


Fig. 2 Functional block diagram

V Pin Description

Symbol	Pin No.	Type	Function
SDT	1	I/O	This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore the SDT pin requires a pull-up resistor to VDD. It has the Schmitt trigger input.
SCK	2	I	Schmitt trigger input pin. This pin is used to synchronize the data transfer from and to the device.
P10~P17	10~17	I/O	P10~P17 are bi-directional I/O ports.
P00~P05	3~8	I/O	P00~P05 are bi-directional I/O ports. P00~P02 are also the R-option pins which are used for chip addressing.
VDD	18	-	Power supply pin.
VSS	9	-	Ground pin.

VI Function Description

VI.1 Serial Interface

1. Characteristic of Two Wire Bus

The EM83010 supports a bi-directional two wire serial bus for data transmission with master device. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generated serial clock (SCK) and the START and STOP conditions, while the EM83010 works as slave. Up to eight slave devices (EM83010s, or others) can be on the same bus.

The start of one transmission is the START signal , and then are the GRP bit and one byte DATA (Control Byte or Data or Address) and ACK bit , and the end of one transmission is a STOP. During the DATA transmission period, the most significant bit of one data byte is transmitted first.

First , each slave device on the bus has to receive the Control Byte data for addressing or setting the control register . Only the device which is addressed is allowed to receive/transmit other data (data and address in, and data out) on the bus. After the data transmission, the addressed slave/master device generates the ACK signal to acknowledge the master/slave device in WRITE mode. But user has to generate a ACK signal to EM83010 in READ mode.

The START is defined as a HIGH to LOW transition of the SDT line while the SCK line is HIGH. The STOP is defined as a LOW to HIGH transition of the SDT line while the SCK line is HIGH.

The first bit data after the START is not included into the 8-bit DATA and is named as GRP. If GRP is "0", the following byte are the Control Byte, otherwise the following are data (or address). The ACK (generated by master or slave device) is generated by pulling down the SDT line during the acknowledge clock pulse in such a way that SDT line is LOW during the HIGH period of the SCK clock pulse. **Note!! The ACK is not generated at the end of data transmission during the reading period for master device**.

After STOP condition being generated by the master device, the SCK and SDT lines are maintained HIGH continuously.

The Data transfer sequence on the serial bus is as follows:

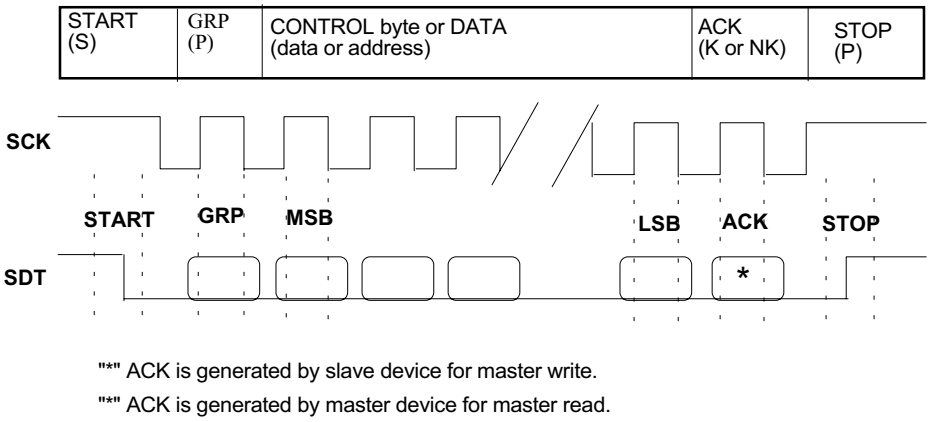
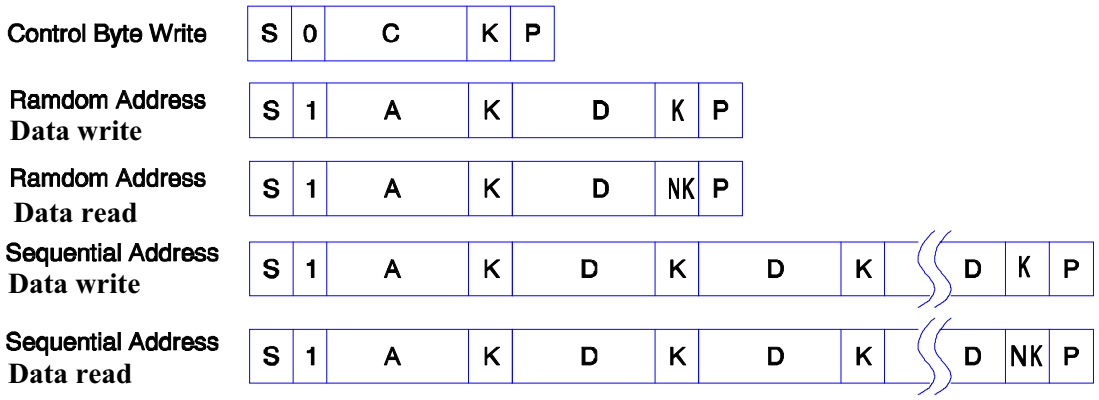


Fig. 3 Two wire serial interface

There are three kinds of data format defined on the serial bus. From the viewpoints of a master device, we list them as follow. Refer to Fig. 4.

(A) Send Control Byte to slave device.
(B) Random address Data Read/Write.
(C) Sequential address Data Read/Write.



Legend: S: START P: STOP D: Data (8 bits) 1: (GRP) One bit "HIGH"
A: Address (8 bits) K: Acknowledge 0 : (GRP) One bit "LOW"
C: Control Byte (8 bits) ***NK:High signal Acknowledg for master read***

Fig. 4 Data format on the bus

2. Control Byte

If the GRP bit after the START is "0", the following byte are the Control Byte and each slave device on the serial bus is obliged to receive the data. After receiving the Control Byte data, the addressed slave device will generate the acknowledge signal (ACK) .

7 (MSB)	6	5	4	3	2	1	0 (LSB)
T1	T0	A2	A1	A0	M1	M0	R/W

Bit	Name	Description
7 6	T1 T0*	T0~T1 are the Type Code. The (T1,T0) is (0,0) for an I/O expander. Each slave device on the bus has to compare T1~T0 with its internal Type code. If the compare is not true, the following transmission is neglected. The (T1,T0) is (1,1) for R-option check. And save the R-option address to status register (STS) RP2 to RP0.
5 4 3	A2* A1 A0	A0~A2 are defined as the Device Code. These three bits select which of the devices (up to eight devices) are to be accessed. The Device Code, A0~A2, are compared with the contents of bits 3~5 of Status register (STS) of slave device whose Type Code is (0,0), and the device is selected if the A2 to A0 compare is true.
2 1	M1 M0	Operating Mode selection. Except the Control Byte Write operation, there are four kinds of data format defined on the serial bus. These four modes are selected by M0~M1. After the Control Byte write operation, the data between the next START and STOP must be the format defined by M0~M1. (M1,M0): (0,0), Reserved (M1,M0): (0,1), Random address Data read/write. (M1,M0): (1,0), Sequential address Data read/write. (M1,M0): (1,1), Reserved The read/write operation is defined by R/W bit.
0	R/W	R/W bit defines the operation to be performed. R/W is loaded into bit 0 of the status register (STS) after Control Byte is received. When set to "1" a Read operation is selected, when set to "0" a Write operation is selected.

*** For the device which Type code is (1 1), it cannot have the device code (0 0 0). (T1 T0 A2 A1 A0) = (1 1 0 0 0) is reserved for R-option addressing. Refer to section on R-Option Addressing.**

VI.2 Registers (I/O Ports and RAM)

All registers described in this section are readable and writable. The RAM configuration is depicted in Fig. 5.

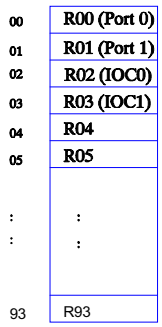


Fig. 5 RAM configuration

1. R00~R01 (Port 0 ~ Port 1)

- R00 is a 6-bit I/O register (Port 0). Writing to the upper two bits (bits 6~7) of R00 has no effect. The upper two bits will be read as "0"s.
- R01 is an 8-bit I/O register (Port 1).
- Each I/O pin can be defined as input or output pin.
- The equivalent circuit for a single I/O pin is shown in Fig. 6.
- Although data written to Port 0 or Port 1 are received serially, they are written into Port in one time. Similarly, data of Port are sampled at the same time while reading data on Port 0 or Port 1.

2. R02~R03 (IOC0 ~ IOC1)

- IOC0(R02) is a 6-bit I/O control register used to control the direction of I/O Port 0. Writing to the upper two bits (bits 6~7) of IOC0 has no effect. The upper two bits will be read as "0"s.
- IOC1(R03) is an 8-bit I/O control register used to control the direction of I/O Port 1.
- A "1" from a IOC0(IOC1) register bit puts the corresponding I/O pin into high impedance (input port) . A "0" from a IOC0(IOC1) register bit puts the corresponding I/O pin as output.
- **After power on, IOC0~IOC1 are set all "1"s.** That is, each I/O pin is configured as input pin (high impedance).
- Although data for IOC0 or IOC1 are received serially, they are written into register in one time.

3. R04~R93 (General Registers)

- R04~R93 are the 144 byte general registers (SRAM).

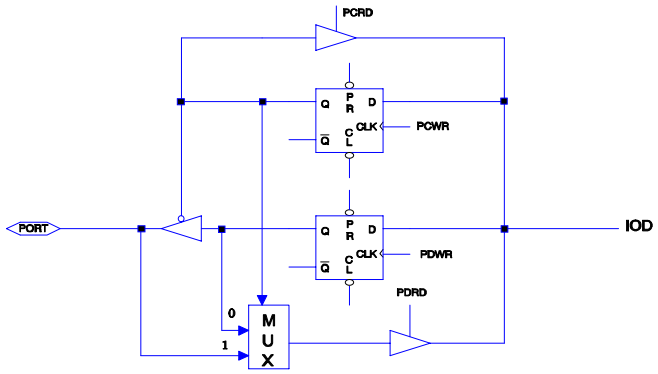


Fig. 6 The circuit of I/O pin and I/O control register

VI.3 R-Option initial Addressing (after Power-On each time)

Before the serial interface being performed between the devices on the bus, each slave device must has its address. That is, the R-option function is performed by the command resided in the Control byte from master device. If the code is (1 1 0 0 0 0 0 1) on the bus , all of the devices have to receive the "R-option read" command for reading the status of R-option pin.

P00~P02 are used as the R-option addressing pins. These pins are used to configure the proper chip address in multiple-chip applications (more than one EM83010 on the same bus). **Each R-option pin has weakly internal pull-high.** If one external resistor (approximately 560KΩ) is connected to one R-option pin, the associated pin will be read as "0" when the R-option is enabled. On the other hand, if no external resistor is connected to one R-option pin, the associated pin will be read as "1".

Note that **Because of R-option function, P00~P02 are recommended to be used as output pins**.

The "R-option read" command resided in Control Byte is listed below. Each slave device (no matter what its address is) on the bus has to perform the following function. Note that the Tpsu (STOP setup time) for "R-option read" command is longer than other STOP condition.

T1	T0	A 2	A 1	A 0	M1	M0	R/W	Function
1	1	0	0	0	0	0	1	Read R-option, clear ADP, set R02, R03
1	1	0	0	0	0	1	1	Reserved
1	1	0	0	0	1	x	1	Reserved
1	1	0	0	0	x	x	0	Reserved

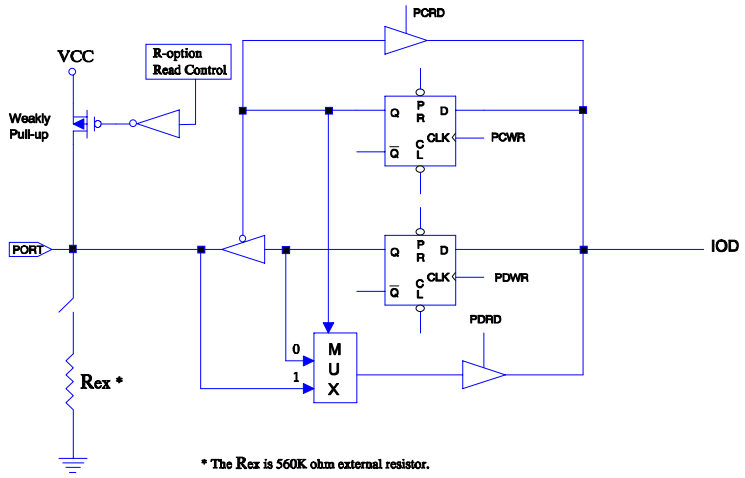


Fig. 7 The circuit of I/O pin with R-option (P00~P02)

VII Absolute Maximum Ratings

Temperature under bias	0°C	to	70°C
Storage temperature	-65°C	to	150°C
Input voltage	-0.3V	to	+6.0V
Output voltage	-0.3V	to	+6.0V

VIII DC Electrical Characteristic

(Ta=0°C~70°C, VDD=5.0V, VSS=0V)

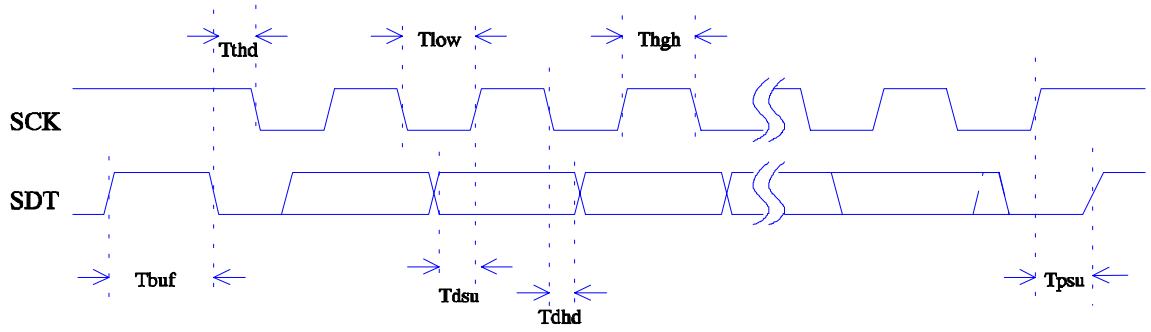
Symbol	Parameter	Condition	Min	Typ	Max	Unit
IIL	Input Leakage Current	VIN = VDD, VSS	-0.5		+0.5	μA
VIH1	Input High Voltage	I/O Ports	2.0	2.4		V
VIL1	Input Low Voltage	I/O Ports		0.4	0.8	V
VIH2	Input High Voltage	SCK, SDT	3.5			V
VIL2	Input Low Voltage	SCK, SDT			1.0	V
VOH	Output High Voltage	I/O Ports (IOH = -10.0mA)	2.4			V
VOL	Output Low Voltage	I/O Ports (IOL = 10.0mA)			0.4	V
ICC	Operating supply current	All input and I/O pins at VDD, output pin floating, SCK=500KHz			0.5	mA
ISB	Standby current	All input and I/O pins at VDD, output pin floating, SDT=SCK="High"			15	μA

IX AC Electrical Characteristic

(Ta=0°C~70°C, VDD=5V, VSS=0V)

Symbol	Parameter	Min	Typ	Max	Unit
Tclk	Clock frequency			500	KHz
Tlow	Clock Low period	1			µs
Thgh	Clock High period	1			µs
Tbuf	Free time before a new START	1			µs
Tthd	START hold time	1			µs
Tpsu	STOP setup time	1			µs
	STOP setup time for "R-option read" command resided in Control byte	500			µs
Tdhd	Data hold time	0			ns
Tdsu	Data setup time	200			ns

X Timing Diagrams



XI Application Circuit