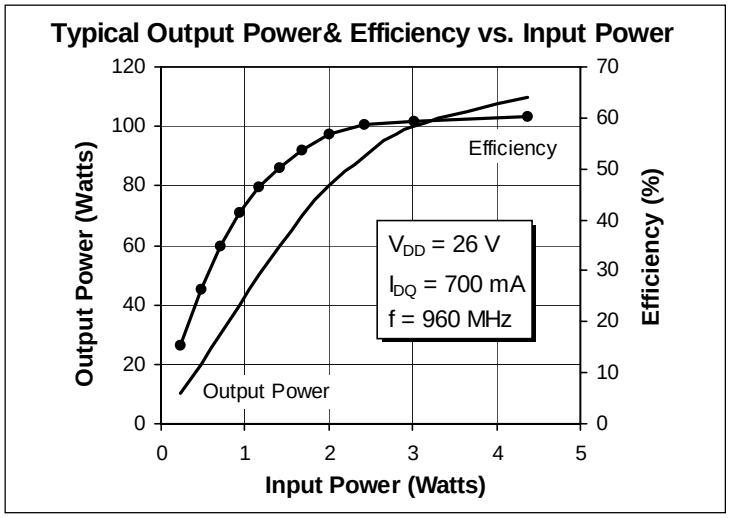
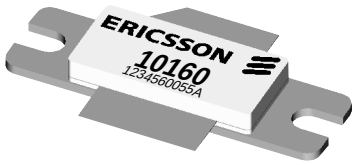
PTF 10160
85 Watts, 860–960 MHz
GOLDMOS® Field Effect Transistor

Description

The PTF 10160 is an internally matched 85–watt *GOLDMOS* FET intended for cellular, GSM, D-AMPS and EDGE applications. It operates with 53% efficiency and 16 dB typical gain. Full gold metallization ensures excellent device lifetime and reliability.

- ***INTERNALLY MATCHED***
- **Performance at 960 MHz, 26 Volts**
  - Output Power = 85 Watts
  - Power Gain = 16 dB Typ
  - Efficiency = 53% Typ
- **Full Gold Metallization**
- **Silicon Nitride Passivated**
- **Excellent Thermal Stability**
- **100% Lot Traceability**





Package 20248

RF Specifications (100% Tested)

Characteristic	Symbol	Min	Typ	Max	Units
Gain (V_{DD} = 26 V, P_{OUT} = 85 W, I_{DQ} = 700 mA, f = 960 MHz)	G_{pe}	15	16	—	dB
Power Output at 1 dB Compression (V_{DD} = 26 V, I_{DQ} = 700 mA, f = 960 MHz)	P-1dB	85	90	—	Watts
Drain Efficiency (V_{DD} = 26 V, P_{OUT} = 85 W, I_{DQ} = 700 mA, f = 960 MHz)	η	50	53	—	%
Load Mismatch Tolerance (V_{DD} = 26 V, P_{OUT} = 85 W, I_{DQ} = 700 mA, f = 960 MHz —all phase angles at frequency of test)	Ψ	—	—	5:1	—

All published data at T_{CASE} = 25°C unless otherwise indicated.

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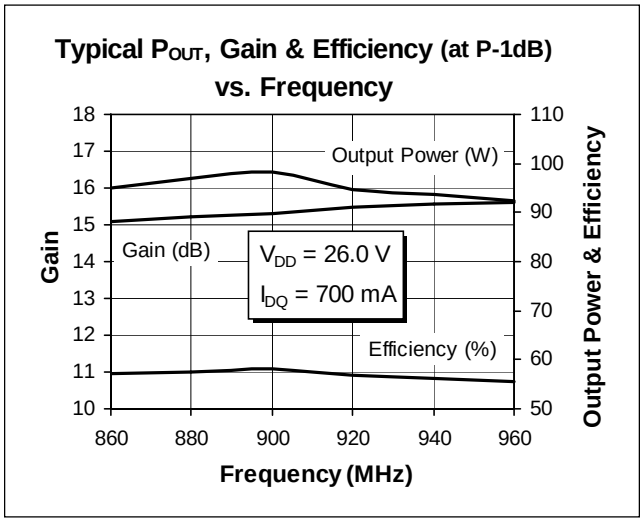
Electrical Characteristics (100% Tested)

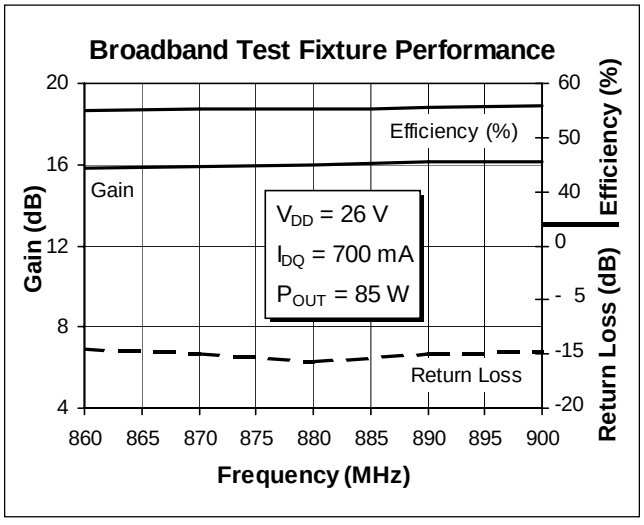
Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 25 mA	$V_{(BR)DSS}$	65	—	—	Volts
Drain-Source Leakage Current	V_{DS} = 26 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	mA
Gate Threshold Voltage	V_{DS} = 10 V, I_D = 75 mA	$V_{GS(th)}$	3.0	—	5.0	Volts
Forward Transconductance	V_{DS} = 10 V, I_D = 3 A	g_{fs}	—	3.0	—	Siemens

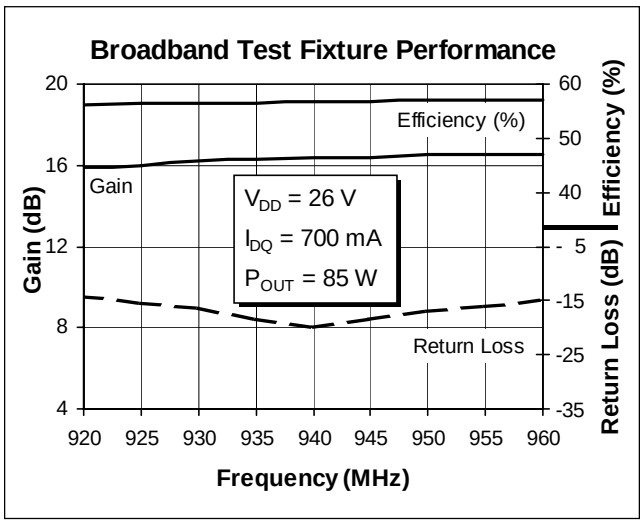
Maximum Ratings

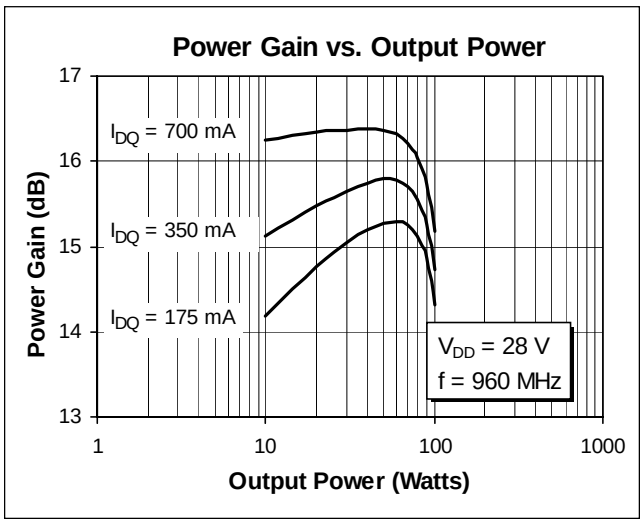
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Operating Junction Temperature	T_J	200	°C
Total Device Dissipation Above 25°C derate by	P_D	205 1.18	Watts W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.85	°C/W

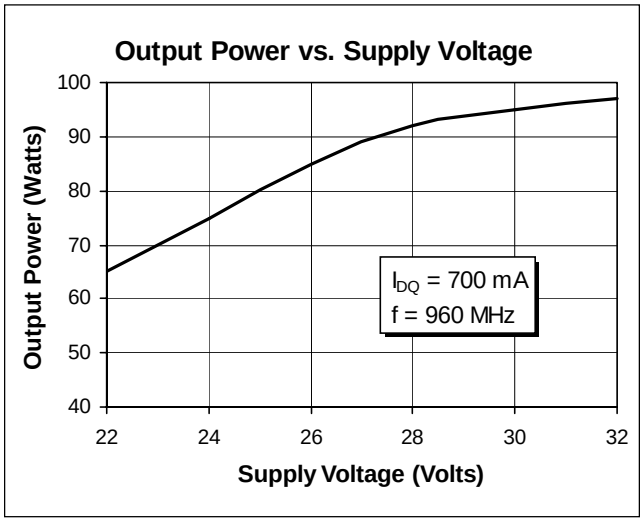
Typical Performance

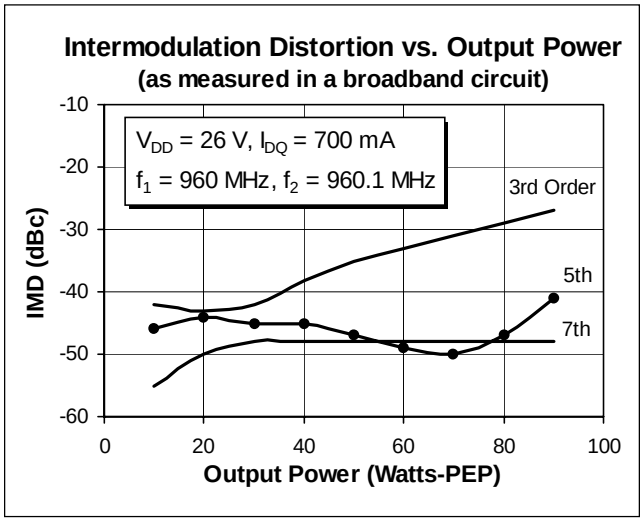


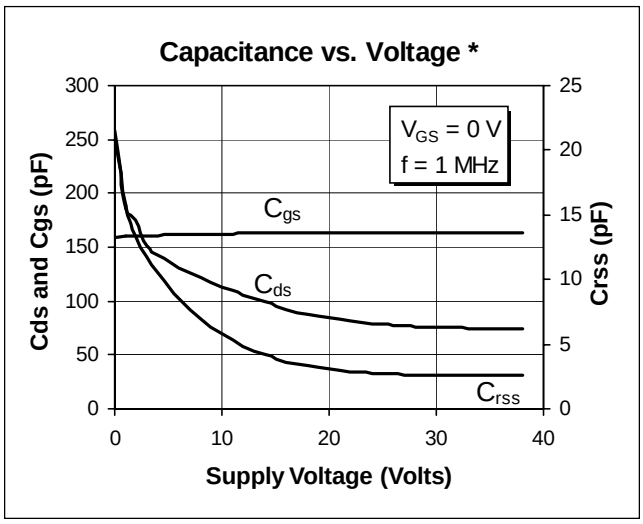


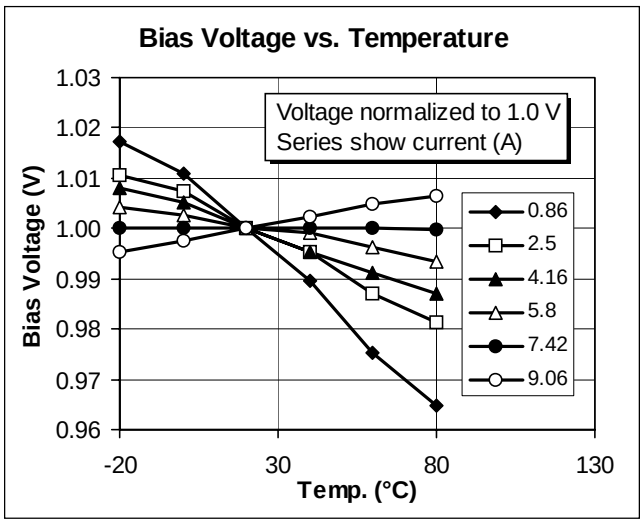






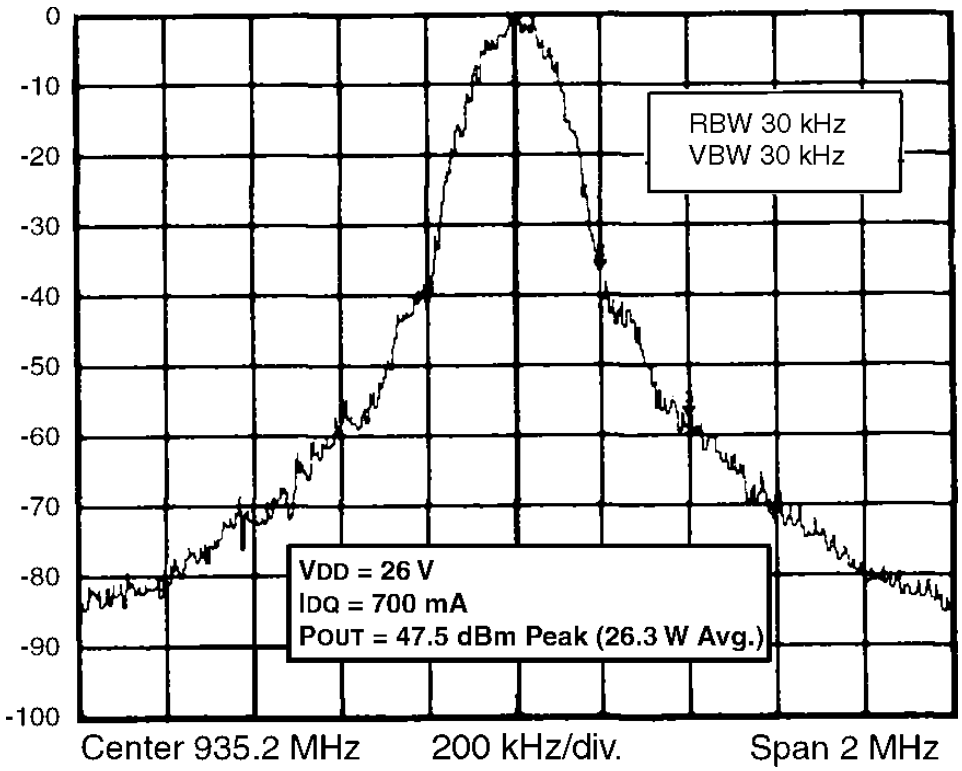






* This part is internally matched. Measurements of the finished product will not yield these figures.

Spectrum Due to Modulation (Edge Modulation)

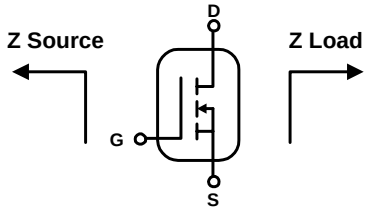


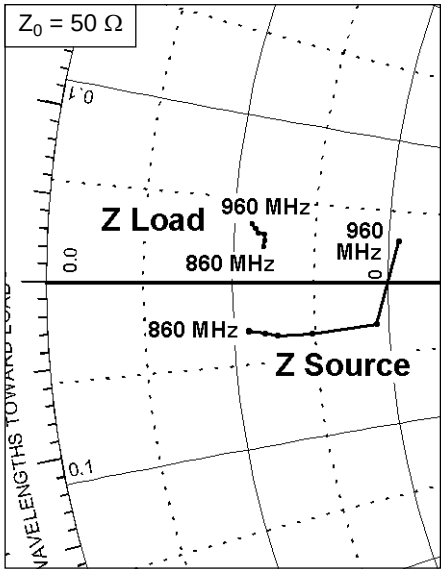
Without correction circuit

200 kHz = -36 dBc
400 kHz = -57 dBc
600 kHz = -70 dBc

Impedance Data

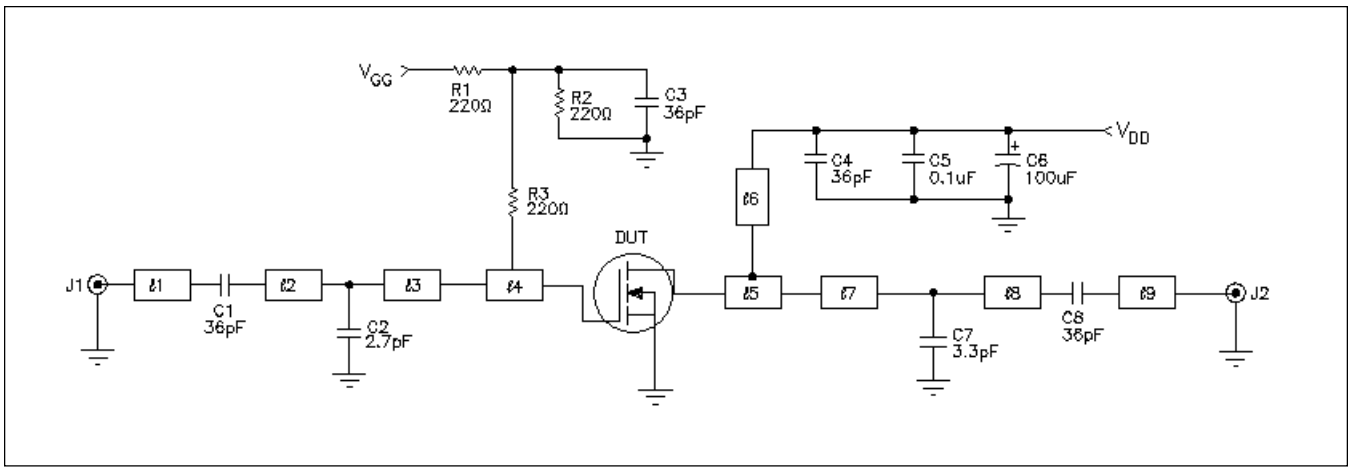
V_{DD} = 26 V, P_{OUT} = 85 W, I_{DQ} = 700 mA





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
860	2.1	-1.5	2.6	1.1
880	2.6	-1.6	2.6	1.3
900	3	-1.7	2.6	1.5
920	4.1	-1.7	2.4	1.5
940	6.3	-1.5	2.3	1.65
960	7.1	1.5	2.2	1.8

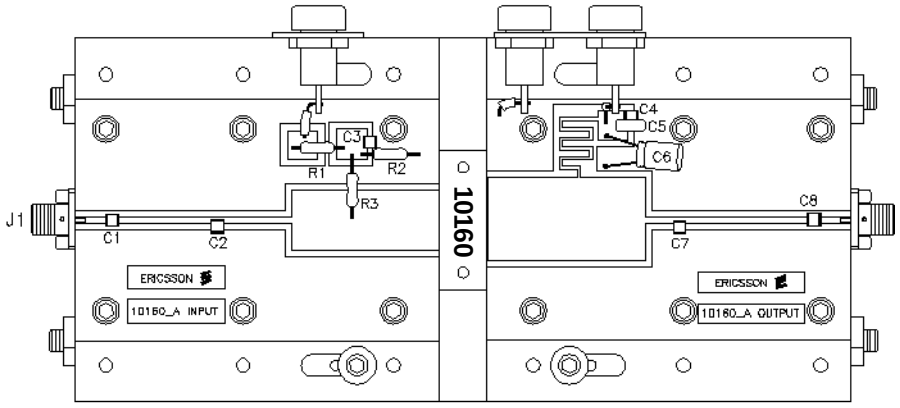
Test Circuit



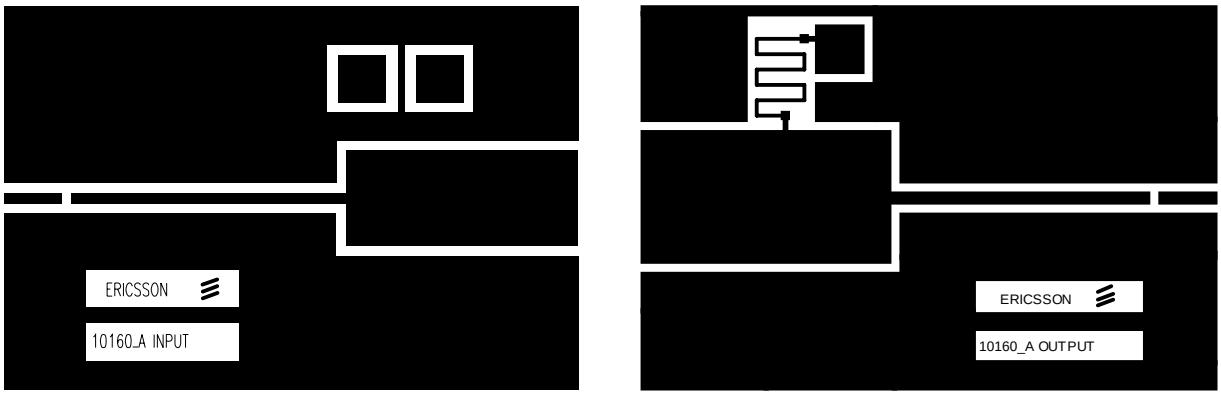
Test Circuit Schematic for f = 921 to 960 MHz

DUT	PTF 10160	LDMOS Transistor
ℓ1, ℓ9	0.037 λ	Microstrip 50 Ω
ℓ2	0.120 λ	Microstrip 50 Ω
ℓ3	0.080 λ	Microstrip 50 Ω
ℓ4	0.187 λ	Microstrip 9.29 Ω
ℓ5	0.204 λ	Microstrip 6.98 Ω
ℓ6	0.250 λ	Microstrip 77.9 Ω
ℓ7	0.031 λ	Microstrip 50 Ω
ℓ8	0.157 λ	Microstrip 50 Ω
ℓ1, ℓ9	0.037 λ	Microstrip 50 Ω

C1, C3, C4, C8	100 B	Capacitor, 36 pF
C2	100 B	Capacitor, 2.7 pF
C5	Digi-Key P4525-ND	Capacitor, 0.1 µF, 50 V
C6	Digi-Key P5182-ND	Capacitor, 100 µF, 50 V
C7	ATC 100 B	Capacitor, 3.3 pF
J1, J2	SMA Panel Mount Female Connector	
R1, R2, R3	220 Ω	Resistor, Digi-Key 1K QBK
Circuit Board	.031" Thickness, ε_r = 4.0, AlliedSignal, G200, 2 oz. copper	



Components Layout (not to scale)



Artwork (not to scale)

Case Outline Specifications

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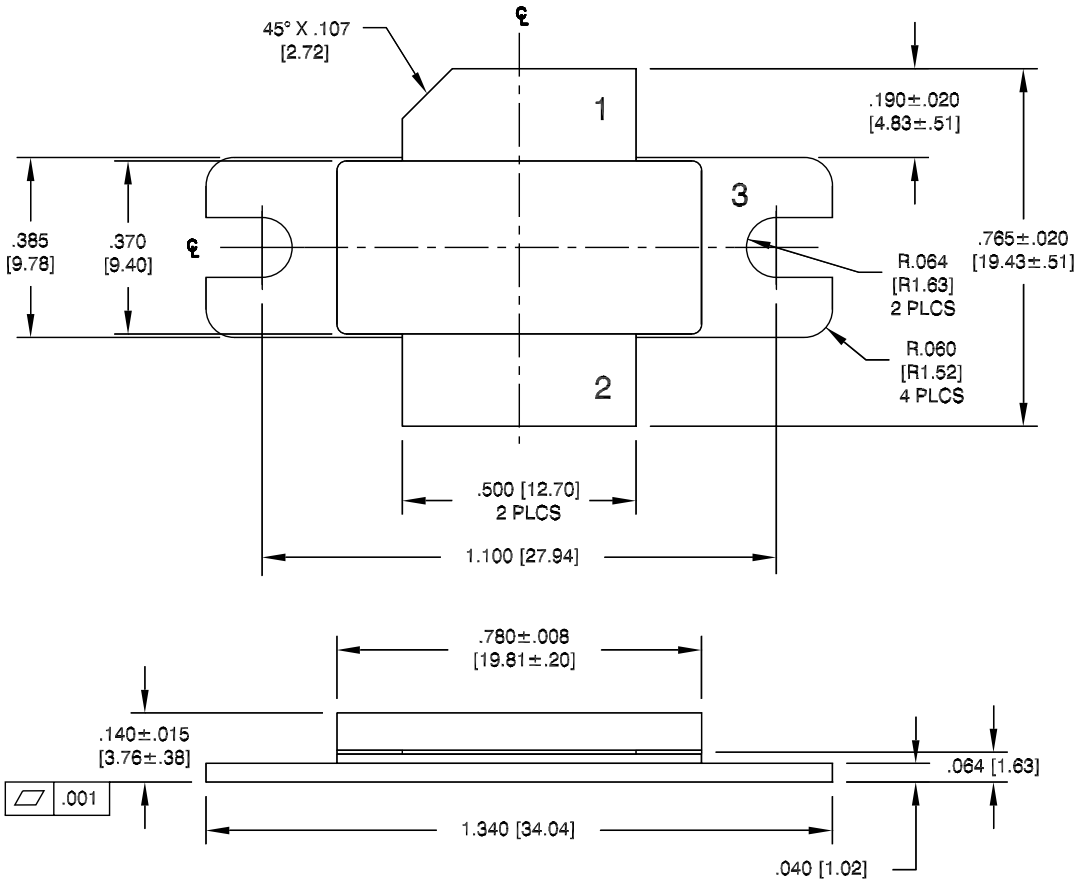

Unless otherwise specified
all tolerance ±0.005" [0.13mm]

Pins: 1. Drain 2. Gate 3. Source
Lead Thickness: 0.004 +0.002/-0.001"
[0.10 +.05/-0.03mm]

Primary dimensions are inches; alternate dimensions are mm.

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