ERICSSON

Preliminary

May 2000

PBL 386 65/2 Subscriber Line Interface Circuit

Description

The PBL 386 65/2 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in DLC, Central Office and other telecommunications equipment. The PBL 386 65/2 has been optimized for low total line interface cost and a high degree of flexibility in different applications.

The PBL 386 65/2 emulates a transformer equivalent dc-feed, programmable between 2x25 Ω and 2x900 Ω, with short loop current limiting adjustable to max 65 mA.

A second lower battery voltage may be connected to the device to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control.
The SLIC incorporates loop current, ground key and ring trip detection functions. The PBL 386 65/2 is compatible with loop start and ground start signalling.

Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, e.g. SLAC, SiCoFi, Combo II. The programmable line terminating impedance could be complex or real to fit every market.

Longitudinal line voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet the DLC requirements.

The PBL 386 65/2 package is 28-pin PLCC and 28-pin SSOP.

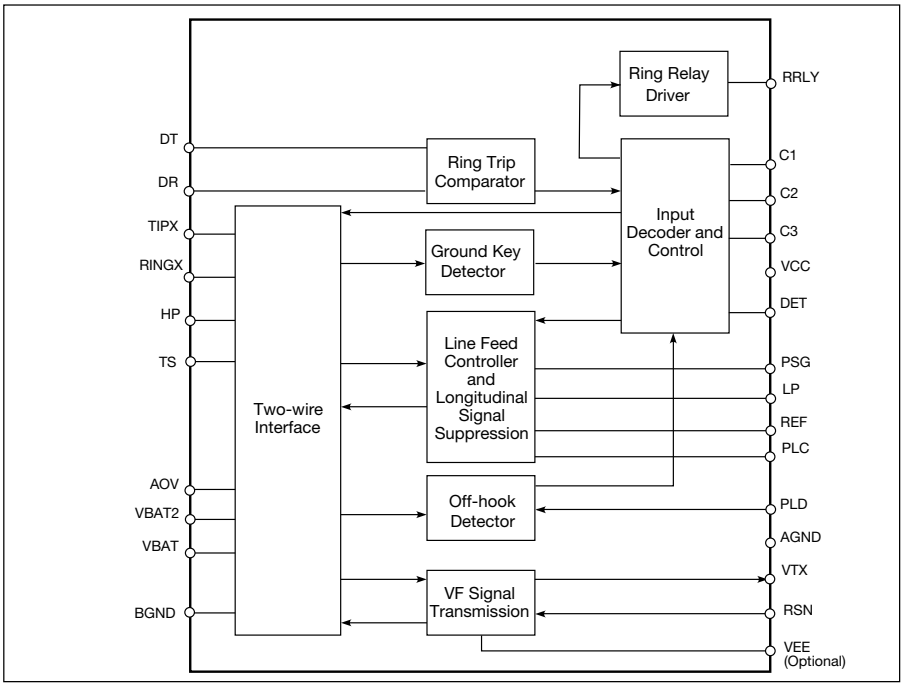
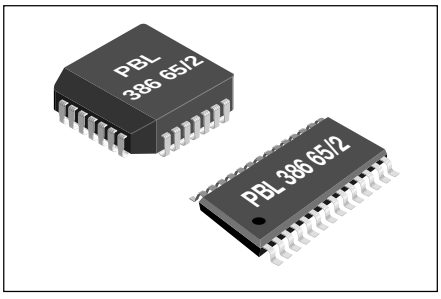


Figure 1. Block diagram.

Key Features

- Selectable overhead voltage principle
  – All adaptive: The overhead voltage follows $0.6_{Peak}V$ < signals < $6.2V_{Peak}$.
  – Semi adaptive: The overhead voltage follows $3.1V_{Peak}$ < signals < $6.2V_{Peak}$.
- Metering 2.2 V_{rms}
- High and low battery with automatic switching
- Battery supply as low as -10 V
- Only +5 V in addition to GND and battery (VEE optional)
- 39 mW on-hook power dissipation in active state
- Long loop battery feed tracks V_{Bat} for maximum line voltage
- 44V open loop voltage @ -48V battery feed
- Constant loop voltage for line leakage <5 mA
- On-hook transmission
- Full longitudinal current capability during on-hook
- Programmable loop & ring-trip detector threshold
- Ground key detector
- Analog temperature guard
- Tip open state with ring ground detector
- Silent polarity reversal
- Line voltage measurement
- -40° C to +85° C ambient temperature range



28-pin PLCC and 28-pin SSOP.

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating temperature range	T_{Amb}	-40	+110	°C
Operating junction temperature range, Note 1	T_J	-40	+140	°C
Power supply, -40°C ≤ T_{Amb} ≤ +85°C				
V_{CC} with respect to A/BGND	V_{CC}	-0.4	6.5	V
V_{EE} with respect to A/BGND	V_{EE}	V_{Bat}	0.4	V
V_{Bat} with respect to A/BGND, continuous	V_{Bat}	-75	0.4	V
V_{Bat} with respect to A/BGND, 10 ms	V_{Bat}	-80	0.4	V
V_{Bat2} with respect to A/BGND	V_{Bat2}	V_{Bat}	0.4	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ +85 °C	P_D		1.5	W
Ground				
Voltage between AGND and BGND	V_G	-5	VCC	V
Relay Driver				
Ring relay supply voltage			BGND +13	V
Ring relay current			75 mA	
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	V_{CC}	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, C3, DET)				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (DET not active)	V_{OD}	-0.4	V_{CC}	V
Output current (DET)	I_{OD}		30	mA
TIPX and RINGX terminals, -40°C < T_{Amb} < +85°C, V_{Bat} = -50V				
Maximum supplied TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-110	+110	mA
TIPX or RINGX voltage, continuous (referenced to AGND), Note 2	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 20	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 40	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 3	V_{TA}, V_{RA}	V_{Bat} - 70	15	V

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	V_{Bat}	-4.75	V
V_{Bat} with respect to BGND	V_{Bat}	-58	-10	V
V_{Bat2} with respect to BGND		V_{Bat}	-10	V

Notes

1. The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.
2. A diode in series with the VBat input increases the permitted continuous voltage and pulse < 10 ms to -85 V. A pulse ≤1µs is increased to the greater of |-70V| and |VBat -40V|.
3. R_{F1}, F_{R2} ≥20 Ω is also required. Pulse is supplied to TIP and RING outside R_{F1}, F_{R2}.

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ +85 °C, V_{CC} = +5V ±5 %, V_{EE} = -5V ± 5%, V_{Bat} = -58V to -40V, R_{LC}=18.7kΩ, I_L = 27 mA, Z_L = 600 Ω, R_{F1}, R_{F2} =0 Ω, R_{Ref} = 15kΩ, C_{HP} = 68nF, C_{LP}=0.33 µF, R_T = 120 kΩ, R_{SG} = 24 kΩ, R_{RX} = 120 kΩ, AOV- and V_{Bat2} pin not connected, unless otherwise specified. Current definition: current is positive if flowing into a pin.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO} ,I_{LDC} ≥ 10 mA	2	Active state				
		1% THD, Note 1	3.1			V_{Peak}
On-Hook, I_{LDC} ≤ 5 mA			1.4			V_{Peak}
Input impedance, Z_{TR}		Note 2		Z_T/200		
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state	28			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}	3	IEEE standard 455-1985, Z_{TRX}=736Ω, active state				
		Normal polarity:				
		0.2 kHz < f < 1.0 kHz, T_{amb} 0-70°C	63			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} 0-70°C	58			dB
		0.2 kHz < f < 1.0 kHz, T_{amb} -40-85°C	58			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} -40-85°C	54			dB
		Reverse polarity:				
		0.2 kHz < f < 3.4 kHz, T_{amb} -40-85°C	54			dB
Longitudinal to metallic balance, B_{LME}	3	Active state				
		Normal polarity:				
		0.2 kHz < f < 1.0 kHz, T_{amb} 0-70°C	63			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} 0-70°C	58			dB
$B_{LME} = 20 \bullet Log \left\lvert \frac{E_{LO}}{V_{TR}} \right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz, T_{amb} -40-85°C	58			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} -40-85°C	54			dB
		Reverse polarity:				
		0.2 kHz < f < 3.4 kHz, T_{amb} -40-85°C	54			dB
Longitudinal to four-wire balance, B_{LFE}	3	Active state				
		Normal polarity:				
		0.2 kHz < f < 1.0 kHz, T_{amb} 0-70°C	69			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} 0-70°C	64			dB
$B_{LFE} = 20 \bullet Log \left\lvert \frac{E_{LO}}{V_{TX}} \right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz, T_{amb} -40-85°C	64			dB
		1.0 kHz < f < 3.4 kHz, T_{amb} -40-85°C	60			dB
		Reverse polarity:				
		0.2 kHz < f < 3.4 kHz, T_{amb} -40-85°C	54			dB
Metallic to longitudinal balance, B_{MLE}	4	Active state				
		0.2 kHz < f < 3.4kHz	40			dB
$B_{MLE} = 20 \bullet Log \left\lvert \frac{V_{TR}}{V_{LO}} \right\rvert$						

Figure 2. Overload level, V_{TRO}, two-wire port

$\frac{1}{\omega C}$ << R_L, R_L= 600 Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

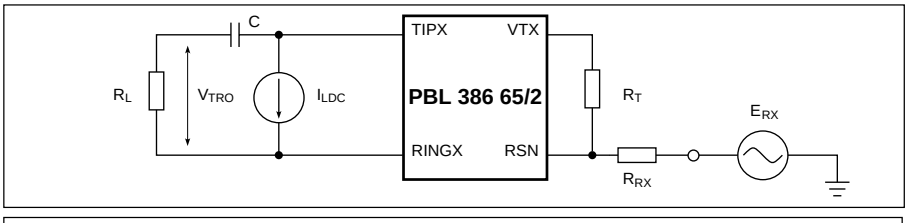
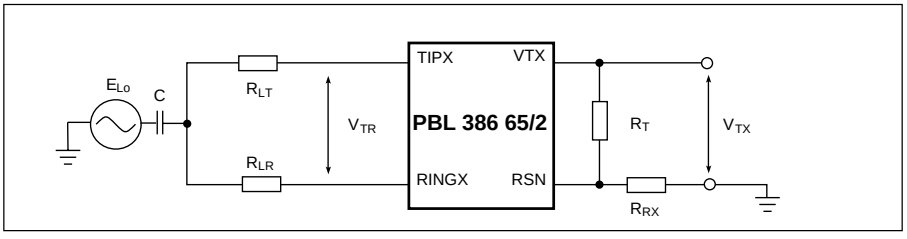


Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

$\frac{1}{\omega C}$ << 150 Ω, R_{LR} = R_{LT} = R_L /2= 300Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	Active state $B_{FLE} = 20 \bullet Log\left\lvert\frac{E_{RX}}{V_{Lo}}\right\rvert$				
		0.2 kHz < f < 3.4 kHz	40			dB
Two-wire return loss, r		$r = 20 \bullet Log \frac{\lvert Z_{TR} + Z_L\rvert}{\lvert Z_{TR} - Z_L\rvert}$				
		0.2 kHz < f < 0.5 kHz	25			dB
		0.5 kHz < f < 1.0 kHz	27			dB
		1.0 kHz < f < 3.4 kHz, Note 3	23			dB
TIPX idle voltage, V_{Ti}		active, I_L < 5 mA		- 1.5		V
RINGX idle voltage, V_{Ri}		active, I_L < 5 mA		V_{Bat} + 2.7		V
RINGX idle voltage, V_{Ri}		tip open, I_L < 5 mA		V_{Bat} + 3.0		V
V_{TR}		active, I_L < 5 mA		V_{Bat} +4.2		V
Four-wire transmit port (VTX)						
Overload level, V_{TXO}, $I_L \geq 10$ mA	5	Load impedance > 20 kΩ,	1.55			V_{Peak}
On hook $I_L \leq 5$ mA		1% THD, Note 4	0.7			V_{Peak}
Output offset voltage, ΔV_{TX}			-60		60	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		5	20	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0 mA	-25	GND	+25	mV
Receive summing node (RSN) impedance		0.2 kHz < f < 3.4 kHz		10	50	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 kHz < f < 3.4 kHz		400		ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	6	relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8.0 kHz, 12 kHz, 16 kHz	-0.5	0	+0.1	dB

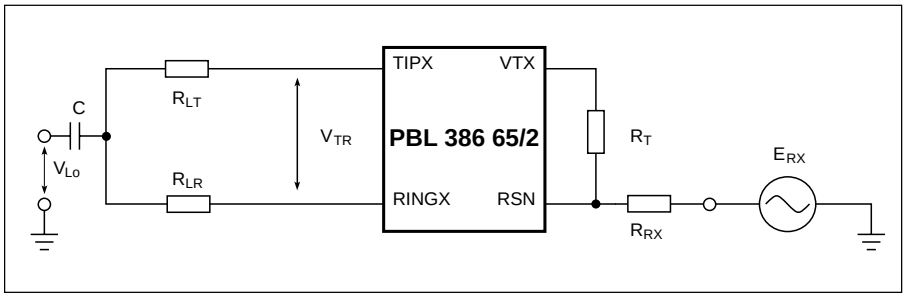


Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C}$ << 150 Ω, $R_{LT} = R_{LR} = R_L / 2 = 300\Omega$

R_T = 120 kΩ, R_{RX} = 120 kΩ

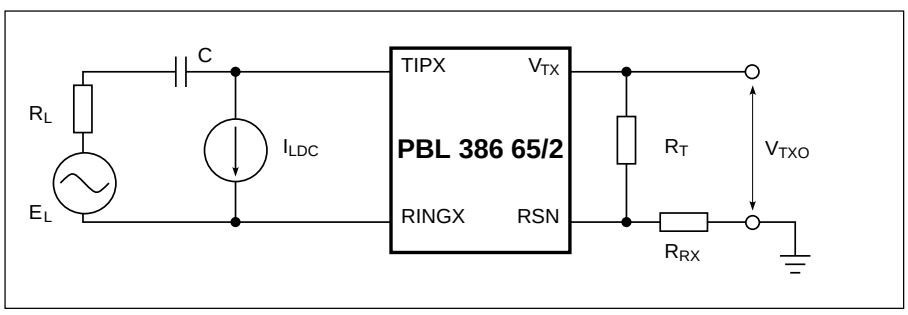


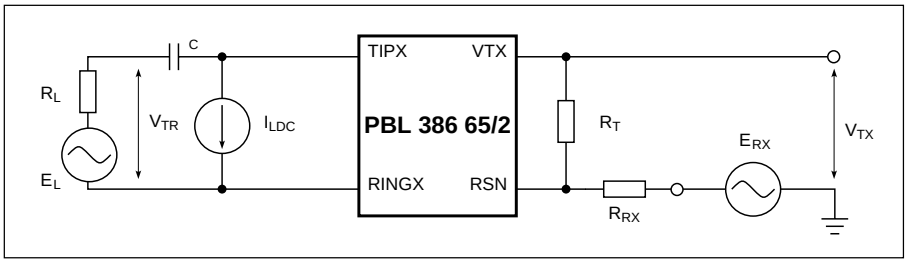
Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C}$ << R_L, R_L = 600 Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to two-wire, g_{4-2}	6	relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8 kHz, 12 kHz,	-1.0	-0.2	0	dB
		16 kHz	-1.0	-0.3	0	dB
Four-wire to four-wire, g_{4-4}	6	relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5				
		$G_{2-4} = 20 \bullet \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert, E_{RX} = 0$	-6.22	-6.02	-5.82	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 5, 6				
		$G_{4-2} = 20 \bullet \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert, E_L = 0$	-0.2		0.2	dB
Gain tracking						
Two-wire to four-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire		C-message weighting		7	12	dBrnC
(TIPX-RINGX)		Psophometrical weighting Note 8		-83	-78	dBmp
Harmonic distortion						
Two-wire to four-wire	6	0 dBm, 1.0 kHz test signal			-50	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz			-50	dB
Battery feed characteristics						
Constant loop current, I_{Lconst}	15	$I_{LProg} = \frac{500}{R_{LC}}$				
		18 < I_{LProg} < 65 mA	0.92 I_{LProg}	I_{LProg}	1.08 I_{LProg}	mA
Tip open state TIPX current, I_{Leak}	7	S = closed; R = 7 kΩ			-100	µA
Tip open state RINGX current, I_{LRTO}	7	R_{LRTO} = 0Ω, V_{Bat} = -48V		I_L		mA
		R_{LRTO} = 2.5 kΩ, V_{Bat} = -48V		17		mA
Tip open state RINGX voltage, V_{RTO}	7	I_{LRTO} < 23 mA		V_{Bat}+ 5.8		V
Tip voltage (ground start)	7	Active state, Tip lead open (S open), Ring lead to ground through 150 Ω	-4	-2.5	-	V
Tip voltage (ground start)	7	Active state, tip lead to -48 V through 7 kΩ (S closed), Ring lead to ground through 150 Ω	-6	-3.1	-	V
Open circuit state loop current, I_{LOC}		R_L = 0Ω	-100	0	100	µA

Figure 6.
Frequency response, insertion loss, gain tracking.



$\frac{1}{\omega C} << R_L$, R_L = 600 Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Loop current detector						
Programmable threshold, I_{DET}		$I_{LTh} = \frac{500}{R_{LD}}$	$0.9 \cdot I_{LTh}$	I_{LTh}	$1.1 \cdot I_{LTh}$	mA
Progammable threshold in Tip Open state, I_{DET}		$I_{LTh} = \frac{500}{R_{LD}}$	$0.9 \cdot I_{LTh}$	I_{LTh}	$1.1 \cdot I_{LTh}$	mA
Ground key detector						
Ground key detector threshold (I_{LTIPX} and I_{LRINGX} current differance to trigger ground key det.)			11	15	19	mA
Line voltage measurement						
Frequency		$f = \frac{10^6}{\lvert V\rvert_{TR}+1}$		f		Hz
Ring trip comparator						
Offset voltage, ΔV_{DTDR}		Source resistance, R_S = 0 Ω	-20	0	20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-50	-20	200	nA
Input common mode range, V_{DT}, V_{DR}			V_{Bat}+1		-1	V
Ring relay driver						
Saturation voltage, V_{OL}		I_{OL} = 50 mA			0.5	V
Off state leakage current, I_{Lk}		V_{OH} = 12 V			100	µA
Digital inputs (C1, C2, C3)						
Input low voltage, V_{IL}			0		0.5	V
Input high voltage, V_{IH}			2.5		V_{CC}	V
Input low current, I_{IL}		V_{IL} = 0.5			-200	µA
Input high current, I_{IH}		V_{IH} = 2.5 V			200	µA
Detector output (DET)						
Output low current, I_{OL}		V_{OL} < 0.6V	0.5	1		mA
Internal pull-up resistor				10		kΩ
Power dissipation (V_{Bat} = -48V; V_{Bat2} = -32V)						
P_1		Open circuit state		14		mW
P_2 @ VEE=-5V		Active state I_{Lo} = 0 mA, I_L = 0 mA		39		mW
P_3 @ VEE=-48V		Active state I_{Lo} = 0 mA, I_L = 0 mA		44		mW
P_4 @ VEE=-5V		Active state R_L = 300Ω (off-hook)		710		mW
P_5 @ VEE=-5V		Active state R_L = 800Ω (off-hook)		340		mW
Power supply currents (V_{Bat} = -48V)						
V_{CC} current, I_{CC}		Open circuit state		0.8		mA
V_{EE} current, I_{EE}		Open circuit state		-0.15		mA
V_{Bat} current, I_{Bat}		Open circuit state		-0.2		mA
V_{CC} current, I_{CC}		Active state I_{Lo}= 0 mA, I_L = 0 mA		2.0		mA
V_{EE} current, I_{EE}		Active state I_{Lo}= 0 mA, I_L = 0 mA		-0.15		mA
V_{Bat} current, I_{Bat}		Active state I_{Lo}= 0 mA, I_L = 0 mA		-0.7		mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active state, f = 1 kHz, V_n = 100mV	28.5	35		dB
V_{EE} to 2- or 4-wire port		Active state, f = 1 kHz, V_n = 100mV	28.5	55		dB
V_{Bat} to 2- or 4-wire port		Active state, f = 1 kHz, V_n = 100mV	28.5	40		dB
V_{Bat2} to 2- or 4-wire port		Active state, f = 1 kHz, V_n = 100mV	28.5	60		dB
Temperature guard						
Junction threshold temperature, T_{JG}			140			°C
Thermal resistance						
28-pin PLCC, $\theta_{JP28PLCC}$				39		°C/W
28-pin SSOP, $\theta_{JP28SSOP}$				55		°C/W

Notes

1. The overload level is automatically expanded when the signal level > 3.1 V_{Peak} and is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TR} = Z_T/|G_{2\text{-}4S}\,\alpha_{RSN}|$ where:
   Z_{TR} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the V_{TX} and RSN terminals
   $G_{2\text{-}4S}$ = transmit gain, nominally = 0.5
   α_{RSN} = receive current gain, nominally = 400 (current defined as positive flowing into the receivesumming node, RSN, and when flowing from tip to ring).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.
4. The overload level is automatically expanded, as needed up to 3.1 V_{Peak} when the signal level >1.55 V_{Peak} and is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S}$ = 0.5.
5. Secondary protection resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for R_F = 0.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the four-wire receive port and referenced to a 600 Ω programmed two-wire impedance level.
8. The two-wire idle noise is specified with the four-wire receive port grounded (E_{RX} = 0; see figure 6).
   The four-wire idle noise at VTX is the two-wire value -6 dB and is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω programmed two-wire impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).

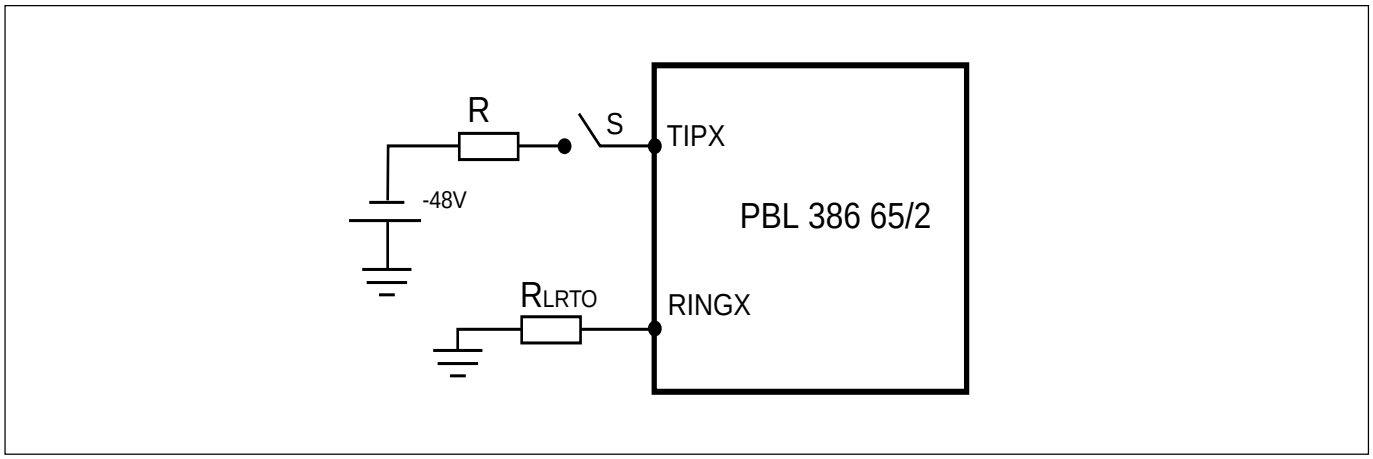


Figure 7. Tipx voltage.

Pin Description

Refer to figure 8.

PLCC	SSOP	Symbol	Description
1	7	VBAT	Battery supply voltage. Negative with respect to BGND.
2	8	VBAT2	An optional second battery voltage, connected in series with a diode, or an external powerhandling resistor connects to this pin.
3	9	AOV	**A**daptive **O**verhead **V**oltage. If the pin is left open, then the overhead voltage is set internally to 3.1V_{Peak} in off-hook and 1.4 V_{Peak} in on-hook. The overhead voltage will automatically adapt to signals > 3.1V_{Peak}. If the pin is connected to AGND, then no overhead voltage is set internally. The overhead voltage adapts automatically to 0.6 V_{Peak} < signals < 6.2 V_{Peak}.
4	10	PSG	**P**rogrammable **S**aturation **G**uard. The resistive part of the DC feed characteristic is programmed by a resistor connected from this pin to VBAT.
5	11	LP	**L**ow **P**ass filter. Saturation guard filter capacitor connected here to filter out noise and improve PSRR. Other end of C_{LP} connects to VBAT.
6	12	DT	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The ring trip network connects to this input.
7	13	DR	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The ring trip network connects to this input.
8	16	VEE	-5V to VBAT power supply.
9	17	REF	A 15 kΩ resistor should be connected between this pin and AGND.
10	18	SPR	**S**ilent **P**olarity **R**eversal. The polarity reversal time can be adjusted with a capacitor connected to AGND. If pin is left open: Shortest polarity reversal time.
11	19	PLC	**P**rog. **L**ine **C**urrent, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
12	20	PLD	**P**rogrammable **L**oop **D**etector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
13	21	VCC	+5 V power supply.
14	22	C3	C1, C2 and C3 are digital inputs **C**ontrolling the SLIC operating states. Refer to section Operating states for details.
15	23	C2	
16	24	C1	
17	14	NC	**N**o **C**onnect. Must be left open.
18	25	DET	**Det**ector output. Active low when indicating loop or ring trip detection, active high when indicating ground key detection
19	26	RSN	**R**eceive **S**umming **N**ode. 400 times the current flowing into this pin equals the metallic (transversal) current flowing from RINGX to TIPX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
20	27	AGND	**A**nalog **G**rou**nd**, should be tied together with BGND.
21	28	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of -0.5. The two-wire impedance programming network connects between VTX and RSN.
22	1	RRLY	**R**ing **R**e**l**a**y** driver output.
23	2	TS	**T**ip **S**ense should be connected to TIPX.
24	15	NC	**N**o **C**onnect. Must be left open.
25	3	HP	**H**igh **P**ass connection for ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to RINGX.
26	4	RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
27	5	BGND	**B**attery **G**rou**nd**, should be tied together with AGND.
28	6	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).

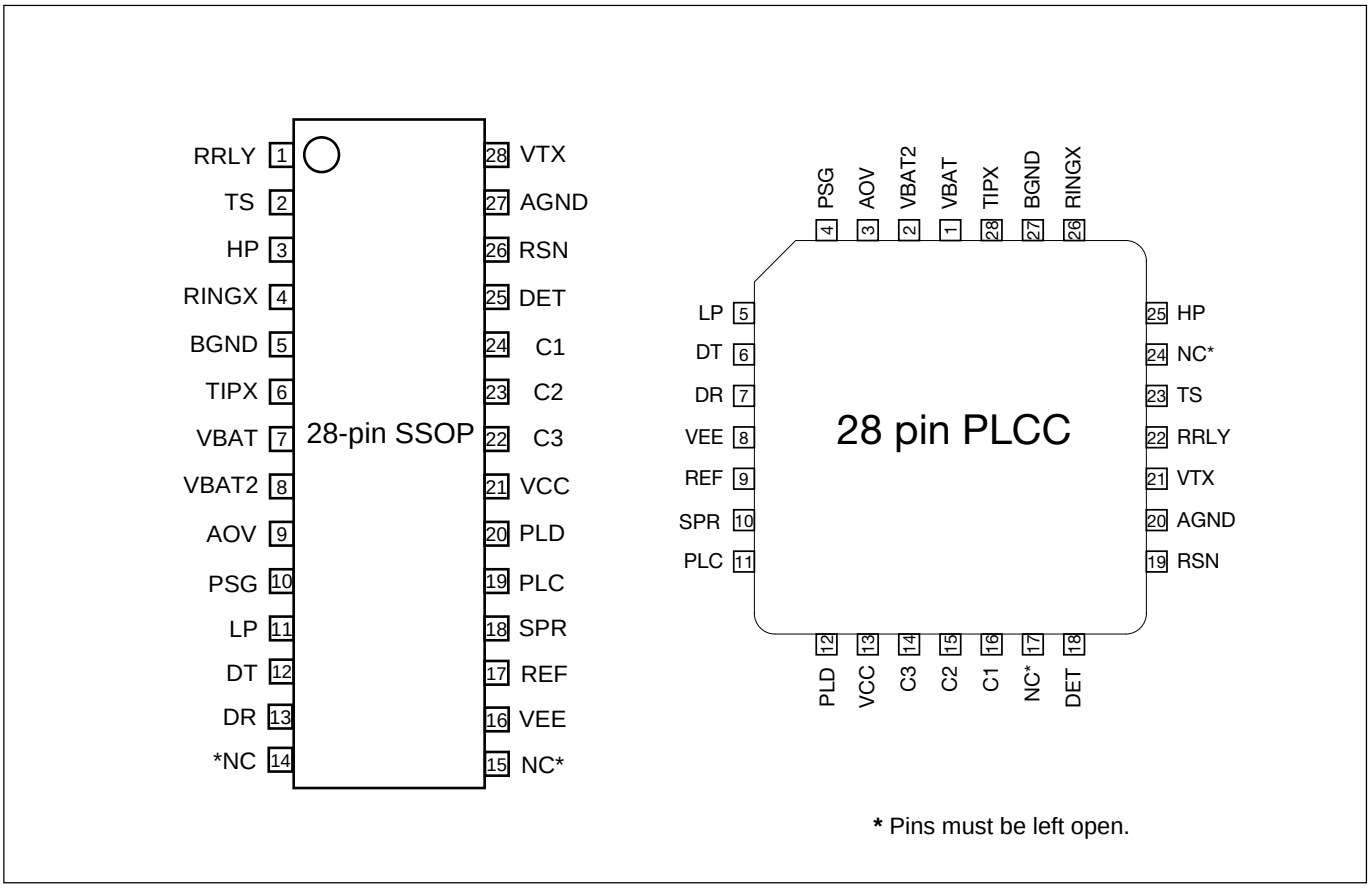


Figure 8. Pin configuration 28 pin SSOP and 28 pin package, top view.

SLIC Operating States

State	C3	C2	C1	SLIC operating state	Active detector
0	0	0	0	Open circuit	Detector is set high
1	0	0	1	Ringing state	Ring trip detector (active low)
2	0	1	0	Active state	Loop detector (active low)
3	0	1	1	Active state	Line voltage measurement
4	1	0	0	Tip open state	Loop detector (active low)
5	1	0	1	Active state	Ground key detector (active high)
6	1	1	0	Active reverse	Loop detector (active low)
7	1	1	1	Active reverse	Ground key detector (active high)

Table 1. SLIC operating states.

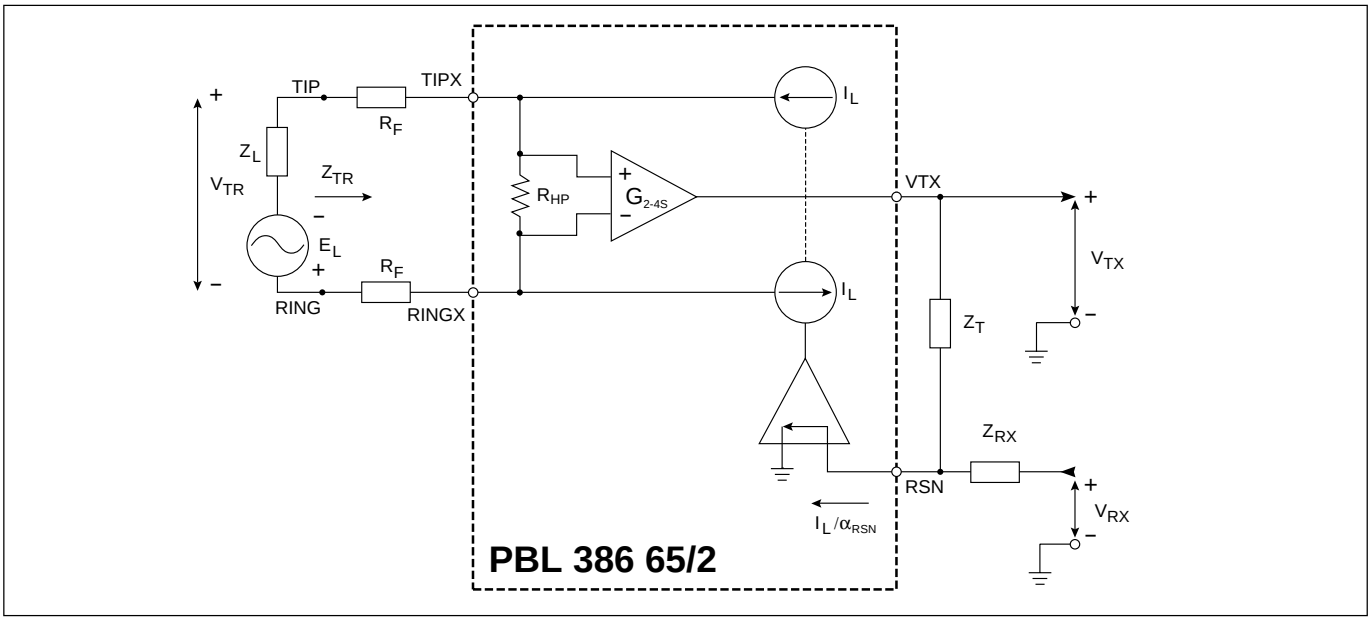


Figure 9. Simplified ac transmission circuit.

Functional Description and Applications Information Transmission

General

A simplified ac model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = \frac{V_{TX}}{G_{2-4S}} - I_L \cdot 2R_F \qquad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{\alpha_{RSN}} \qquad (2)$$

$$V_{TR} = I_L \cdot Z_L - E_L \qquad (3)$$

where:

- V_{TX} is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_L is the line open circuit ac metallic voltage.
- I_L is the ac metallic current.
- R_F is a fuse resistor.
- G_{2-4S} is the SLIC two-wire to four-wire gain (transmit direction) with a nominal value of -0.5. (Phase shift 180°)
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance for signal in the 0 - 20kHz frequency range.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analogue ground referenced receive signal.
- α_{RSN} is the receive summing node current to metallic loop current gain. The nominal value of α_{RSN}=400

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistor R_F, let V_{RX} = 0.

From (1) and (2):

$$Z_{TR} = \left| \frac{Z_T}{\alpha_{RSN} \cdot G_{2-4S}} - 2R_F \right|$$

Thus with Z_{TR}, G_{2-4S}, α_{RSN}, and R_F known:

$$Z_T = \alpha_{RSN} \cdot G_{2-4S} \cdot (2R_F - |Z_{TR}|)$$

Two-Wire to Four-Wire Gain

From (1) and (2) with V_{RX} = 0:

$$G_{2-4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/\alpha_{RSN}}{\frac{Z_T}{\alpha_{RSN} \cdot G_{2-4S}} - 2R_F}$$

Four-Wire to Two-Wire Gain

From (1), (2) and (3) with E_L = 0:

$$G_{4-2} = \frac{V_{TR}}{V_{RX}} = \frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{\frac{Z_T}{\alpha_{RSN}} - G_{2-4S} \cdot (Z_L + 2R_F)}$$

In applications where $2R_F - Z_T/(\alpha_{RSN} \cdot G_{2-4S})$ is chosen to be equal to Z_L, the expression for G_{4-2} simplifies to:

$$G_{4-2} = -\frac{Z_T}{Z_{RX}} \cdot \frac{1}{2 \cdot G_{2-4S}}$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with E_L = 0:

$$G_{4-4} = \frac{V_{TX}}{V_{RX}} = \frac{Z_T}{Z_{RX}} \cdot \frac{G_{2-4S} \cdot (Z_L + 2R_F)}{\frac{Z_T}{\alpha_{RSN}} - G_{2-4S} \cdot (Z_L + 2R_F)}$$

Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \ (E_L = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = - R_{TX} \cdot \frac{V_{RX}}{V_{TX}} =$$

$$- R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{\frac{Z_T}{\alpha_{RSN}} - G_{2\text{-}4S} \cdot (Z_L + 2R_F)}{G_{2\text{-}4S} \cdot (Z_L + 2R_F)}$$

When choosing R_{TX}, make sure the output load of the VTX terminal is > 20 kΩ.

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended.

The PBL 386 65/2 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase.

Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LoT} and Z_{LoR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission.

Capacitors C_{TC} and C_{RC}

If RFI filtering is needed, the capacitors designated C_{TC} and C_{RC} in figure 13, connected between TIPX and ground as well as between RINGX and ground, may be mounted.

C_{TC} and C_{RC} work as RFI filters in conjunction with suitable series impedances (i.e. resistances, inductances). Resistors R_{F1} and R_{F2} may be sufficient, but series inductances can be added to form a second order filter. Current-compensated inductors are suitable since they suppress common-mode signals with minimum influence on return loss. Recommended values for C_{TC} and C_{RC} are below 1 nF. Lower values impose smaller degradation on return loss and longitudinal balance, but also attenuate radio frequencies to a smaller extent. The influence on the impedance loop must also be taken into consideration when programming the CODEC. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) = 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

AC - DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and RINGX provides the separation of the ac and dc signals. C_{HP} positions the low end frequency response break point of the ac loop in the SLIC. Refer to table 1 for recommended value of C_{HP}.

Example: A C_{HP} value of 68 nF will position the low end frequency response 3dB break point of the ac loop at 13 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where R_{HP} = 180 kΩ.

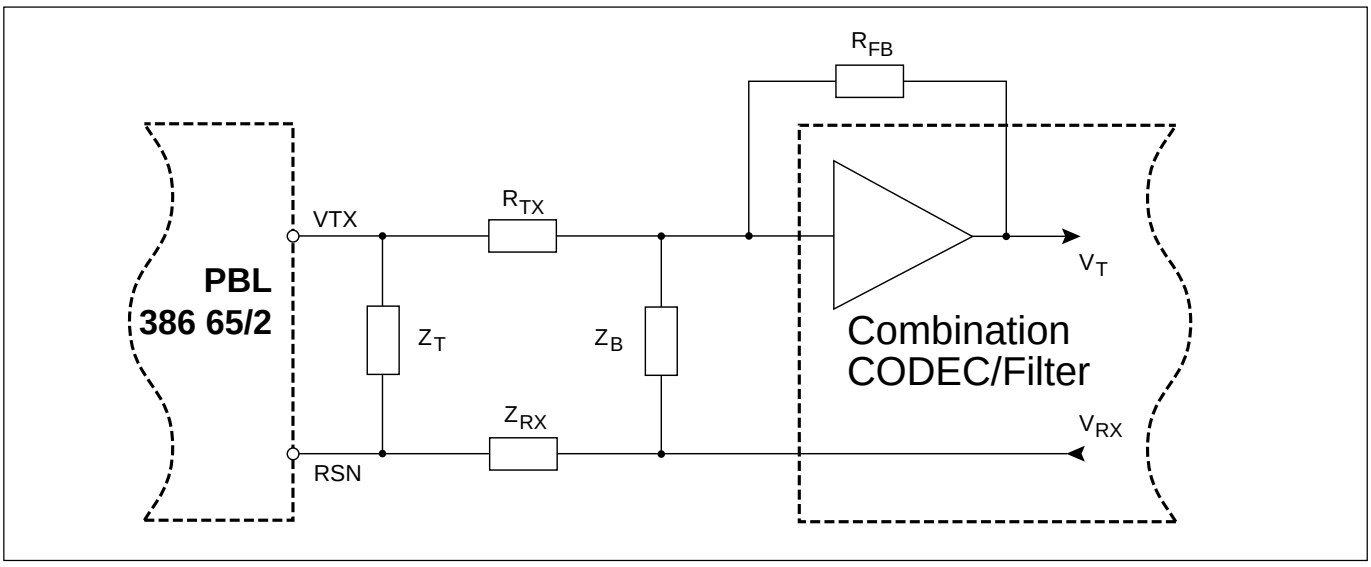


Figure 10. Hybrid function.

High-Pass Transmit Filter

When CODEC/filter with a singel 5 V power supply is used, it is necessary to separate the different signal reference voltages between the SLIC and the CODEC/filter. In the transmit direction this can be done by connecting a capacitor between the VTX output of the SLIC and the CODEC/filter input. This capacitor will also form, together with R_{TX} and/or the input impedance of the CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a fast enough response for the dc steps that may occur with DTMF signaling.

Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals LP and VBAT, positions the high end frequency break point of the low pass filter in the dc loop in the SLIC. C_{LP} together with C_{HP} and Z_T (see section Two-Wire Impedance) forms the total two wire output impedance of the SLIC. The choice of these programming components influence the power supply rejection ratio (PSRR) from VBAT to the two wire side in the low frequency range.

R_{Feed} [Ω]	R_{SG} [kΩ]	C_{LP} [nF]	C_{HP} [nF]
2•25	4.02	330	68
2•50	23.7	330	68
2•200	147	100	33
2•400	301	47	33
2•800	619	22	33

Table 1. R_{SG}, C_{LP} and C_{HP} values for different feeding characteristics.

Table 1 suggest values of C_{LP} and C_{HP} for different feeding characteristics.

Adaptive Overhead Voltage, AOV

The Adaptive Overhead Voltage feature minimises the power dissipation and at the same time provides a flexible solution for differing system requirements and possible future changes concerning voice, metering and other signal levels. This is done by using an overhead voltage which automatically adapts to the signal level (voice + metering). With the AOV-pin left open, the PBL 386 65/2 will behave as a SLIC with fixed overhead voltage for signals in the 0 - 20kHz frequency range and with an amplitude less than $3.1V_{Peak}$[11]. For signal amplitudes between $3.1V_{Peak}$ and $6.2V_{Peak}$, the AOV-function will expand the overhead voltage making it possible for the signal, Vt, to propagate through the SLIC without distortion (see figure 11). The expansion of the overhead voltage occurs instantaneously. When the signal amplitude decreases, the overhead voltage returns to its initial value with a time constant of approximately one second.

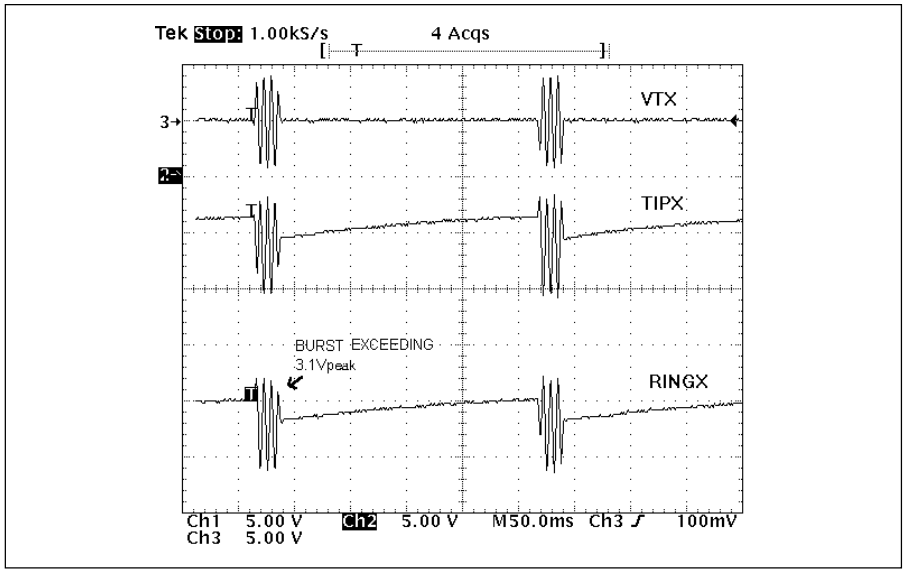


Figure 11. The AOV funktion when the AOV-pin is left open. (Observe, burst undersampled).

If the AOV-pin is connected to AGND, the overhead voltage will automatically be adjusted for signal levels between 0.6 V_{Peak} and 6.2 V_{Peak}.

AOV In the Constant Current Region

When the overhead voltage is automatically increased, the apparent battery (V_{App}, reference F in figure 15), will be reduced by the signal amplitude minus 3.1 V_{Peak}[(11)], (Vt - 3.1[(11)]).

In the constant current region this change will not affect the line current as long as

$V_{TR} < V_{App} - (I_{LConst} \cdot R_{Feed}) - (Vt\text{-}3.1^{(11)})$, (references A-C in figure 15).

AOV In the Resistive Loop Feed Region

The saturation guard will be activated when the SLIC is working in the resistive loop feed region, i.e.

$V_{TR} > V_{App} - (I_{LConst} \cdot R_{Feed}) - (Vt - 3.1^{(11)})$ (references D in figure 15).

If the signal amplitude is greater than $3.1V_{Peak}$[11] the line current, I_L, will be reduced corresponding to the formula

$\Delta I_L = | (Vt - 3.1^{(11)})/(R_L + R_{Feed}) |$.

This reduction of line current will introduce a transversal signal into the two-wire which under some circumstances may be audible (e g when sending metering signals > 3.1 V_{Peak} without any speech signal burying the transversal signal generated from the linecurrent reduction).

The sum of all signals should not exceed 6.2 V_{Peak}.

Line Feed

If $V_{TR} < V_{App} - (I_{LConst} \cdot R_{Feed})$, the PBL 386 65/2 SLIC will emulate constant current feed (references A-C in figure 15).

For $V_{TR} > V_{App} - (I_{LConst} \cdot R_{Feed})$ the PBL 386 65/2 SLIC will emulate resistive loop feed programmable between 2•25 Ω[12] and 2•900 Ω (references D in figure 15). The current limitation region is adjustable between 0 mA and 65 mA[13].

When the line current is approaching open loop conditions, the overhead voltage is reduced. To ensure maximum open loop voltage, even with telephone line leakage, this occurs at a line current of approximately 5 mA (references E in figure 15). After the overhead voltage reduction, the line voltage is kept nearly constant with a steep slope corresponding to 2 • 25 Ω(reference G in figure 15).

The open loop voltage, V_{TRMax}, measured between the TIPX and RINGX terminals is tracking the battery voltage V_{Bat} (references H in figure 15). V_{TRMax} is programmable by connecting the AOV-pin to AGND or by leaving the AOV-pin open.

V_{TRMax} is defined as the battery voltage on the VBat terminal minus the Battery Over Head voltage, V_{BOH}, according to the equation

$$V_{TRMax}(\text{at } I_L = 0 \text{ mA}) = |V_{Bat}| - V_{BOH}$$

Refer to table 2 for typical V_{BOH} values.

	V_{BOH}(typ) [V]
AOV-PIN NC	4.2
AOV-PIN to AGND	3.2

Table 2. The battery overhead voltages at open loop conditions.

Resistive Loop Feed Region

The resistive loop feed (reference D in figure 15) is programmed by connecting a resistor R_{SG} , between terminals PSG and VBAT according to the equation

$$R_{Feed} = \frac{R_{SG}}{400} + 40 + 2R_F$$

Constant Current Region

The current limit (reference C in figure 15) is adjusted by connecting a resistor, R_{LC}, between terminal PLC and ground according to the equation:

$$R_{LC} = \frac{500}{I_{LProg}} \quad ^{14}$$

Battery Switch (VBAT2)

To reduce short loop power dissipation, a second lower battery voltage may be connected to the device through an external diode at terminal VBAT2. The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching occurs when the line voltage passes the value

$V_{TR} = |V_{Bat2}| - 40 \cdot I_L - 6$ [15]

Connect the terminal VBAT2 to the second power supply via the diode D_{B2} in figure 14.

An optional diode D_{BB} connected between terminal VBAT and the VB2 power supply, see figure 13, will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears.

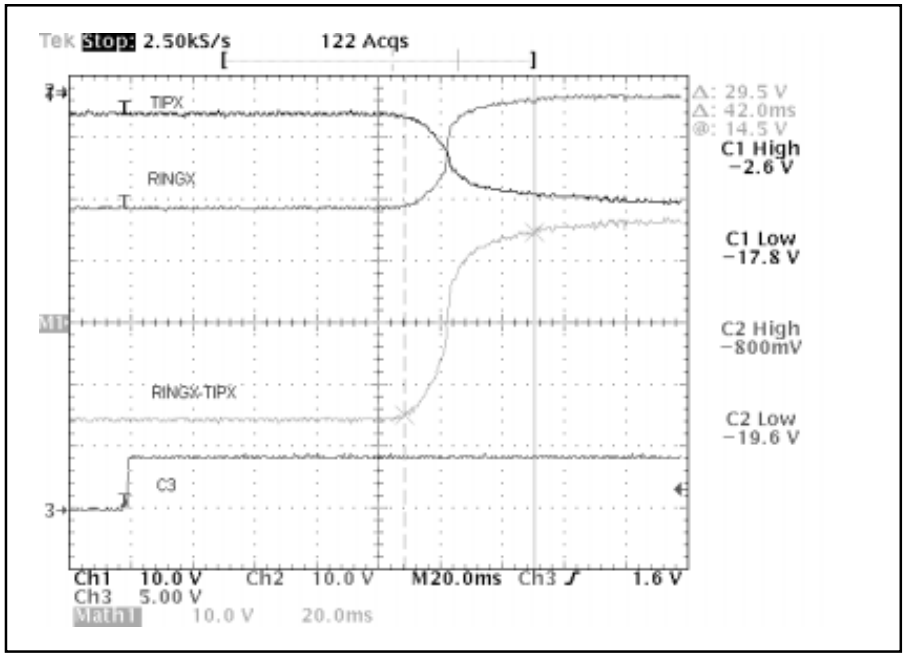


Figure 12. Silent Polarity Reversal

If the V_{B2} voltage is not available, an optional external power management resistor, R_{PM}, may be connected between the VBAT2-pin and the VBAT-pin to move power dissipation outside the chip.

Calculation of the external power management resistor to locate the maximum power dissipation outside the SLIC is according to:

$$R_{PM} = \frac{|V_{Bat}| - 3}{I_{LProg}}$$

Metering Applications, TTX

It is very easy to use PBL 386 65/2 in metering applications; simply connect a suitable resistor (R_{TTX}) in series with a capacitor (C_{TTX}) between pin RSN and the metering source. Capacitor C_{TTX} decouples all DC-voltages that may be superimposed on the metering signal. Choose $1/(2\pi R_{TTX} C_{TTX}) \geq 5$kHz to suppress low frequency disturbances from the metering puls generator. The metering signal gain can be calculated from the equation:

$$G_{4\text{-}2TTX} = \frac{V_{TR}}{V_{TTX}} =$$

$$\frac{Z_T}{R_{TTX}} \cdot \frac{Z_{LTTX}}{\frac{Z_T}{\alpha_{RSN}} - G_{2\text{-}4S} \cdot (Z_{LTTX} + 2R_F)}$$

where:

V_{TTX} is the voltage of the signal at the metering generator,

Z_{LTTX} is the line impedance seen by the 12 or 16 kHz metering signal,

$G_{2\text{-}4S}$ is the transmit gain through the SLIC, i e -0.5. (Phase shift 180°)

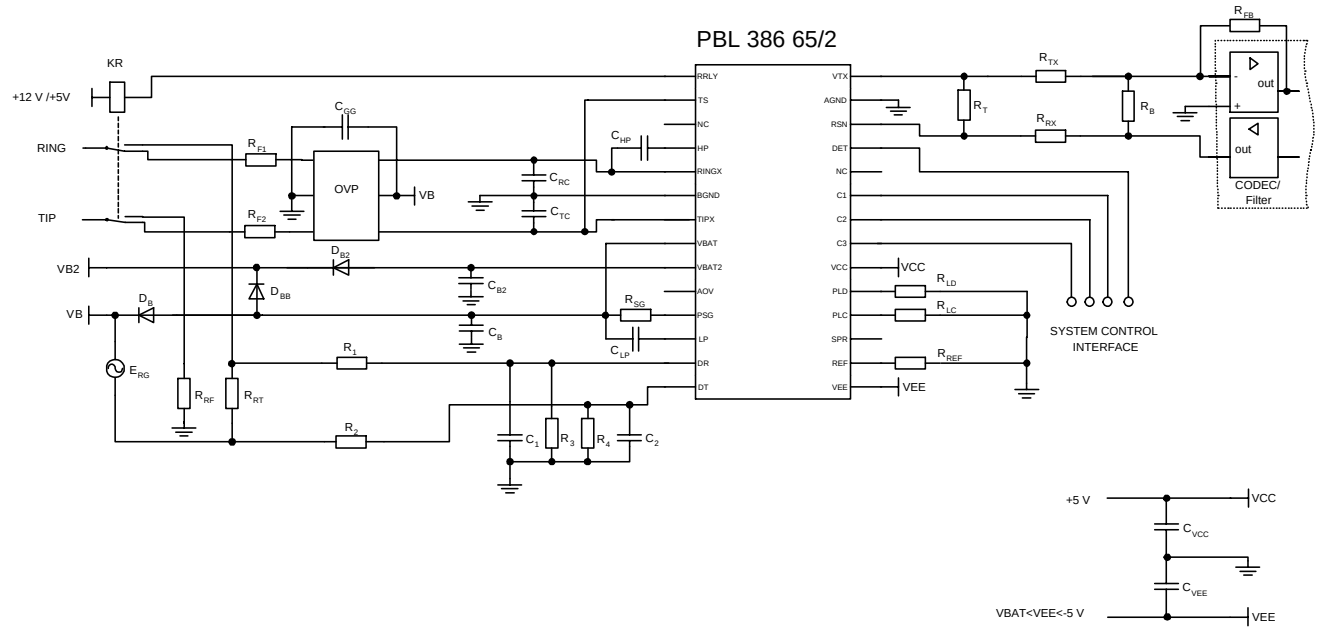
In metering applications with resistive line feeding characteristic and very strict requirements (as mentioned earlier in chapter “AOV in resistive loop feed region“), the metering signal level should not exceed 2.2 V_{RMS} [16], since a reduction of the line current will generate a transversal, and sometimes audible, signal (which is not the case in the constant current region).

Silent Polarity Reversal

The reversal time is set by a capacitor, $C_{sprv,}$ between the pin SPR and AGND. The reversal has a setup time and reversal time see figure 12.

The setup time is different in Active- to Reversal-state and Reversal- to Active state but the silent polarity reversal time is the same Active- to Reversal-state and Reversal- to Active state. To calculate the silent polarity reversal time use following formula:

$$t_r = C_{SPR} \cdot 9500$$



RESISTORS: (Values according to IEC-63 E96 series)

R_{SG}	= 23.7 kΩ	1%	1/10 W
R_{LD}	= 49.9 kΩ	1%	1/10 W
R_{LC}	= 18.7 kΩ	1%	1/10 W
R_{REF}	= 15 kΩ	1%	1/10 W
R_T	= 105 kΩ	1%	1/10 W
R_{TX}	= 32.4kΩ	1%	1/10 W
R_B	= 57.6kΩ	1%	1/10 W
R_{RX}	= 105kΩ	1%	1/10 W
R_{FB}	Depending on CODEC / filter		
R_1	= 604 kΩ	1%	1/10 W
R_2	= 604 kΩ	1%	1/10 W
R_3	= 249 kΩ	1%	1/10 W
R_4	= 280 kΩ	1%	1/10 W
R_{RT}	= 332 Ω	5%	2 W
R_{RF}	= 332 Ω	5%	2 W
R_{F1}, R_{F2}	= Line resistor, 40 Ω	1%	

CAPACITORS:(Values according to IEC-63 E6 series)

C_B	= 100 nF	100 V 20%
C_{B2}	= 150 nF	100 V 20%
C_{VCC}	= 100 nF	10 V 20%
C_{VEE}	= 100 nF	10 V* 20%
C_{TC}	= 1 nF	100 V 20%
C_{RC}	= 1 nF	100 V 20%
C_{HP}	= 68 nF	100 V 20%
C_{LP}	= 330 nF	100 V 20%
C_{GG}	= 220 nF	100 V 20%
C_1	= 330 nF	63 V 10%
C_2	= 330 nF	63 V 10%

*100V if VEE pin connected to VBAT, VBAT2

DIODES:

D_B	= 1N4448
D_{B2}	= 1N4448
D_{BB}	= 1N4448 (optional)

OVP:
Secondary protection (eg Power Innovations TISP PBL2). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably a groundplane.

Figure 13. Single-channel subscriber line interface with PBL 386 65/2 and combination CODEC/filter

Active- to Reversal-state and Reversal- to Active state and the setup time use following formulas.

Active → Reversal:
$t_{Act \rightarrow Rev} = C_{SPR} \cdot 17500$

Reversal → Active:
$t_{Rev \rightarrow Act} = C_{SPR} \cdot 15500$

The time is measured between 10% and 90% of the line voltage. The reversal time is independent of line load and line current.

Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 386 65/2 SLIC reduces the dc line current and the longitudinal current limit when the chip temperature reaches approximately 145°C and increases it again automatically when the temperature drops.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, DET. The status of the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to section Control Inputs for a description of the control interface.

Loop Current Detector

The loop current detector indicates that the telephone is off hook and that DC current is flowing in the loop by putting the output pin

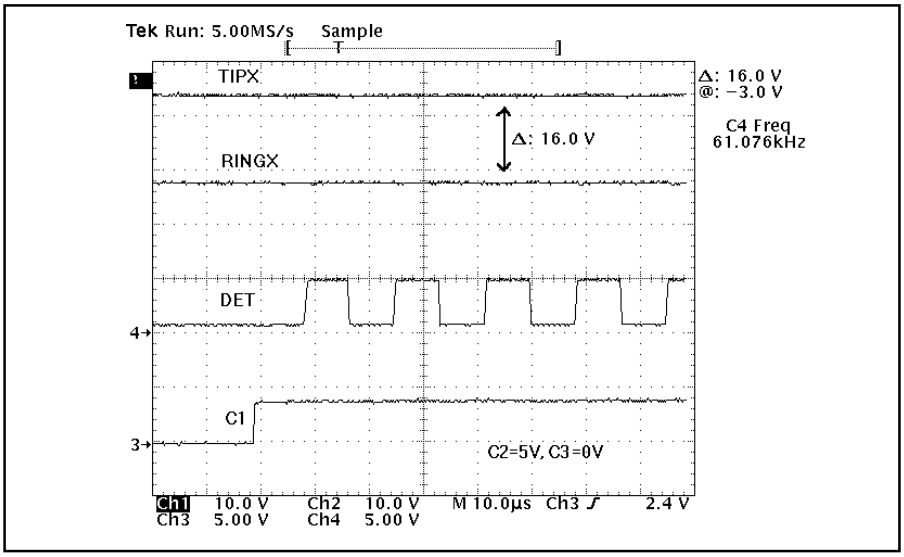


Figure 14. Line voltage Measurement

DET, to a logic low level when selected. The loop current detector threshold value, I_{LTh}, where the loop current detector changes state, is programmable with the R_{LD} resistor. R_{LD} connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{LTh}}$$

The current detector is internally filtered and is not influenced by the ac signal at the two wire side.

Ground Key Detector

The ground key detector indicates when the ground key is pressed (active) by putting the output pin DET to a logic high level when selected. The ground key detector circuit senses the difference between TIPX and RINGX currents. The detector is triggered when the difference exceeds the current threshold.

Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced e g superimposed on the battery voltage or ground. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 13 gives an example of a ring trip detection network. This network is applicable, when the ring voltage superimposed on the battery voltage is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT and DR via the filter network R_1, R_2, R_3, R_4, C_1 and C_2. DT is more positive than DR, with the line on-hook (no dc current). The DET output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow through the loop including sense resistor R_{RT} and will cause the input DT to become more negative than input DR. This changes the output on the DET pin to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay via the SLIC, i.e. ring trip.

Complete filtering of the 20 Hz ac component at terminals DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. Off-hook condition is indicated when the DET output is at logic level low for more than half the time.

Line Voltage Detector

The line voltage is presented on the detector output as a pulse train (see figure 15) with a frequency inversely proportional to the voltage according to the equation:

$$\text{freq} = \frac{10^6}{|V_{TR}| + 1} \text{ [Hz]}$$

The line voltage measurement will be started when entering this state from any other state.

Detector Output (DET)

The PBL 386 65/2 SLIC incorporates a detector output driver designed as open collector (npn) with a current sinking capability of min 3 mA, and a 5 kΩ pull-up resistor. The emitter of the drive transistor is connected to AGND. A LED can be connected in series with a resistor (≈1 kΩ) at the DET output to visualize, for example loop status.

Relay driver

The PBL 386 65/2 SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA.The emitter of the drive transistor is connected to BGND. The relay driver has an internal zener diode clamp to protect the SLIC from inductive kick-back voltages. No external clamp is needed.

Control Inputs

The PBL 386 65/2 SLIC has three digital control inputs, C1, C2 and C3.

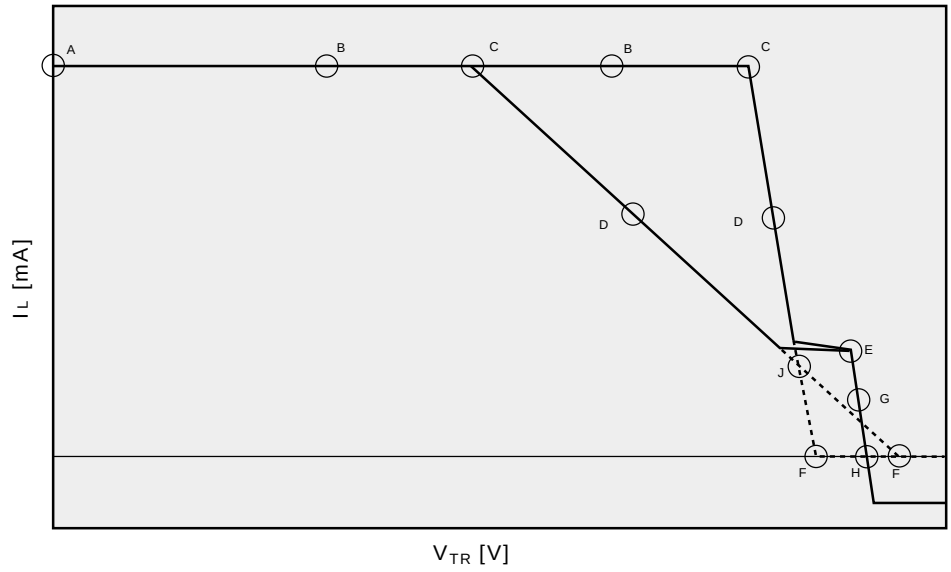
A decoder in the SLIC interprets the control input condition and sets up the commanded operating state.

C1 to C3 are internal pull-up inputs.

Open Circuit State

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active.

DC characteristics



A: I_L (@ V_{TR} = 0) = I_{LConst} I_{LConst} (typ) = $I_{LProg} = \frac{500}{R_{LC}}$ (14)

B, C: $I_L = I_{LConst}$ $V_{TR} = V_{BatVirt} - R_{Feed} \cdot (I_{LProg} - 5 \cdot 10^{-3})$

D: $R_{Feed} = \frac{R_{SG}}{400} + 40$

E: $I_L \approx 5$ mA

F: Apparent battery V_{App} (@I_L = 0) = $V_{BatVirt} + 5 \cdot 10^{-3} \cdot R_{Feed}$

G: $R_{FeedG} = 2 \cdot 25\ \Omega$

H: $V_{TRMax} = |V_{Bat}| - V_{BOH}$

J: Virtual battery $V_{BatVirt}$ (@ I_L = 5 mA) = $|V_{Bat}| - 6.8$ (17)

Figure 15. Battery feed characteristics (without the protection resistors on the line).

Ringing State

In the ringing state the SLIC will behave as in the active state with the exception that the ring relay driver and the ring trip detector are activated. The ring trip detector will indicate off hook with a logic low level at the detector output.

Active State

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. The loop current or the ground key detector is activated. The loop current detector indicates off hook with a logic low level and the ground key detector indicates active ground key with a logic high level present at the detector output.

Active Line Voltage State

In PBL 386 65/2 a line voltage measurement feature is available in the active state. A frequency inversely proportional to the line voltage is presented on the detector output (see chapter “Line Voltage Detector“). The data can be used in a variety of ways, for example to set transmission parameters in a programmable CODEC, in-line testing where short circuits on the line can be detected and to control the metering signal amplitude. In the active line voltage state the SLIC will be as in the active state except for the detector.

Active Polarity Reversal State

TIPX and RINGX polarity is reversed compared to the Active State: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. The loop current or the ground key detector is activated. The loop current detector will indicate off hook with a logic low level and the ground key detector will indicate active ground key with a logic high level present at the detector output.

Tip Open State

The Tip Open State is used for ground start signaling.

In this state the SLIC presents a high impedance on the TIPX pin and the programmed dc characteristic on the RINGX pin, without the longitudinal current compensation.

The loop current detector is active (refer to the datasheet for information on the detector threshold level).

Overvoltage Protection

PBL 386 65/2 must be protected against overvoltages on the telephone line. The overvoltages could be caused for instance by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum continuous and transient voltages.

Secondary Protection

The circuit shown in figure 13 utilizes series resistors together with a programmable overvoltage protector (e g Power Innovations TISP PBL2), serving as a secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage, V_B). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_B supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. If a PTC is chosen for R_F , note that it is important to always use the PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the TISP.

Power-up Sequence

No special power-up sequence is necessary except that ground has to be present before all other power supply voltages.

The digital inputs C1 to C3 are internal pull-up terminals.

Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function;

The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN pin. Ground plane surrounding the RSN pin is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) on the PCB in one point.

R_{LC} and R_{REF} should be connected to AGND with short leads. Pin LP, pin PSG and pin AOV are sensitive to leakage currents. Pin AOV should be surrounded by a guardring connected to AGND.

R_{SG} and C_{LP} connections to VBAT should be short and very close to each other.

C_B and C_{B2} must be connected with short wide leads.

Notes

Note 11.

3.1 V_{Peak} if AOV-pin is left open and 0.6 V_{Peak} if AOV-pin is connected to AGND.

Note 12.

R_{Feed} lower than 2x50Ω will reduce noise and PSRR performance in resistive loop region (reference D in figure 15). Better PSRR performance can be achieved by increasing C_{LP} and C_{HP}.

Note 13.

If the momentary value of the current in TIPX-pin or RINGX-pin exceeds 85mA harmonic distortion specification can be derated.

Note 14.

The accurate equation for R_{LC} is:

$$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \cdot \ln(I_{LProg} \cdot 32)}{I_{LProg}}$$

Note 15.

6.0V when AOV-pin is not connected, 3.9V when AOV-pin is connected to AGND.

Note 16.

2.2V_{RMS} if AOV-pin is left open and 0.4V_{RMS} if AOV-pin is connected to AGND.

Note 17.

6.8V when AOV-pin is left open, 4.2V when AOV-pin is connected to AGND.

Ordering Information

Package	Temp. Range	Part No.
28pin PLCC Tube	-40° - +85° C	PBL 386 65/2QNS
28pin PLCC Tape & Reel	-40° - +85° C	PBL 386 65/2QNT
28pin SSOP Tape & Reel	-40° - +85° C	PBL 386 65/2SHT

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