PBL 402 15

RF Transceiver circuit for the Digital Enhanced Cordless Telecommunications (DECT) system

Description.

The PBL 402 15 is a complete RF transceiver to be used in the Digital Enhanced Cordless Telecommunications (DECT) system. It is designed to interface to various base-band controllers.

The circuit contains transmit and receive functions that share integrated high stability VCO´s and a phase locked loop function (PLL). All functionality is controlled through a 3-wire bus interface with optional hard wire lines.

The receive section comprises of a low noise image reject down conversion to the first intermediate frequency, an external channel filter, a second down convertion to a second intermediate frequency, an integrated channel pass filter, a high gain limiting amplifier, a received signal strenght indicator with DC compensation loop, a self aligned frequency discriminator and a preamble based data slicer.

The transmit section comprises of a signal gate and a pre-power amplifier. Data transmission is achieved by direct open loop modulation of the Tx VCO.

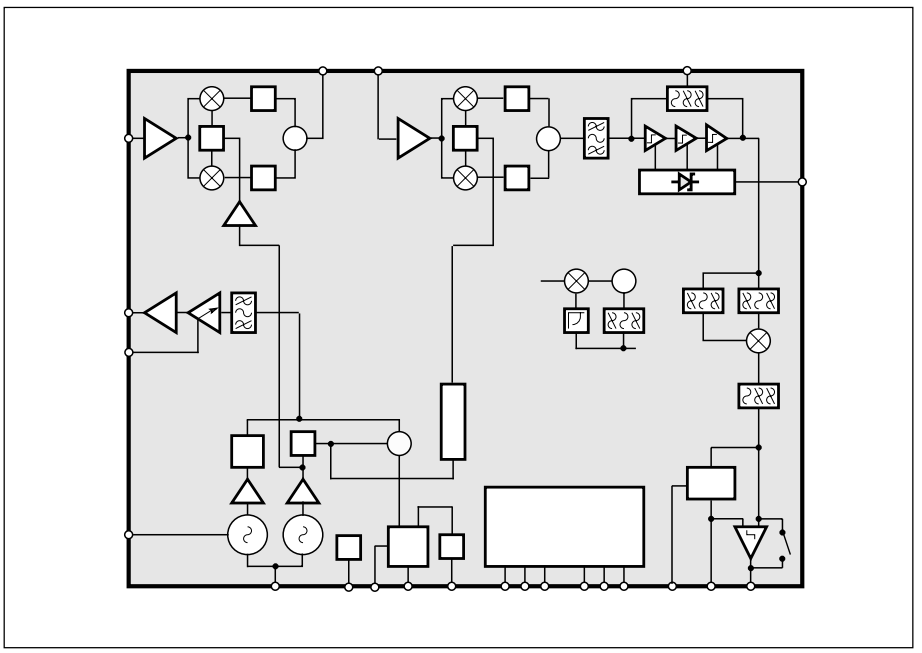


Figure 1. Block diagram.

Key features.

- High Tx output power to +7dBm
- Integrated PLL and high stability VCO´s
- 3-line serial interface bus
- Minimum 2.7 V supply voltage
- Low current consumption
- Differential Rx input and Tx output
- Flexible interface to various base-band controllers
- Exellent performance with Ericsson´s power amplifier PBL403 09
- Low cost

Applications:

- DECT Handset and base station
- Wireless local area network (WLAN)
- Wireless local loop (WLL)

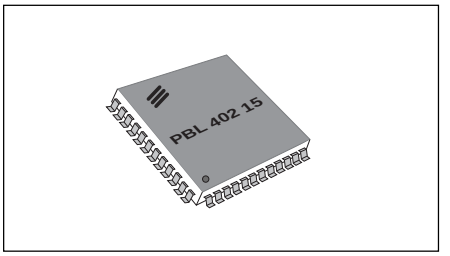


Figure 2. Package outlook.

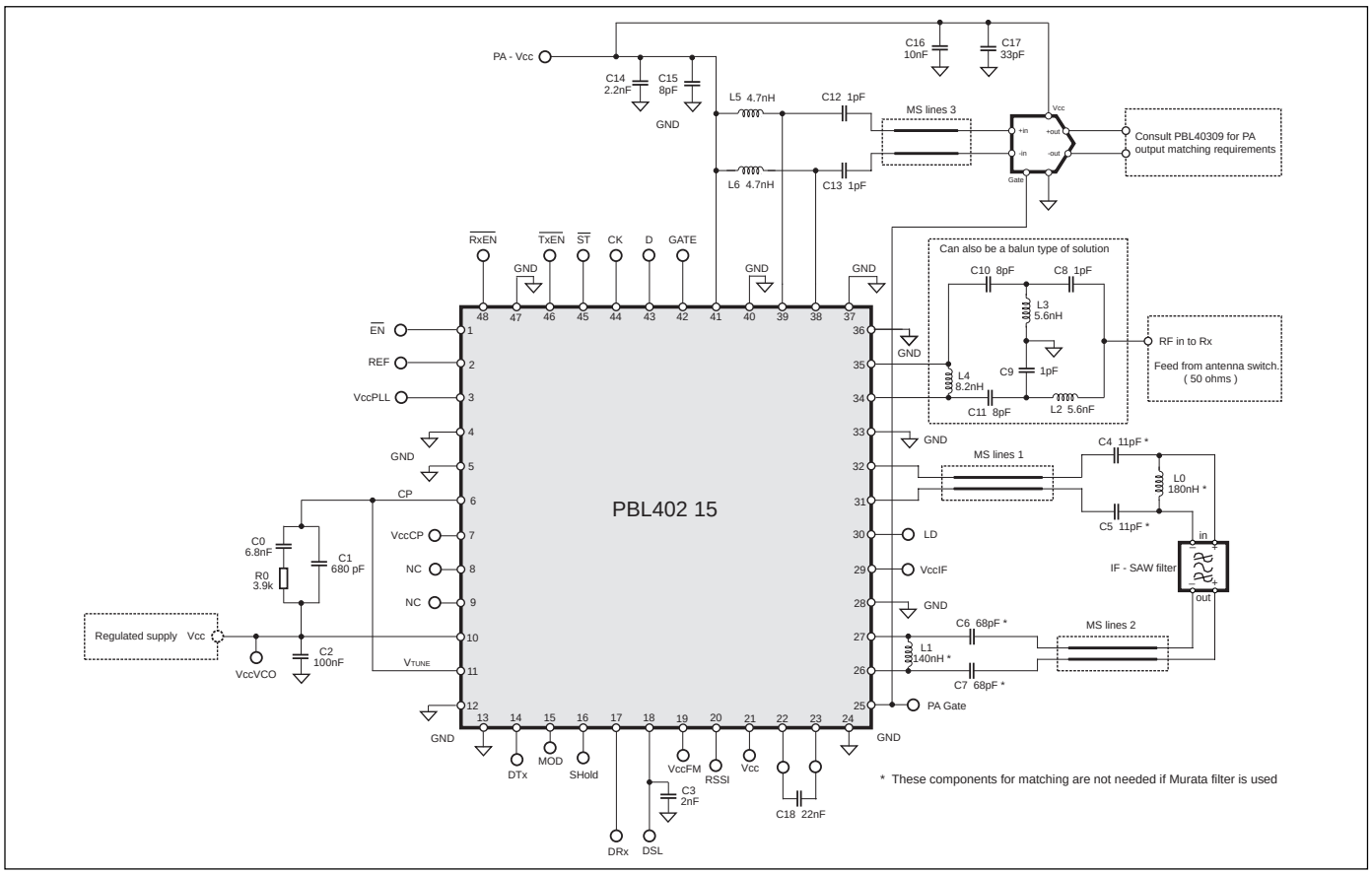


Figure 3. DECT application.

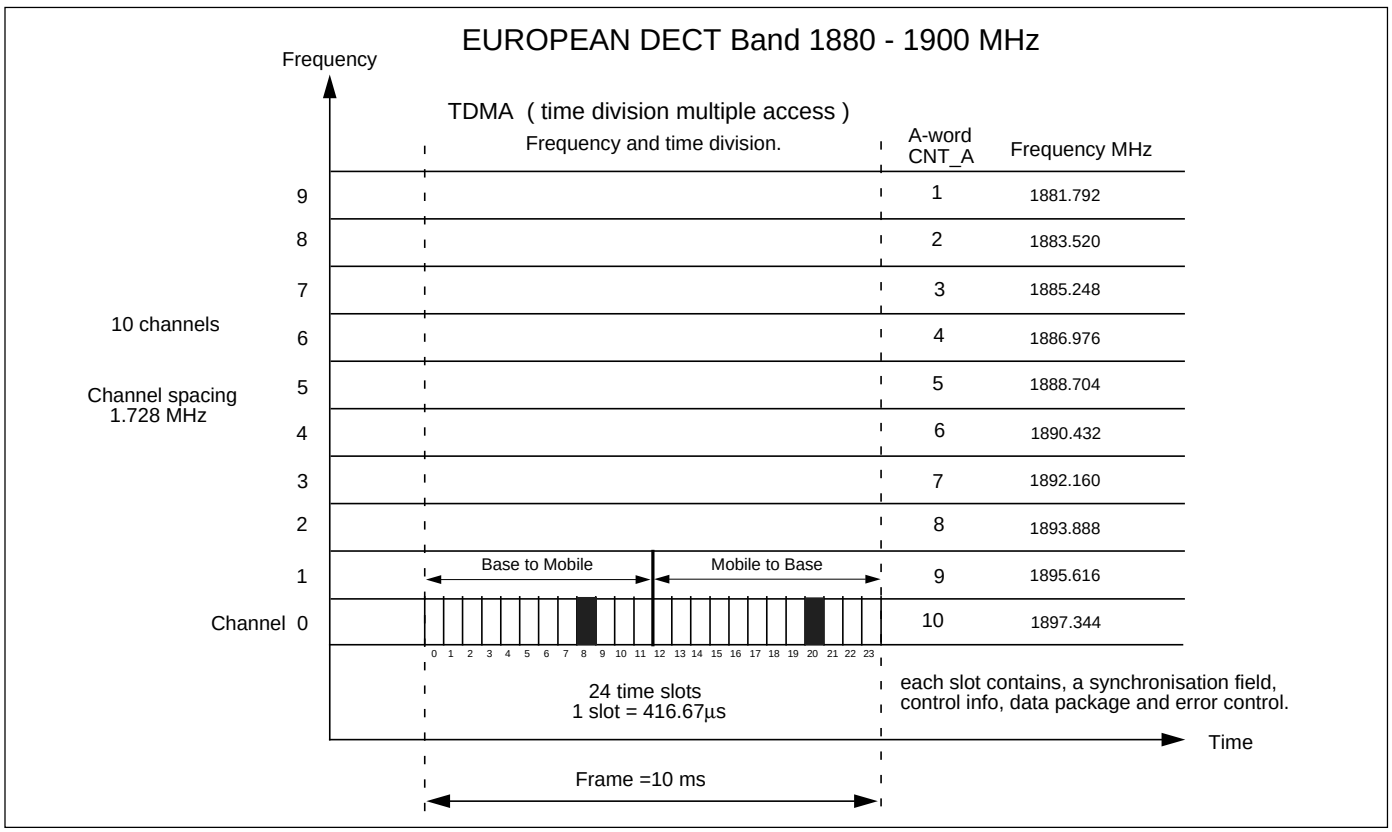


Figure 4. The European DECT band .

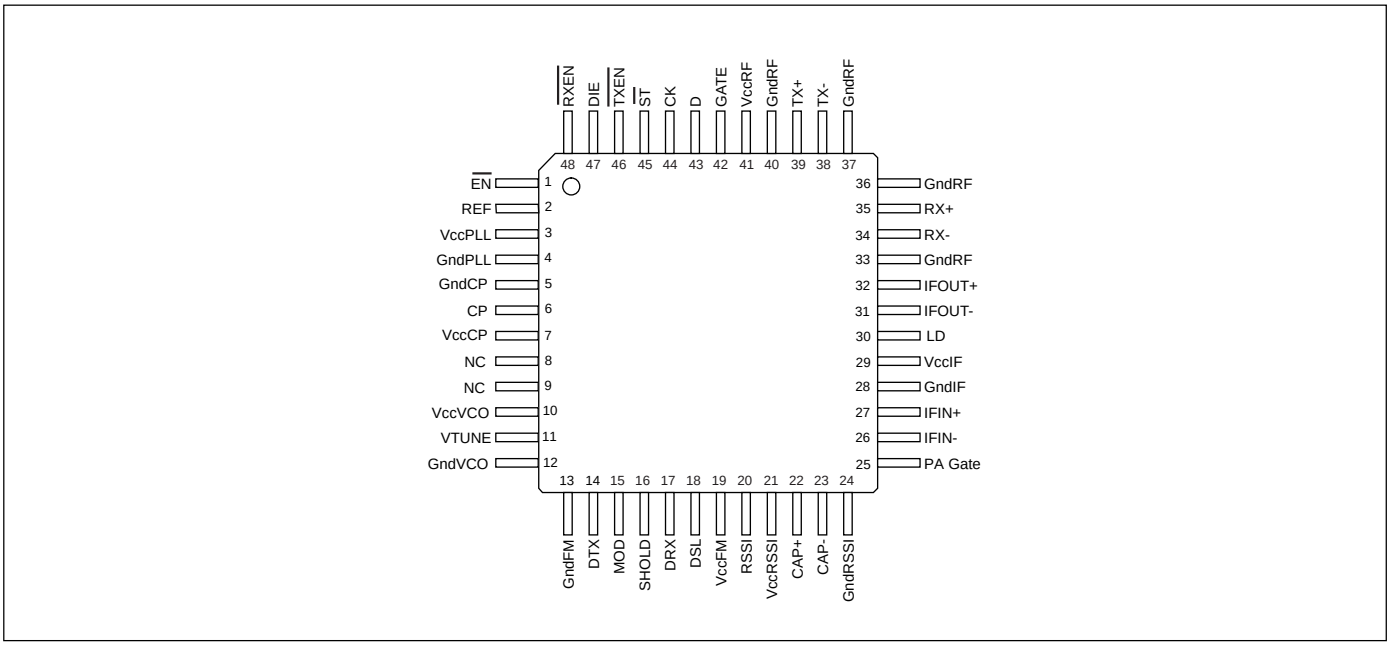
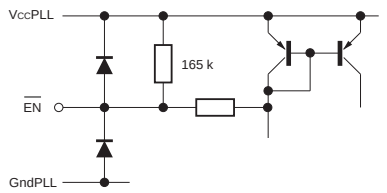
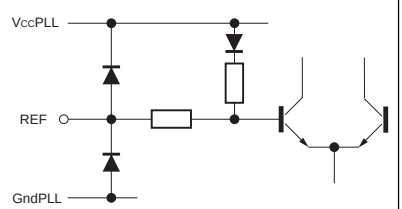
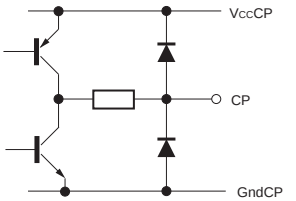


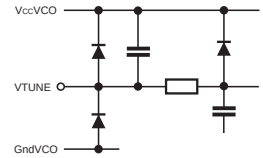
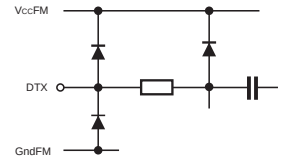
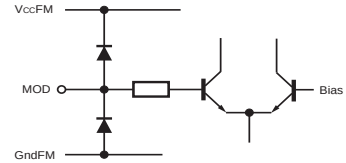
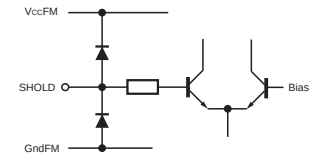
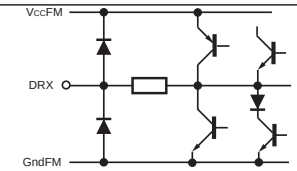
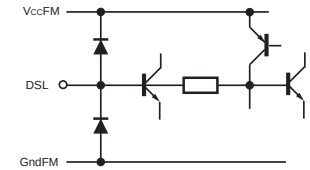
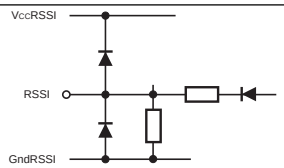
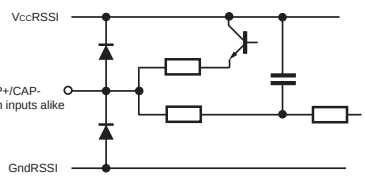
Figure 5. Pinning configuration.

Pin Descriptions:

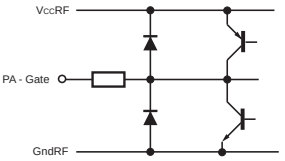
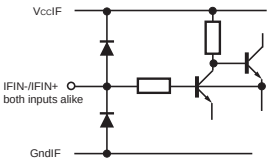
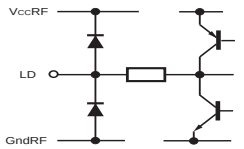
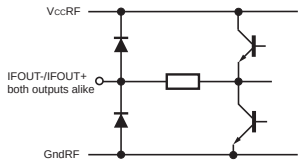
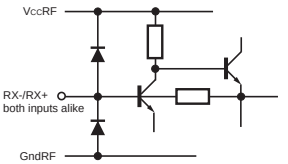
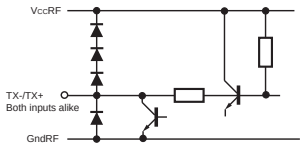
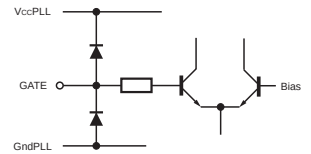
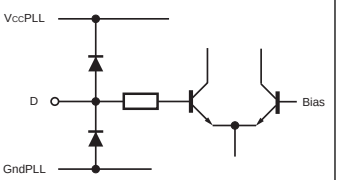
Refer to pin configuration.

Pin number	Name	Function	Schematic in/output of the pin
1	$\overline{EN}$	Enable 3-wire interface and synthesiser.	
2	REF	PLL reference clock input	
3	VccPLL	Voltage supply to the frequency synthesiser.	Clamp to GndPLL
4	GndPLL	Ground connection to the frequency synthesiser.	A diode to GndCP and GndRF
5	GndCP	Ground connection to the charge pump.	A diode to GndPLL and GndVCO
6	CP	Charge pump output.	
7	VccCP	Voltage supply to the charge pump.	Clamp to GndCP

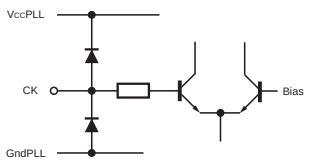
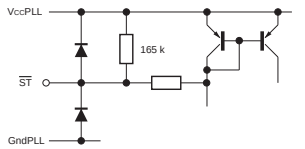
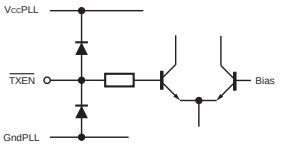
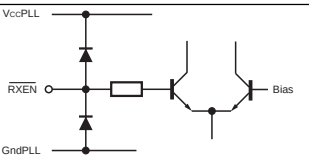
Pin Descriptions (cont.):

Pin number	Name	Function	Schematic in/output of the pin
8 9		Not connected Not connected	N/C
10	VccVCO	Voltage supply to the VCO	Clamp to GndVCO
11	VTUNE	Tuning voltage input for the VCO	
12	GndVCO	Ground connection to the VCO	A diode to GndCP and GndFM
13	GndFM	Ground connection to the FM discriminator section.	
14	DTX	Tx data input for either analog or logic signal.	
15	MOD	Apply modulation. The PLL is set into open loop condition and modulation is applied to the VCO.	
16	SHOLD	Slice level hold logic input. (In Tx mode this input may also act as the MOD pin).	
17	DRX	Rx data output of FM discriminator for either analog or logic signal.(In standby mode outputs lock detect)	
18	DSL	Data slice level output.	
19	VccFM	Voltage supply to the FM discriminator section.	Clamp to GndFM
20	RSSI	RSSI output of limiting strip detector chain.	
21	VccRSSI	Voltage supply to the RSSI section.	Clamp to GndRSSI
22 23	CAP+ CAP-	External stabilising capacitors for limiting strip DC input offset correction loop.	

Pin Descriptions (cont.):

Pin number	Name	Function	Schematic in/output of the pin
24	GndRSSI	Ground connection to the RSSI.	A diode to GndFM and GndIF
25	PA Gate	Output control signal for external PA power on/off.	
26 27	IFIN- IFIN+	Rx IF inputs to internal channel filtering, limiting amplifiers,RSSI and FM discriminator. Internally matched to 300 Ω.	
28	GndIF	Ground connection to the down IF convertor and channel filter sections.	A diode to GndFM and GndIF
29	VccIF	Voltage supply to the down IF convertor and channel filter sections.	Clamp to GndIF
30	LD	Lock detect.	
31 32	IFOUT- IFOUT+	Rx IF outputs to external adjacent channel filter. Internally matched to 300Ω.	
33, 36 37, 40	GndRF	Ground connection to the RF sections.	A diode to GndIF and GndPLL
34 35	RX- RX+	RF inputs to LNA and image reject mixer. Internally matched to 100Ω.	
38 39	TX- TX+	Tx outputs to external PA. Internally matched to 100 Ω. Each output requires an externalchoke to Vcc.	
41	VccRF	Voltage supply to the RF sections.	Clamp to GndRF
42	GATE	Input to gate the Tx output power.	
43	D	Serial interface, Data .	

Pin Descriptions (cont.):

Pin number	Name	Function	Schematic in/output of the pin
44	CK	Serial interface, Clock .	
45	$\overline{ST}$	Serial interface, Strobe .	
46	$\overline{TXEN}$	Transmitter enable.	
47	DIE	Gnd. pin used for internal shielding. Connected to DIE substrate.	
48	$\overline{RXEN}$	Receiver enable	

Maximum Ratings

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vcc			5.5	V
Voltage applied between two different supply pins, except VccRF [a]		Vccdiff			0.6	V
Voltage applied between two different ground pins [a]	Grounds are clamped together by diodes	Gnddiff			0.6	V
Maximum input power	LNA input	P_{max}			10	dBm
Maximum power dissipation		P_D			250	mW
IC storage temperature		T_S	-65		150	°C
Lead temperature	solder, 10 sec.	T_{LEAD}			300	°C

(a). Under continous operation and during power-up sequences.

Handling

Every pin withstands the ESD test in accordance with MIL-STD-883 (method 3050) and IEC 68-2.

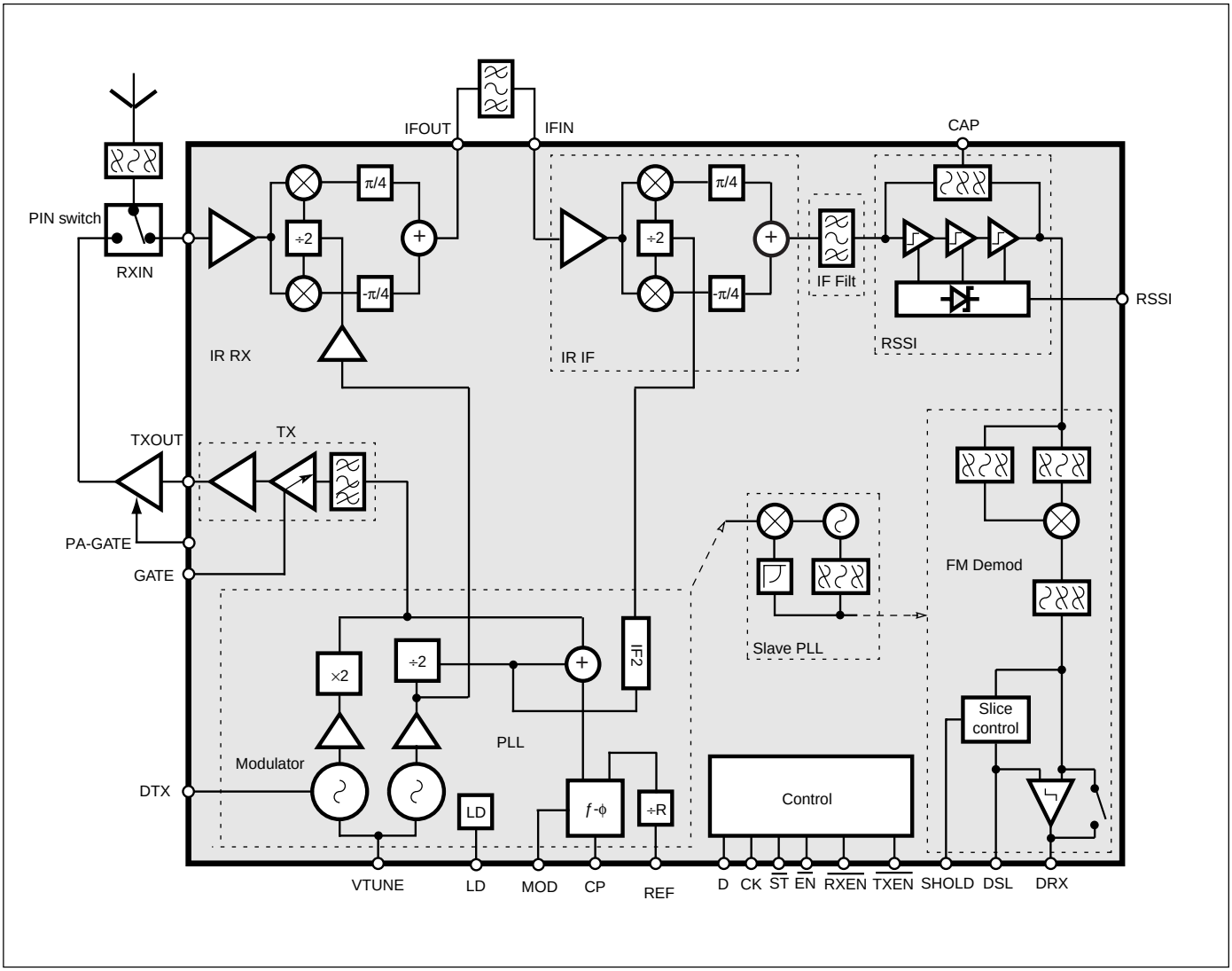


Figure 6. Block diagram.

Operating conditions:

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Temperature range	Fully compliant	T_{AMB}	-20		70	°C
	Operational		-40		85	
Supply voltage range		Vcc	2.7		4.5	V
Shutdown supply current		I_{OFF}			2	µA
Supply current	One slot duplex communication	I_{ACTIVE}		6		mA
Stand-by turn on time [(a)]		τ_{ON}			3	µs
Receive turn on time [(b)]		τ_{RXON}			3	µs
Transmit turn on time [(b)]		τ_{TXON}			3	µs

a. Time may depend upon settling time of the limiting strip DC correction feedback.
b. Time for the receive or transmit gain to be within 1 dB of its final value.

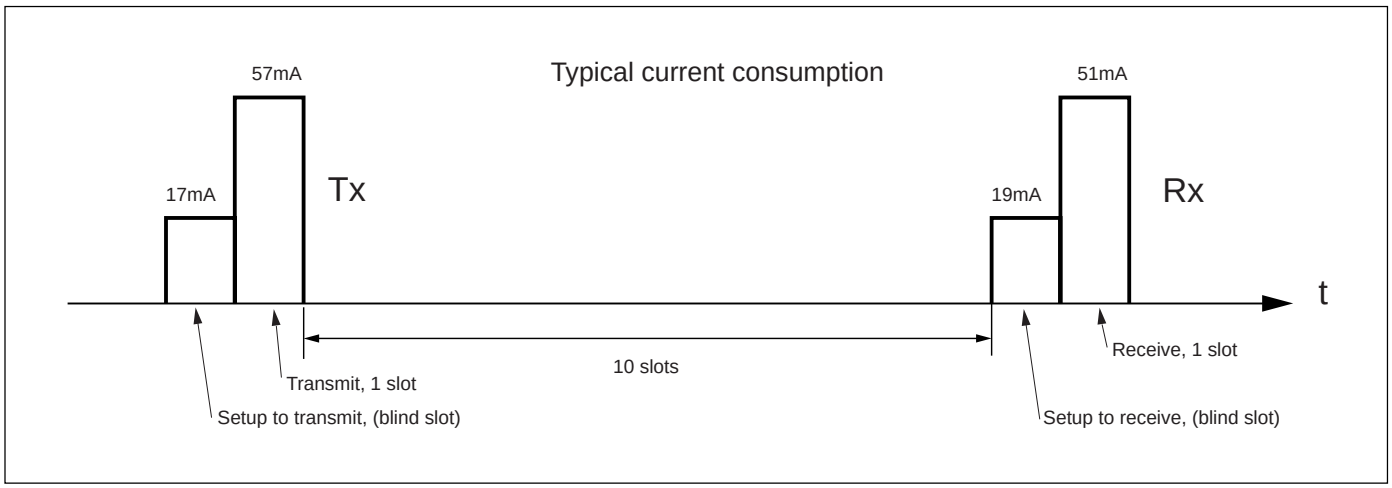


Figure 7. Typical current consumtion.

Digital I/O Parameters

The digital output PA_GATE is served of the VccRF/GndRF supply. All other digital signals are served of the VccPLL/GndPLL supply. The digital signals are $\overline{EN}$, $\overline{RXEN}$,$\overline{TXEN}$, $\overline{ST}$, D, CK, GATE, LD, MOD and SHOLD.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input voltage high		V_{IH}	2.1			V
Input voltage low		V_{IL}			0.6	V
Output voltage high		V_{OH}	V_{CC}-0.4	V_{CC}-0.2		V
Output voltage low		V_{OL}			0.6	V
Digital input capacitance		C_{DI}			2	pF
Digital input resistance		R_{DI}	100			kΩ
Digital load capacitance		C_{DL}			4	pF
Digital load resistance		R_{DL}	30			kΩ

The 3-Wire Control Bus Interface.

The 3-wire serial bus interface controls the various IC parameters and consists of 3 lines, strobe, data and clock (ST, D, CK). Alternatively, selected power control modes may be controlled by 3 hard-wire control lines ($\overline{EN}$, $\overline{RXEN}$, $\overline{TXEN}$).

The 3-wire bus is active when either $\overline{EN}$ or $\overline{ST}$, or both are active. The strobe signal is used to enable the clock and latch the data frame. Each frame consists of 24 bits, built from a word field and a data field. The word address is the last bit to be sent (LSB), with the data field being the proceeding 23 bits. Data on D is shifted into the frame register by clock CK.

The 3-wire interface allows setting of word A and word B. These control the IC configuration.

Frame definition:

	MSB First in																			LSB Last in			
					Data															Word Address			
Frame:	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
Description tag:	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	W0

Digital Interface:

Pin	Spec.	Description
$\overline{ST}$	Digital input	The control section is powered up when $\overline{ST}$ is low. Data is latched on the rising edge. $\overline{ST}$ has an internal 160kΩ pull up resistor to V_{CC} PLL.
CK	Digital input	3-wire interface clock. May be running continuously, but to minimise the risk of VCO spurious it is recommended that the clock only runs when required.
D	Digital input	3-wire interface data. Data latched by rising edge of CK.
$\overline{EN}$	Digital input	IC enable control. Active low. The control section is powered when $\overline{EN}$ is active. $\overline{EN}$ has an internal 160 kΩ pull up resistor to V_{CC} PLL.
$\overline{RXEN}$	Digital input	Receiver enable. Active low.
$\overline{TXEN}$	Digital input	Transmitter enable. Active low.

Digital Interface:

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Serial clock frequency		f_{CK}			13.9	MHz
Delay strobe to first rising clock		t_{SCK}	288			ns
Data setup time: D to CK		t_{DS}	18			ns
Data hold time		t_{DH}	18			ns
Clock pulse widh high		t_{CKW}	18			ns
Strobe hold time high		t_{SW}	144			ns

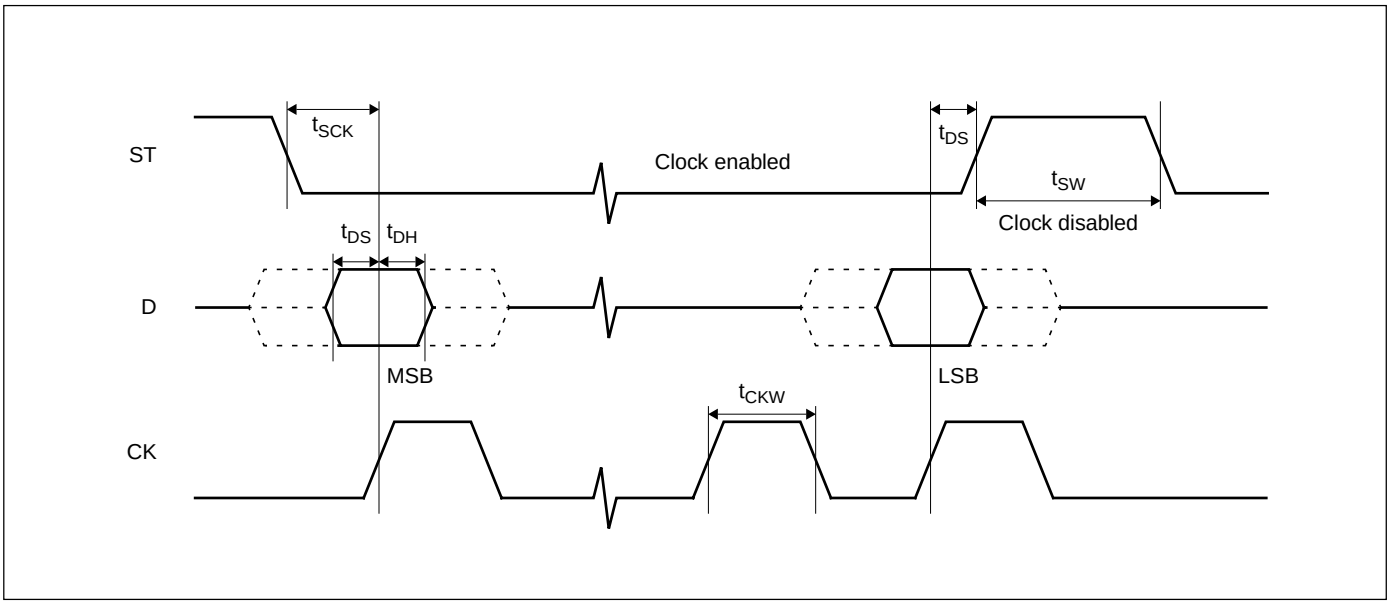


Figure 8. 3-wire timing diagram.

Word A.

Description.

Word A has the address W0 = 0. It permits IC operation and defines the synthesiser frequency.

IC operation is controlled by the $\overline{EN}$ pin and the CE flag. If $\overline{EN}$ is not active then CE must be enabled for the IC to become and remain operational. If CE is disabled then the IC shuts down completely with only the status of $\overline{ST}$ and $\overline{EN}$ determining if the control section takes power. All configurations are erased and must be re-programmed if the chip has been disabled.

CL determines if the internal flags or the hard wire control lines are used to control section power. The internal flags provide more flexibility.

Word A Table.

Data address	Name	Default	Description
D0	CE	0	0 = Chip disable 1 = Chip enable Active low on the external EN pin will also enable the chip
D1	CL	0	0 = Internal control flags 1 = External control lines
D2	CNT_A0	0	Synthesiser frequency counter A bit 0 (LSB) to 4 (MSB)
D3	CNT_A1	0	
D4	CNT_A2	0	
D5	CNT_A3	0	
D6	CNT_A4	0	
D7	CNT_M	0	Synthesiser frequency counter M 0 → M = 32 (used for receive) 1 → M = 34 (used for transmit)
D8	CNT_R	0	Synthesiser reference counter R 0 → R = 6 used if REF = 10.368 MHz 1 → R = 8 used if REF = 13.824 MHz
D9	(a)	0	Receiver VCO enable . 000 = VCO disabled. Any other setting activates the VCO. (default 100)
D10	(a)	0	
D11	RXVCO_EN	0 (1)	
D12	(a)	0	Transmit VCO enable . 000 = VCO disabled. Any other setting activates the VCO. (default 100)
D13	(a)	0	
D14	TXVCO_EN	0 (1)	
D15	Reserved	0	(a)
D16	DRX_T	0	1 = Analog signal output at DRX pin. 0 = Digital data output at DRX pin.
D17	TX_P0	0	Transmit power trim bits 0 (LSB) to 1 (MSB) 00 = -1.3 dB Min. 01 = Nominal power 10 = +1.3 dB 11 = +1.9 dB Max.
D18	TX_P1	0	
D19	RX_G	0	IRRX gain. 0 = +0dB extra 1 = +9dB extra
D20	IFT0	1	Demodulation IF frequency trim bits 0 (LSB) to 2 (MSB). This should be programmed to the default settings.
D21	IFT1	1	
D22	IFT2	0	

a. Use ´0´ only.
b. Recommended at all times.

Word B.

Description.

Word B has address W0 =1. It controls modes, functionality and configuration. Word B signals are only active when CE is enabled or EN is active.

Word B Table.

Data address	Name	Default	Description
D0	SYN_EN	0	1 = Synthesiser power on. 0 = Synthesiser power off.
D1	IF_EN	0	1 = IF receiver enabled. IF mixer + RSSI + Demodulator + Slave PLL 0 = IF receiver disabled.
D2	RX_EN	0	1 = Receiver power on. LNA + front end mixer 0 = Receiver power off.
D3	TX_EN	0	1 = Transmit power on. 0 = Transmit power off.
D4	SHOLD_P	0	1 = Slice hold pin SHOLD, active high. 0 = Slice hold pin SHOLD, active low.
D5	SHOLD_EN	0	1 = Slice hold enable. 0 = Slice hold disable. Active level on the external SHOLD pin determined by SHOLD_P will also enable slice hold.
D6	MOD_P	0	1 = Modulation pin MOD, active high. 0 = Modulation pin MOD, active low.
D7	MOD_EN	0	1 = Enable modulation. 0 = Disable modulation. Active level on the external MOD pin determined by MOD_P will also enable modulation.
D8	MOD_SW	0	1 = Modulation controlled by the SHOLD pin. 0 = Modulation controlled by the MOD pin. The effect is to multiplex between the MOD & SHOLD pins.
D9	GATE_P	0	1 = TX gating pin, GATE active high. 0 = TX gating pin, GATE active low.
D10	CPC0	0	Charge pump operation control.
D11	CPC1	0	00 = Normal 01 = Force CP voltage down (=VCO frequency up) 11 = Tri-state 10 = Force CP voltage up (=VCO frequency down)
D12 to D23			Reserved. These bits need not to be programmed.

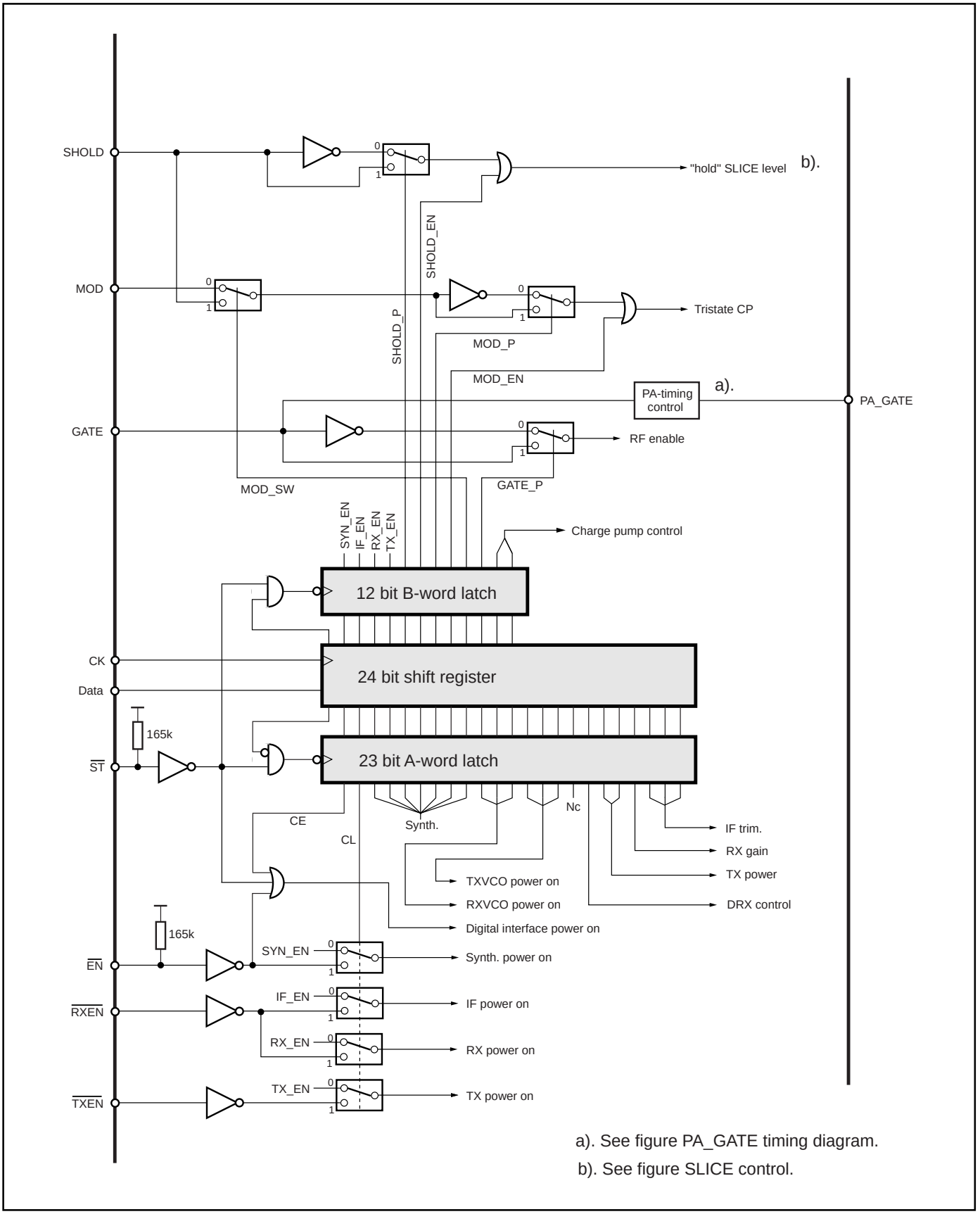


Figure 9. Control logic.

Hard Wire Control Lines.

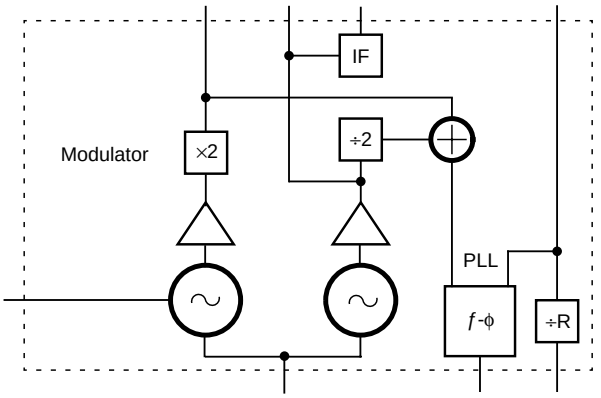
The 3 hardwire control lines $\overline{EN}$, $\overline{RXEN}$ and $\overline{TXEN}$ allow control of the IC by a controller with limited interface access or capabilities. Typically, controllers with only one access per slot or no access between slots.

For correct operation the 3 hard wire lines require appropriate programming of the CE and CL flags.

The hardwire lines directly force the state of the appropriate word B flags as detailed below.

Hard wire line	Description
$\overline{EN}$	Powers the serial bus interface. Upon the rising edge of $\overline{ST}$ and provided CL is set to 1, the effect is as SYN_EN.
$\overline{RXEN}$	Provided $\overline{EN}$ is active and CL is set to 1, the effect is as IF_EN and RX_EN.
$\overline{TXEN}$	Provided $\overline{EN}$ is active and CL is set to 1, the effect is as TX_EN.

LO and Modulation Section.



The LO section consists of a TX VCO with a frequency doubler, a RX VCO and a charge pump PLL.

The VCO´s are fully integrated and are phase/frequency locked to an external reference frequency applied to the REF pin. The frequency is programmed by the 3-wire interface. Lock detect is available on the LD pin. When neither TX_EN or RX_EN are active, lock detect is also available at the DRX output.

The RX VCO runs at twice the frequency. The frequency of the RX VCO is divided by 2 for the PLL. The TX VCO runs at half the TX frequency to improve pulling immunity to TX harmonics. A frequency doubler generates the TX LO for the PLL.

The TX VCO is modulated by an external signal applied to the DTX pin. The DTX input is permanently connected to the TXVCO. An active MOD_EN signal disables the PLL charge pump output which allows modulation to be applied. A hardware modulation enable signal may be applied to either the MOD pin or SHOLD pin depending upon setting of the MOD_SW flag.

TX VCO.

A fully integrated balanced VCO. The VCO frequency is controlled by the voltage applied to the VTUNE pin, and the applied modulation voltage. Both have a negative sensitivity, i.e., as the voltage increases, the VCO frequency decreases. The base-band must invert the transit modulation data to allow for this. The tuning voltage is referenced to V_{CC}VCO.
The VCO is buffered to provide isolation against frequency pulling and reverse injection.

TX VCO Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Carrier frequency range	$0.4 \leq V_T \leq V_{CC}-0.4$	f_C	940		967	MHz
Tuning voltage		V_T	0.4		V_{CC}-0.4	V
Frequency tuning sensitivity		f_{SEN}	~-40	~-72	~-140	MHz/V
Frequency pulling	stand-by ↔RX stand-by ↔TX	f_{PULL}				kHz
Frequency pushing	against V_{CC}, CPC = 2	f_{PUSH}		1.5		MHz/V
Frequency drift	per slot of 417 µs	f_{DRIFT}			7.5	kHz
Modulation pushing	modulation deviation against V_{CC}	f_{MPUSH}				kHz/V
Modulation tuning sensitivity	modulation deviation against V_T	f_{MSEN}				kHz/V
Analog modulation voltage [a]	± 144 kHz see table below	V_{MOD}		± 375		mVpk

(a). The input analog signal is expected to vary between 0V and 0.75V
Pre-modulation and post-modulation, it is expected to have a level of 0.375.

Typical TX VCO analog modulation voltage table.

Channel No	Supply voltage	Condition	Symbol	-20°C	20°C	70°C	Unit
0	V_{CC} = 2.7	For ± 144 kHz	V_{MOD27}	239	± 222	211	mVpk
31				223	± 208	200	
0	V_{CC} = 3.3	For ± 144 kHz	V_{MOD33}	370	± 339	320	mVpk
31				344	± 315	299	
0	V_{CC} = 3.6	For ± 144 kHz	V_{MOD36}	460	± 419	395	mVpk
31				426	± 390	369	

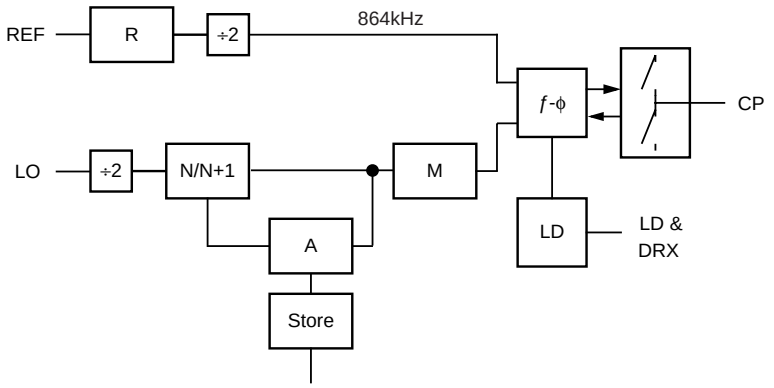
RX VCO.

A fully integrated balanced VCO. The VCO frequency is controlled by the voltage applied to the VTUNE pin, and has a negative sensitivity, i.e., as the voltage increases, the VCO frequency decreases. The tuning voltage is referenced to V_{CC}VCO. The VCO is buffered to provide isolation against frequency pulling and reverse injection.
A divider by 2 stage, reduces the VCO frequency by 2 for the PLL.

RX VCO Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Carrier frequency range	$0.4 \leq V_T \leq V_{CC}-0.4$	f_C	3.53		3.65	GHz
Tuning voltage		V_T	0.4		V_{CC}-0.4	V
Frequency sensitivity		f_{SEN}	~-100	~-280	~-460	MHz/V
Frequency pulling	stand-by ↔RX stand-by ↔TX	f_{PULL}				kHz
Frequency pushing	against V_{CC} , CPC = 2	f_{PUSH}		1,0		MHz/V
Noise floor	nominal output power	N_{FLR}			-140	dBc/Hz

The PLL.



The frequency synthesiser is based on a charge pump PLL (Phase Locked Loop).
Counter R divides the reference clock, REF. The division ratio, R, is determined by the value of CNT_R. Counters N, A and M form a modulus pulse swallow counter which divides the LO clock by M∗N+A . The value of M is determined by CNT_M. The value of A is taken from the CNT_A.

A combined 3 state frequency-phase detector compares the divided REF and LO signals and controls the charge pump.The frequency-phase comparator outputs are controlled by the CPC1-0 bits and MOD_EN. The action of the CPC bits are unsynchronised. The action of MOD_EN is synchronised to the charge pump states, holding the charge pump in tri-state mode when MOD becomes active.

An active high lock detect signal is provided when frequency lock has been achieved for 148 µs. The signal is available on the LD pin and on the DRX pin when SYN_EN is active and neither of RX_EN or TX_EN are active.

The PLL is designed to work with two different reference frequencies, 10.368 MHz (= 9 x the DECT bitrate of 1.152 MHz) or 13.824 MHz (= 12 x the DECT bitrate of 1.152 MHz)

The synthesiser frequency is given by, $f_{RF} = (f_{REF} / R) (M * N+A)$

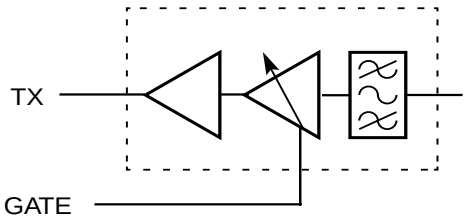
where: f_{RF} = RF frequency
f_{REF} = either 10.368 MHz or 13.824 MHz
R = 6 or 8 (see CNT_R)
M = 32 or 34 (see CNT_M)
N = 32
A = 0, 1, ...,31

PLL Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Carrier frequency range	$0.4 \leq V_T \leq V_{CC}-0.4$	f_C	1769		1934	MHz
Lock time (1)		t_{LOCK}			320	µs
Charge pump current		I_{CP}		400		µA
Charge pump leakage	tri-state	I_{LEAK}		100		pA
Reference frequency	CNT_R=0	f_{REF}		10.368		MHz
	CNT_R=1			13.824		
Reference input voltage		V_{REF}	50			mVpk

(1). Depends upon charge pump loop components.

Transmit section.



Description.

The transmitter consists of a band-pass filter, a gated amplifier and a pre-power amplifier. The band-pass filter cleans the output signal of the LO modulator prior to amplification.

The gated amplifier is controlled by the GATE pin, with signal polarity determined by the GATE_P flag. The attenuation of the gating amplifier should be used in addition to the external PA to meet the transmit power ramp requirements. An active GATE signal causes the output power to ramp up to its required power level. An inactive GATE signal causes the output power to ramp down to a leakage level. Spectral spreading requirements are best met if the external PA turns on before the power ramp up, and turn off after the power ramp down. Should the external PA be controlled by the same GATE signal, a delayed copy of the GATE signal is provided at the PA _GATE output.

The TX output is balanced with an impedance of ~100 Ω and requires external inductors to V_{CC}RF. The transmit power may be trimmed by the TX_P 0-1 bits.

The TX is designed for easy interfacing to the PBL 403 09 DECT PA circuit, which is enabled with an active low signal. See application diagram for details.

Transmit section Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Frequency range at output		f	1800		2000	MHz
Nominal output power	Gate enable	P_{NOM}		5		dBm
Output power	Gate disable	P_{OFF}		-22		dBc
Power of 2xLO spurious		P_{2LO}		-35	-20	dBc
Power of 3xLO spurious		P_{3LO}		-35	-20	dBc
Output power trim about nominal	TX_P1, 0=0, 0	P_{TRIM}		-1.3		dB
	TX_P1, 0=0, 1			0		
	TX_P1, 0=1, 0			+1.3		
	TX_P1, 0=1, 1			+1.9		
P_{OFF} to P_{NOM} time		t_{ON}		2	5	µs
P_{NOM} to P_{OFF} time		t_{OFF}		2	5	µs
Gate active to PA_GATE active		t_{PAON}		100	200	ns
Gate inactive to PA_GATE inactive		t_{PAOFF}		3	6	µs
Noise floor	nominal output power	N_{FLR}			-135	dBm/Hz
Noise at channel M±1	f±1.728 MHz	N_{M1}			-93	dBc
Noise at channel M±2	f±3.456 MHz	N_{M2}			-115	dBc
Noise at channel M±3	f±5.184 MHz	N_{M3}			-129	dBc
Noise at channel M±4	f±6.912 MHz	N_{M4}			-132	dBc
Output impedance		Z_{OUT}		100		Ω
Output VSWR		$VSWR_O$			1.5:1	-

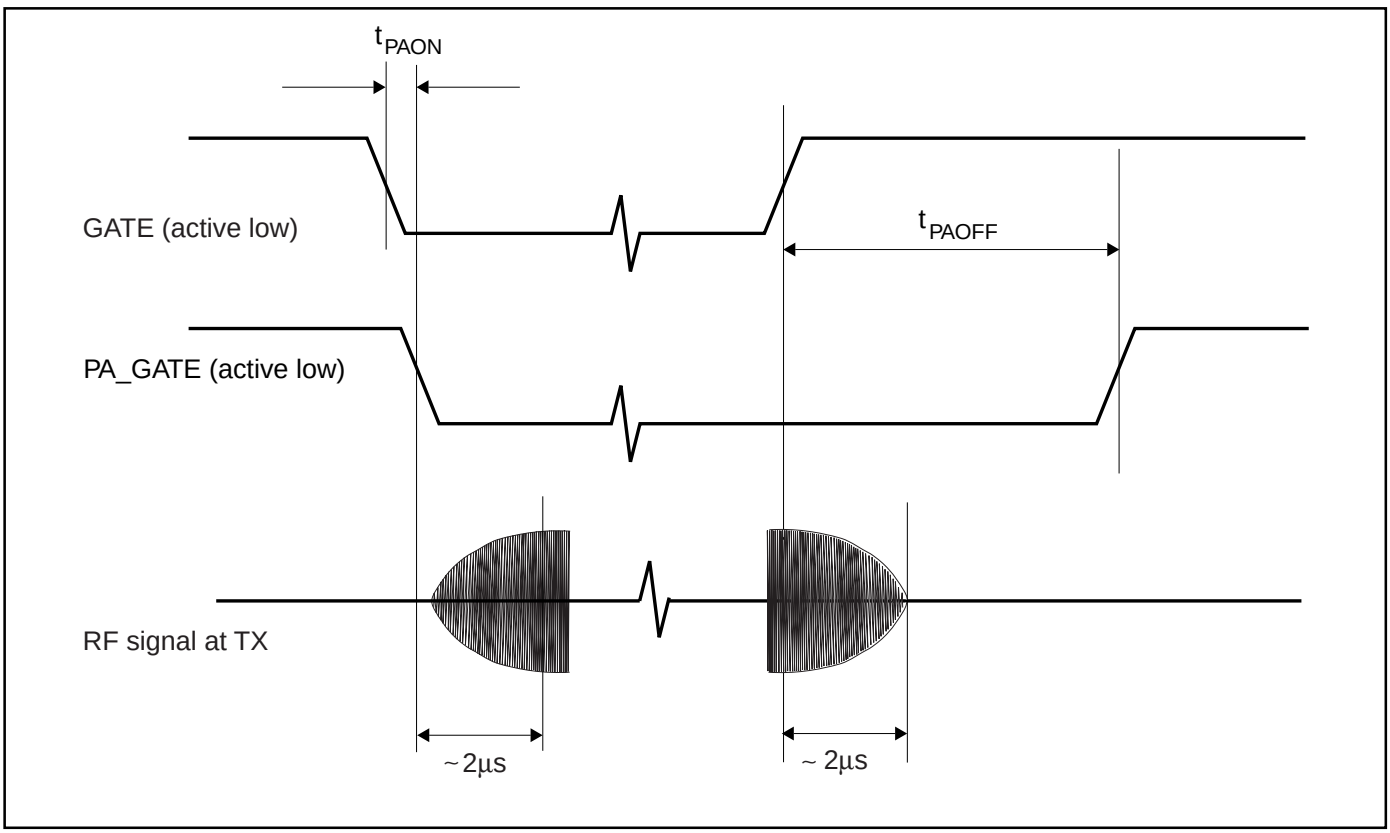
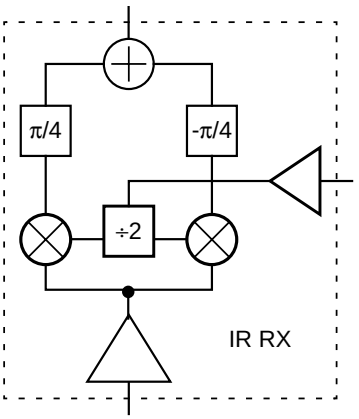


Figure 10. GATE / PA_GATE timing diagram, GATE_P = 0.

Image Reject Front End.



The image reject front end consists of an LNA (Low Noise Amplifier) with dual outputs, 2 mixers, quadrature LO generation, 2 low pass filters, a +π/4 and a -π/4 all-pass filters and a summing output stage.

The receiver input is a 1.9 GHz LNA with a characteristic balanced input impedance. The inputs are self biassing and require external matching to the source, with DC blocking capacitors if the source passes DC.

The high side image rejection mixer, down converts from RF to an IF frequency of 110.6 MHz.

The IF outputs are self biasing and define a balanced output impedance of 300 Ω. The output should be matched to an external adjacent channel filter.

The gain is switchable to cater for the insertion loss of different external filters.

Image Reject Front End Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input frequency range		f_{IN}	1800	1890	2000	MHz
Output frequency range		f_{OUT}	100	110.6	120	MHz
Gain 1	RX_G = 0	G1	18	20	22	dB
Gain 2	RX_G = 1	G2	23	25	27	dB
Input IP3	RX_G = 0 RX_G = 1	IP3	-21	-17 -23		dBm
Input 1 dB compression	RX_G = 0 RX_G = 1	CPI1		-24 -31		dBm
Output 1 dB compression		CPO1		-7		dBm
Output saturation				-1.5		dBm
Lower image suppression	Tested at f_{IN} -2•110.6 MHz	SSB	29	35		dB
Noise figure		NF		3.6	4.1	dB
Input impedance		Z_{IN}		100		Ω
Output impedance		Z_{OUT}		300		Ω
Input VSWR		$VSWR_I$			1.5:1	-
Output VSWR		$VSWR_O$			1.5:1	-

IF Receiver.

The IF receiver consists of an upper sideband image reject down converter, a channel blocking filter, a limiting amplifier and RSSI, an FM discriminator, a post detection filter and a data slicer.

The IF inputs are self biasing and have a balanced input impedance of 300 Ω. Matching to the external filter is required. A band-pass filter provides additional channel selection and noise filtering prior to the limiting chain.

The quadrature based FM discriminator and post detection filter are self tuned to the required frequency by a slave PLL.

The FSK data is recovered by a threshold based data slicer. The slice level is determined up to the end of the 16 bit packet preamble, where it should be held by an active SHOLD signal provided from the base-band controller. The slice controller determines a more accurate level from this signal. An external capacitor is required on the DSL pin.

IF ReceiverTable.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Frequency range		f_{IF}		110.6		MHz
Input IP3		IP3	-13			dBm
Input 1dB compression		CP1	-15	-13		dBm
Lower image suppression	Tested at f_{IF} -23.5 MHz	SSB	29			dB
Noise figure	Referenced to 300 Ω	NF			14	dB
Sensitivity	BER = 10^{-3}	SENS	-79			dBm
Input impedance		Z_{IN}		300		Ω
Input VSWR		$VSWR_I$			1.5:1	-
Attenuation of channel M±1	>f_C ± 1.152 MHz	ATT1				
Attenuation of channel M±2	>f_C ± 2.88 MHz	ATT2				
Attenuation of channel M±3	>f_C ± 4.608 MHz	ATT3				
Attenuation of channel M±4	>f_C ± 6.336 MHz	ATT4				
Group delay deviation	f_C ± 576 kHz	GDD			0.3	µs
Slice hold capacitor	On DSL pin to Gnd	C_{DSL}		2		nF

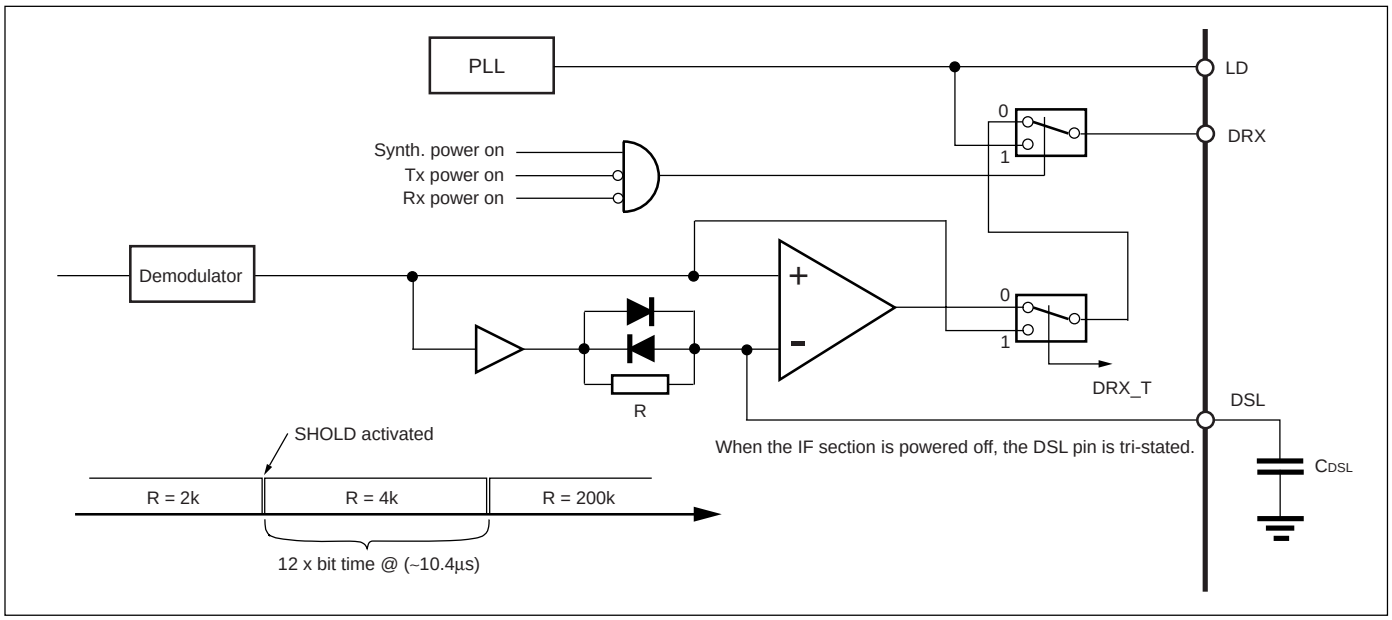


Figure 11. Slice control.

Limiting Amplifier and RSSI (Received Signal Strength Indicator).

The stage consists of a limiting amplifier chain with an RSSI detector. The inputs are internally coupled from the channel selection filter which limits the noise bandwidth. A balanced DC offset correction loop, provides maximum sensitivity, and ensures a short settling time upon power up.

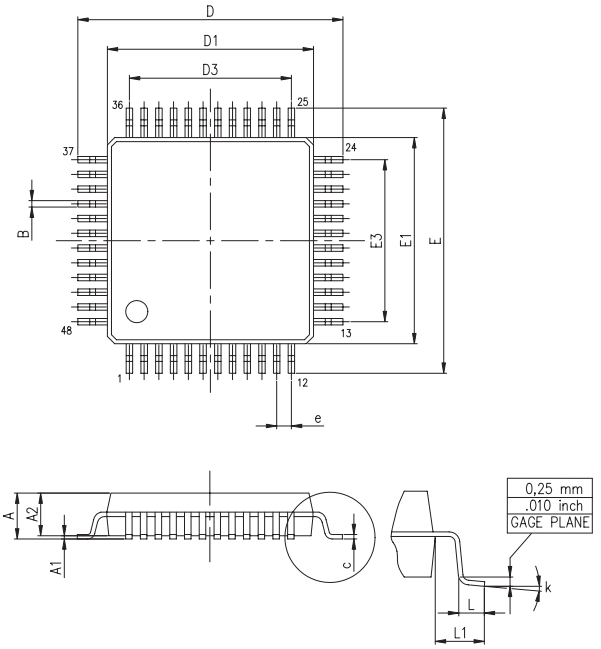
An RSSI output provides a voltage proportional to the logarithm of the rectified input level. The rise time response of the RSSI output and the peak hold is dependent upon the external circuit.

Limiting Amplifier strip and RSSI, Table.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Frequency range		f		11.7		MHz
Limiter 1 dB bandwidth		f_{1dB}	22			MHz
Voltage gain		G		74		dB
RSSI range		R_R	74			dB
RSSI minimum detection level	measured at IFIN	RD_{MIN}			-83	dBm
RSSI maximum detection level	measured at IFIN	RD_{MAX}	-9			dBm
RSSI slope		R_{SLOPE}		15.2		mV/dB
Zero scale RSSI output voltage		VR_{ZERO}		375		mVpk
Full scale RSSI output voltage		VR_{FULL}		1500		mVpk
RSSI relative error	best fit to straight line [a]	R_{ERR}			±2.5	dB
RSSI rise time	20 pF load	t_{RISE}		2		µs
Feedback capacitance		C_{CAP}		18		nF

a. The RSSI relative accuracy is the deviation of the RSSI value from a best fit straight line fitted to several calibration points. These points are determined for each part.

TQFP 48 Pin Package



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.006	0.008	0.010
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.217	
e		0.50			0.020	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.217	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

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