

SURFACE MOUNT SCR

<p>DPAK (Plastic)</p>	<p>On-State Current 8 Amp</p> <p>Gate Trigger Current 0.5 to 15 mA</p> <p>Off-State Voltage 200 V ÷ 600 V</p>
	<p>These series of Silicon Controlled Rectifier use a high performance PNP technology.</p> <p>These parts are intended for general purpose applications where high gate sensitivity is required using surface mount technology.</p>

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 110\text{ °C}$		8	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $= 180\text{ °}, T_c = 110\text{ °C}$		5	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz		73	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz		70	A
I^2t	Fusing Current	$t_p = 10\text{ms}$, Half Cycle		24.5	A ² s
V_{GRM}	Peak Reverse Gate Voltage	$I_{GR} = 10\text{ }\mu\text{A}$		5	V
I_{GM}	Peak Gate Current	20 μs max.		4	A
P_{GM}	Peak Gate Dissipation	20 μs max.		5	W
$P_{G(AV)}$	Gate Dissipation	20ms max.		1	W
T_j	Operating Temperature		-40	+125	°C
T_{stg}	Storage Temperature		-40	+150	°C
T_{sld}	Soldering Temperature	10s max.		260	°C

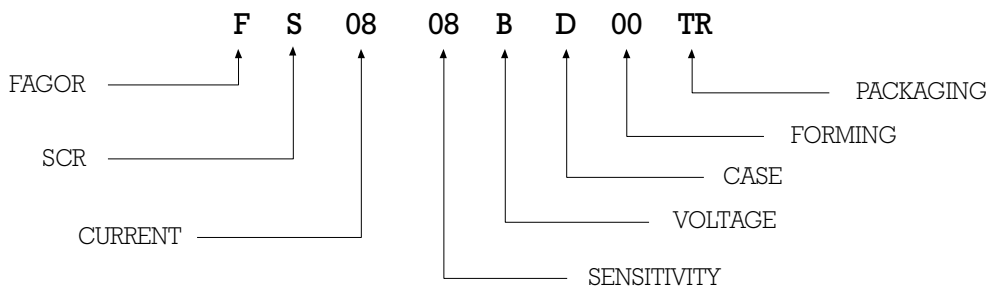
SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	$R_{GK} = 1\text{ K}$	200	400	600	V

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Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	SENSITIVITY		Unit	
			08	09		
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 33 \Omega, T_j = 25^\circ C$	MIN MAX	0.5 5	2 15	mA
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, T_j = 125^\circ C$ $V_R = V_{RRM}, T_j = 25^\circ C$	MAX MAX	2 5		mA μA
V_{TM}	On-state Voltage	at $I_T = 16 \text{ Amp}, t_p = 380 \mu s, T_j = 25^\circ C$	MAX	1.6		V
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 33 \Omega, T_j = 25^\circ C$	MAX	1.3		V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3K \Omega, T_j = 125^\circ C$	MIN	0.2		V
I_H	Holding Current	$I_T = 100 \text{ mA}, \text{ Gate open}$	MAX	25	40	mA
I_L	Latching Current	$I_G = 1.2 I_{GT}, T_j = 25^\circ C$	MAX	30	50	mA
dv / dt	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open}$	MIN	50	150	V/ μs
di / dt	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, T_r = 100 \text{ ns}, F = 60 \text{ Hz}, T_j = 125^\circ C$	MIN	50		A/ μs
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC			20		$^\circ C/W$
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S = 0.5 \text{ cm}^2$		70		$^\circ C/W$
V_{T0}	Threshold Voltage	$T_j = 125^\circ C$	MAX	0.85		V
R_d	Dynamic resistance	$T_j = 125^\circ C$	MAX	46		m

S = Cooper surface under tab



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Fig. 1: Maximum average power dissipation versus average on-state current.

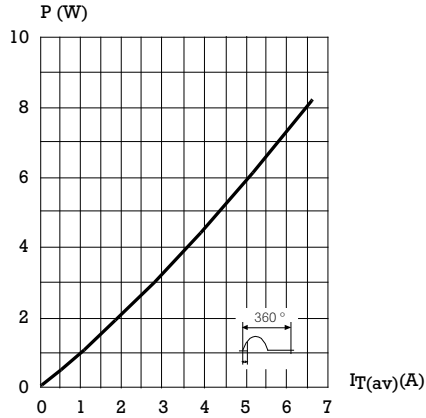


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration.

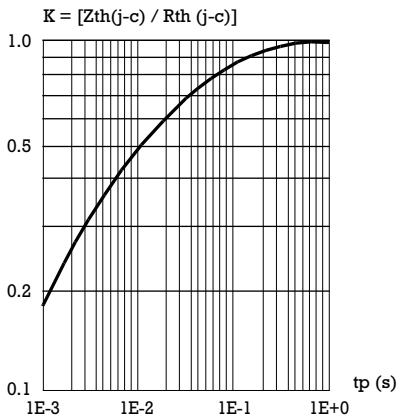


Fig. 5: Non repetitive surge peak on-state current versus number of cycles.

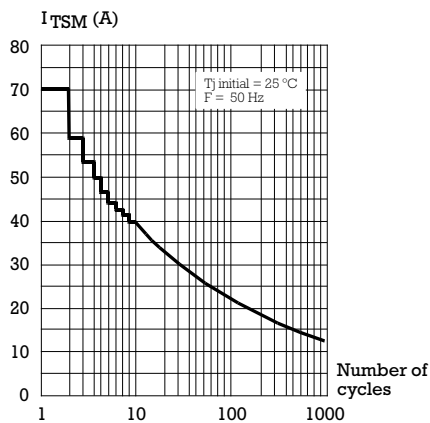


Fig. 2: Average and D.C. on-state current versus case temperature.

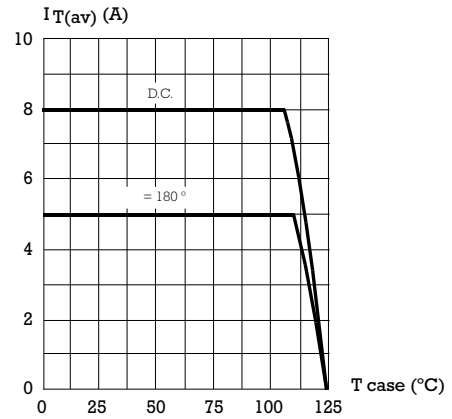
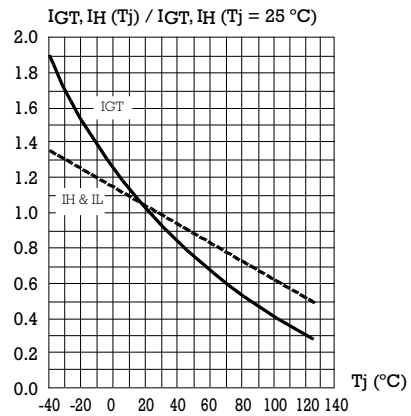
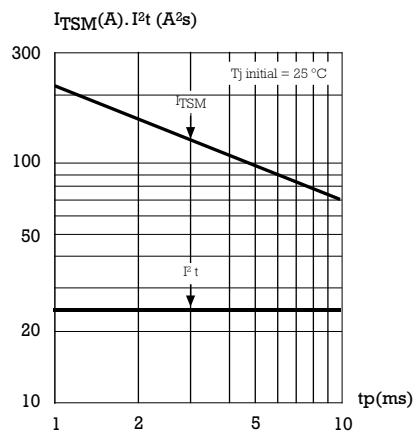
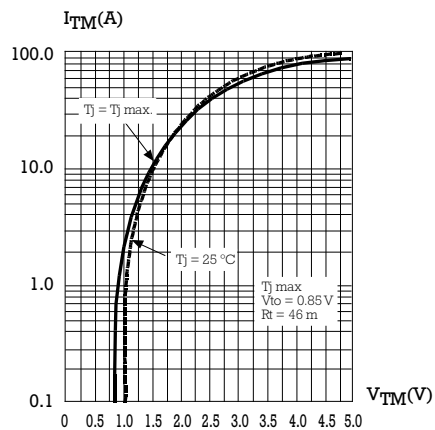


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature.

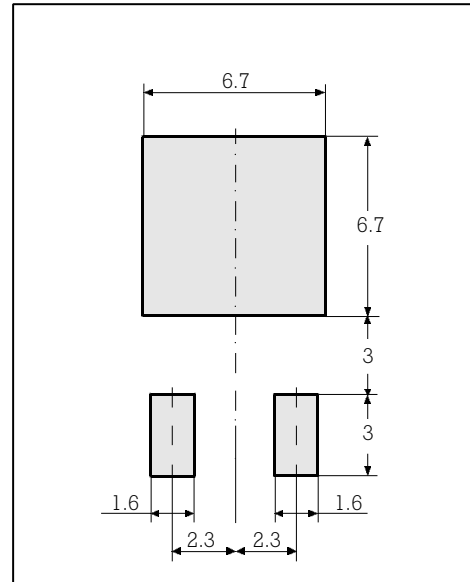

 Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10$ ms, and corresponding value of I^2t .


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Fig. 8: On-state characteristics (maximum values).



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PACKAGE MECHANICAL DATA DPAK TO 252-AA

REF.	DIMENSIONS		
	Millimeters		
	Min.	Nominal	Max.
A	2.18	2.3±0.18	2.39
A1	0	0.12	0.127
b	0.64	0.75±0.1	0.89
c	0.46		0.61
c1	0.46		0.56
c2		0.8±0.013	
D	5.97	6.1±0.1	6.22
D1	5.21		5.52
E	6.35	6.58±0.14	6.73
E1	5.20	5.36±0.1	5.46
e		2.28BSC	
H	9.40	9.90±0.15	10.41
L	1.40		1.78
L1	2.55	2.6±0.05	2.74
L2	0.46	0.5±0.013	0.58
L3	0.89	1.20±0.05	1.27
L4	0.64	0.83±0.1	1.02

Marking: type number
Weight: 0.2 g