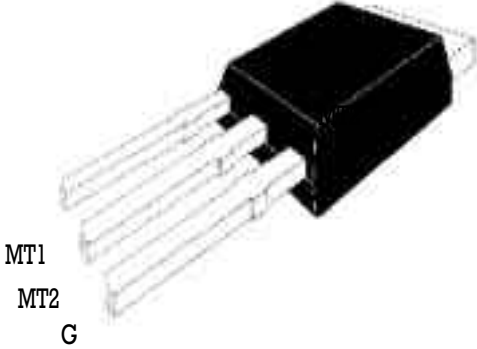


LOGIC LEVEL TRIAC

IPAK (Plastic)	<p>On-State Current 4 Amp</p> <p>Gate Trigger Current < 5 mA to < 10 mA</p> <p>Off-State Voltage 200 V ÷ 600 V</p>
	<p>This series of TRIACs uses a high performance PNPN technology.</p> <p>These parts are intended for general purpose applications where logic compatible gate sensitivity is required, like touch dimmers, fan, electrovalve control.</p>

Absolute Maximum Ratings, according to IEC publication No. 134

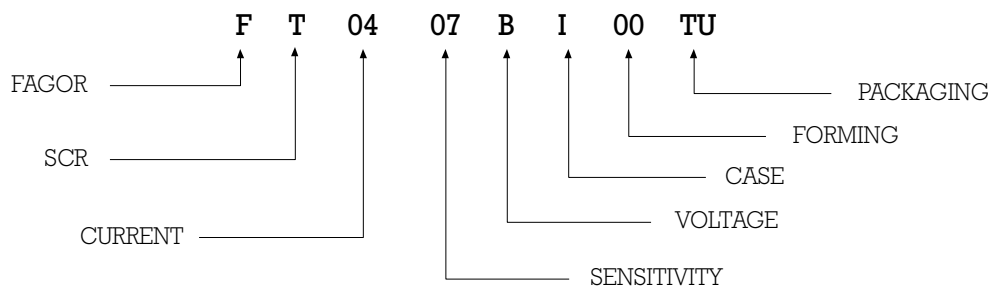
SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	RMS On-state Current	All Conduction Angle, $T_c = 110\text{ }^\circ\text{C}$	4		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	31		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz	30		A
I^2t	Fusing Current	$t_p = 10\text{ ms}$, Half Cycle	5.1		A ² s
I_{GM}	Peak Gate Current	20 μs max.		4	A
P_{GM}	Peak Gate Dissipation	20 μs max.		3	W
$P_{G(AV)}$	Gate Dissipation	20 ms max.		1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$ Tr 100 ns, F = 120 Hz $T_j = 125\text{ }^\circ\text{C}$	50		A/ μs
T_j	Operating Temperature		-40	+125	$^\circ\text{C}$
T_{stg}	Storage Temperature		-40	+150	$^\circ\text{C}$
T_{sld}	Soldering Temperature	4.5 mm from case, 10s max.		260	$^\circ\text{C}$

SYMBOL	PARAMETER	VOLTAGE			Unit
		B	D	M	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	V

LOGIC LEVEL TRIAC
Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					07	08	
I_{GT}	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 30 \Omega, T_j = 25^\circ C$	Q1÷Q3 Q4	MAX MAX	5 7	10	mA
I_{DRM} / I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}, T_j = 125^\circ C$ $V_R = V_{RRM}, T_j = 25^\circ C$		MAX MAX	1 5		mA μA
V_{to}	Threshold Voltage	$T_j = 125^\circ C$		MAX	0.9		V
R_d	Dynamic Resistance	$T_j = 125^\circ C$		MAX	120		m
V_{TM}^*	On-state Voltage	$I_T = 5.5 \text{ Amp}, t_p = 380 \mu s, T_j = 25^\circ C$		MAX	1.6		V
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 30 \Omega, T_j = 25^\circ C$	Q1÷Q3	MAX	1.3		V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3K \Omega, T_j = 125^\circ C$	Q1÷Q3	MIN	0.2		V
I_H^*	Holding Current	$I_T = 100 \text{ mA}, \text{ Gate Open } T_j = 25^\circ C$		MAX	10	15	mA
I_L	Latching Current	$I_G = 1.2 I_{GT}, T_j = 25^\circ C$	Q1,Q3,Q4 Q2	MAX MAX	10 15	20 30	mA
dv / dt^*	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open } T_j = 125^\circ C$		MIN	20	100	V/ μs
$R_{th(j-c)}$	Thermal Resistance Junction-Case for AC				2.6		$^\circ C/W$
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient				100		$^\circ C/W$

(*) For either polarity of electrode MT2 voltage with reference to electrode MT1.

PART NUMBER INFORMATION


LOGIC LEVEL TRIAC

Fig. 1: Maximum RMS power dissipation versus RMS on-state current.

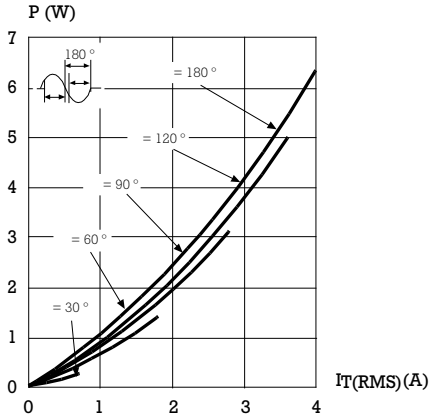


Fig. 3: RMS on-state current versus case temperature.

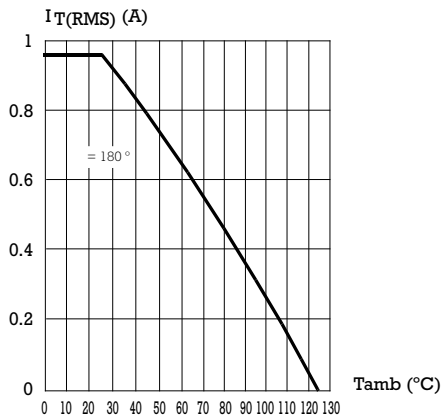


Fig. 5: Relative variation of gate trigger current and holding current versus junction temperature.

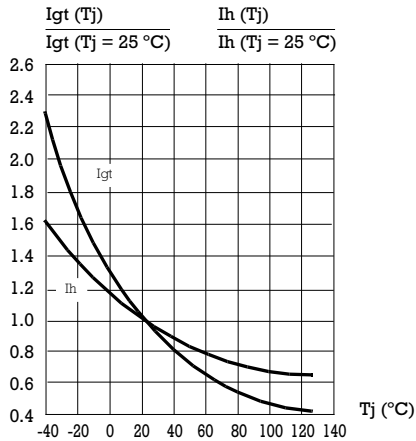


Fig. 2: Correlation between maximum RMS power dissipation and maximum allowable temperature (Tamb and T case).

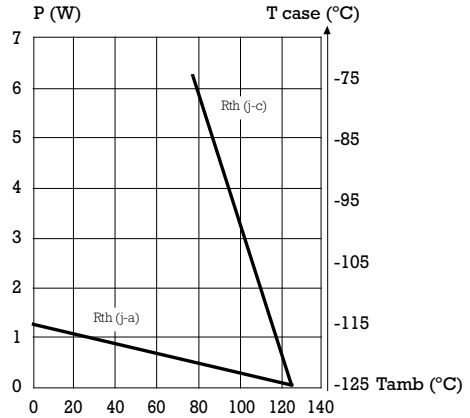


Fig. 4: Relative variation of thermal impedance junction to ambient versus pulse duration.

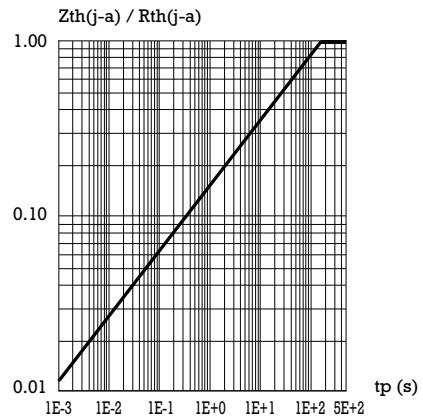
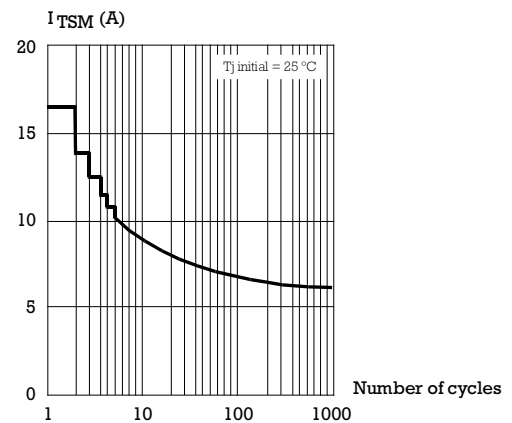


Fig. 6: Non repetitive surge peak on-state current versus number of cycles.



LOGIC LEVEL TRIAC

Fig. 7: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p = 10$ ms, and corresponding value of I^2t .

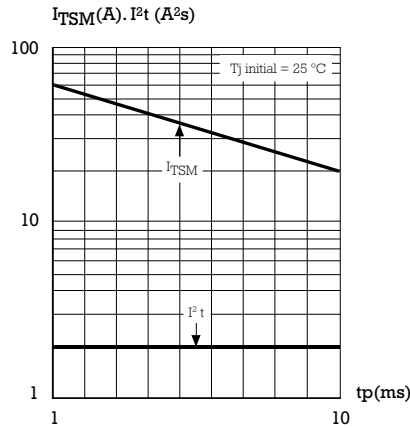
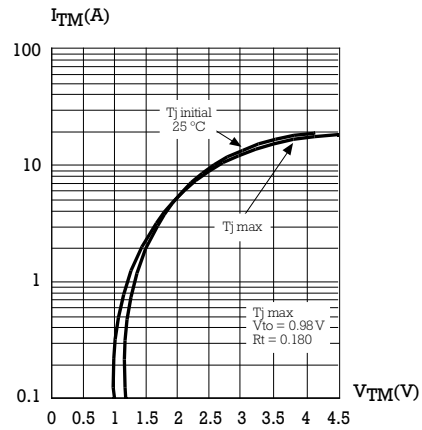


Fig. 8: On-state characteristics (maximum values).



PACKAGE MECHANICAL DATA IPAK TO 251-AA

REF.	DIMENSIONS		
	Millimeters		
	Min.	Nominal	Max.
A	2.19	2.3±0.08	2.38
A1	0.89	1.067±0.01	1.14
b	0.64	0.75±0.1	0.89
b1	0.76	0.95	1.14
c	0.46		0.58
c2		0.8±0.013	
D	5.97	6.1±0.1	6.22
D1	5.21		5.52
E	6.35	6.58±0.14	6.73
E1	5.21	5.36±0.1	5.46
e		2.28BSC	
L	8.89	9.2±0.2	9.65
L1	1.91	2±0.1	2.28
L3	0.89		1.27

Marking: type number
Weight: 0.2 g