

## 74ABT646

### Octal Transceivers and Registers with 3-STATE Outputs

#### General Description

The ABT646 consists of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\overline{OE}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\overline{OE}$  is Active LOW. In the isolation mode (control  $\overline{OE}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

#### Features

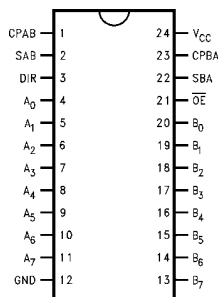
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

#### Ordering Code:

Order Number	Package Number	Package Description
74ABT646CSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-153, 4.4mm Wide
74ABT646CMSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT646CMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs/3-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs/3-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

**Truth Table**

Inputs						Data I/O (Note 1)		Function
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X			Isolation
H	X	↘	X	X	X	Input	Input	Clock A <sub>n</sub> Data into A Register
H	X	X	↘	X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X	Input	Output	A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	↘	X	L	X			Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	↘	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L	Output	Input	B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	↘	X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	↘	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↘ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

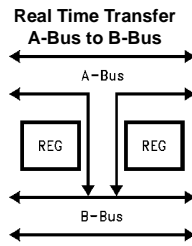


FIGURE 1.

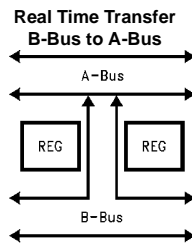


FIGURE 2.

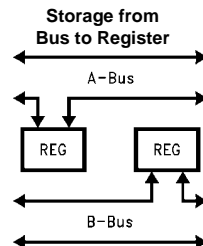


FIGURE 3.

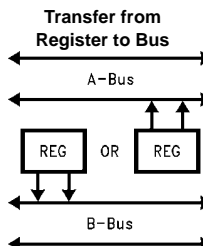
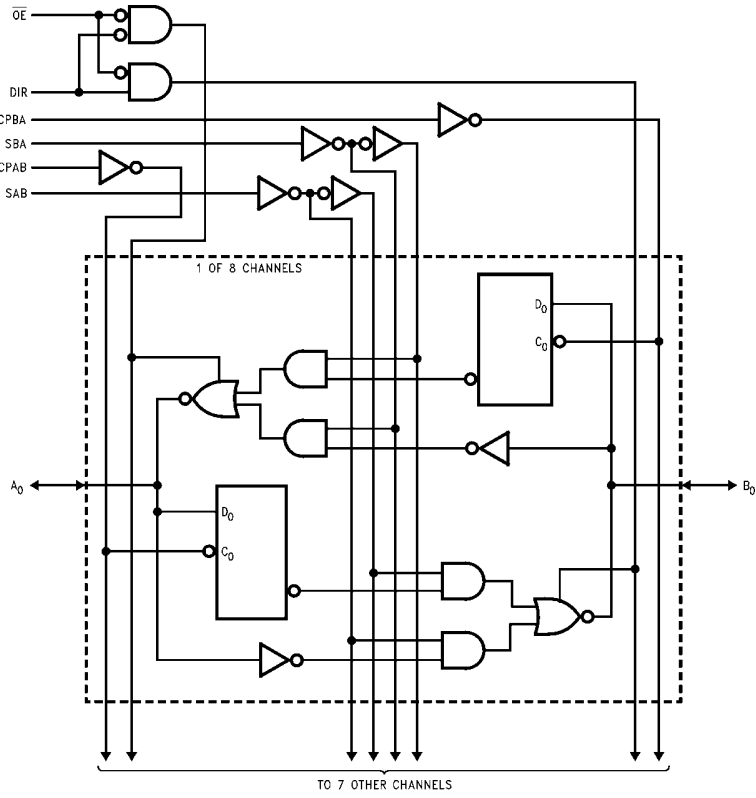


FIGURE 4.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

**Recommended Operating Conditions**

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	2.5					I <sub>OH</sub> = -3 mA, (A <sub>n</sub> , B <sub>n</sub> ) I <sub>OH</sub> = -32 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage			0.55			I <sub>OL</sub> = 64 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 $\mu$ A, (Non-I/O Pins) All Other Pins Grounded
I <sub>IH</sub>	Input HIGH Current			1	$\mu$ A	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins) (Note 4) V <sub>IN</sub> = V <sub>CC</sub> (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	$\mu$ A	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			100	$\mu$ A	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current			-1	$\mu$ A	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins) (Note 4) V <sub>IN</sub> = 0.0V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			10	$\mu$ A	0V-5.5V	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-10	$\mu$ A	0V-5.5V	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	$\mu$ A	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			100	$\mu$ A	0.0V	V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> ); All Others GND
I <sub>CCH</sub>	Power Supply Current			250	$\mu$ A	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	$\mu$ A	Max	Outputs 3-STATE; All Others GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input			2.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Other Outputs at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 4)	No Load		0.18	mA/MHz	Max	Outputs OPEN $\overline{OE}$ and DIR = GND, Non-I/O = GND or V <sub>CC</sub> (Note 5) One Bit toggling, 50% duty cycle

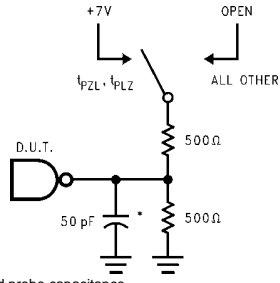
**Note 4:** Guaranteed but not tested.

**Note 5:** For 8-bit toggling, I<sub>CCD</sub> < 1.4 mA/MHz.

DC Electrical Characteristics									
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.6	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 6)		
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.2	-0.9		V	5.0	T <sub>A</sub> = 25°C (Note 6)		
V <sub>OHV</sub>	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T <sub>A</sub> = 25° (Note 7)		
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	2.2	1.8		V	5.0	T <sub>A</sub> = 25°C (Note 8)		
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage		0.8	0.5	V	5.0	T <sub>A</sub> = 25°C (Note 8)		
<p><b>Note 6:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.</p> <p><b>Note 7:</b> Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.</p> <p><b>Note 8:</b> Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.</p>									
AC Electrical Characteristics									
(SOIC and SSOP package)									
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	200			200		200		MHz
t <sub>PLH</sub>	Propagation Delay	1.7	3.0	5.6	2.2	8.8	1.7	5.6	ns
t <sub>PHL</sub>	Clock to Bus	1.7	3.4	5.6	1.7	8.8	1.7	5.6	ns
t <sub>PLH</sub>	Propagation Delay	1.5	2.6	4.8	1.5	7.9	1.5	4.8	ns
t <sub>PHL</sub>	Bus to Bus	1.5	3.0	4.8	1.5	7.9	1.5	4.8	ns
t <sub>PLH</sub>	Propagation Delay	1.5	3.0	5.9	1.5	8.1	1.5	5.9	ns
t <sub>PHL</sub>	SBA or SAB to A <sub>n</sub> to B <sub>n</sub>	1.5	3.4	5.9	1.5	8.9	1.5	5.9	ns
t <sub>PZH</sub>	Enable Time	1.5	3.2	6.3	1.0	7.3	1.5	6.3	ns
t <sub>PZL</sub>	$\overline{\text{OE}}$ to A <sub>n</sub> or B <sub>n</sub>	1.5	3.5	6.3	1.9	8.8	1.5	6.3	ns
t <sub>PHZ</sub>	Disable Time	1.5	3.7	6.0	1.5	9.3	1.5	6.0	ns
t <sub>PLZ</sub>	$\overline{\text{OE}}$ to A <sub>n</sub> or B <sub>n</sub>	1.5	3.2	6.0	1.5	9.3	1.5	6.0	ns
t <sub>PZH</sub>	Enable Time	1.5	3.4	6.3	1.0	7.7	1.5	6.3	ns
t <sub>PZL</sub>	DIR to A <sub>n</sub> or B <sub>n</sub>	1.5	3.7	6.3	2.2	9.5	1.5	6.3	ns
t <sub>PHZ</sub>	Disable Time	1.5	3.8	6.0	1.5	8.7	1.5	6.0	ns
t <sub>PLZ</sub>	DIR to A <sub>n</sub> or B <sub>n</sub>	1.5	3.2	6.0	1.5	9.2	1.5	6.0	ns
AC Operating Requirements									
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		Units	
		Min	Max	Min	Max	Min	Max		
t <sub>S</sub> (H) t <sub>S</sub> (L)	Setup Time, HIGH or LOW Bus to Clock	1.5		1.5	3.0	1.5		ns	
t <sub>H</sub> (H) t <sub>H</sub> (L)	Hold Time, HIGH or LOW Bus to Clock	1.0		1.0	1.0	1.0		ns	
t <sub>W</sub> (H) t <sub>W</sub> (L)	Pulse Width, HIGH or LOW	3.0		3.0	4.0	3.0		ns	

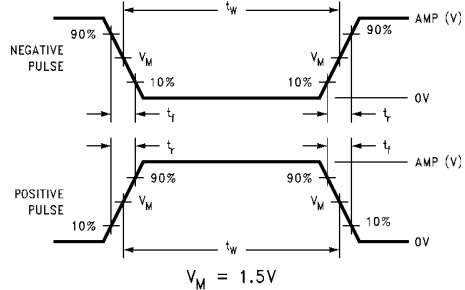
Extended AC Electrical Characteristics								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 9)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 1 Output Switching (Note 10)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 11)		Units
		Min	Max	Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay	1.5	5.5	2.0	7.5	2.5	10.0	ns
$t_{PHL}$	Clock to Bus	1.5	5.5	2.0	7.5	2.5	10.0	
$t_{PLH}$	Propagation Delay	1.5	6.0	2.0	7.0	2.5	9.5	ns
$t_{PHL}$	Bus to Bus	1.5	6.0	2.0	7.0	2.5	9.5	
$t_{PLH}$	Propagation Delay	1.5	6.0	2.0	7.5	2.5	10.0	ns
$t_{PHL}$	SBA or SAB to $A_n$ or $B_n$	1.5	6.0	2.0	7.5	2.5	10.0	
$t_{PZH}$	Output Enable Time	1.5	6.0	2.0	8.0	2.5	10.5	ns
$t_{PZL}$	$\overline{OE}_n$ or DIR to $A_n$ or $B_n$	1.5	6.0	2.0	8.0	2.5	10.5	
$t_{PHZ}$	Output Disable Time	1.5	6.0	(Note 12)		(Note 12)		ns
$t_{PLZ}$	$\overline{OE}_n$ or DIR to $A_n$ or $B_n$	1.5	6.0	(Note 12)		(Note 12)		
<p><b>Note 9:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 10:</b> This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.</p> <p><b>Note 11:</b> This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 12:</b> The 3-STATE delays are dominated by the RC network (500<math>\Omega</math>, 250 pF) on the output and has been excluded from the datasheet.</p>								
Skew								
(SOIC Package)								
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$ 8 Outputs Switching (Note 13)		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 250\text{ pF}$ 8 Outputs Switching (Note 14)		Units		
		Max		Max				
$t_{OSHL}$ (Note 15)	Pin to Pin Skew, HL Transitions	1.3		2.5		ns		
$t_{OSLH}$ (Note 15)	Pin to Pin Skew, LH Transitions	1.0		2.0		ns		
$t_{PS}$ (Note 16)	Duty Cycle, LH-HL Skew	2.0		4.0		ns		
$t_{OST}$ (Note 15)	Pin to Pin Skew, LH/HL Transitions	2.0		4.0		ns		
$t_{PV}$ (Note 17)	Device to Device Skew, LH/HL Transitions	2.5		4.5		ns		
<p><b>Note 13:</b> This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).</p> <p><b>Note 14:</b> This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.</p> <p><b>Note 15:</b> Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (<math>t_{OSHL}</math>), LOW-to-HIGH (<math>t_{OSLH}</math>), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (<math>t_{OST}</math>). This specification is guaranteed but not tested.</p> <p><b>Note 16:</b> This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.</p> <p><b>Note 17:</b> Propagation delay variation for a given set of conditions (i.e., temperature and <math>V_{CC}</math>) from device to device. This specification is guaranteed but not tested.</p>								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$				
$C_{IN}$	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (non I/O pins)				
$C_{I/O}$ (Note 18)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ ( $A_n, B_n$ )				
<p><b>Note 18:</b> <math>C_{I/O}</math> is measured at frequency, <math>f = 1\text{ MHz}</math>, per MIL-STD-883, Method 3012.</p>								

**AC Loading**



\*Includes jig and probe capacitance

**FIGURE 5. Standard AC Test Load**

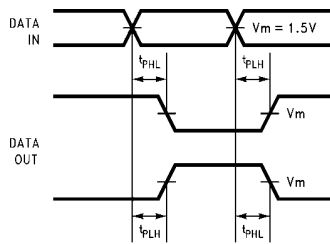


**FIGURE 6. Test Input Signal Levels  
Input Pulse Requirements**

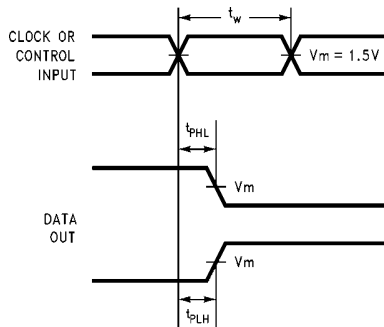
Amplitude	Rep. Rate	$t_W$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**FIGURE 7. Test Input Signal Requirements**

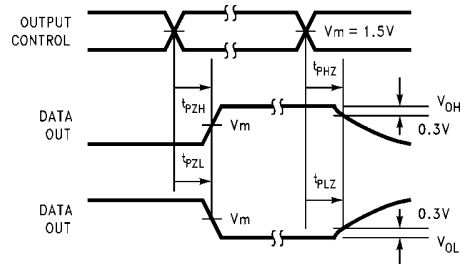
**AC Waveforms**



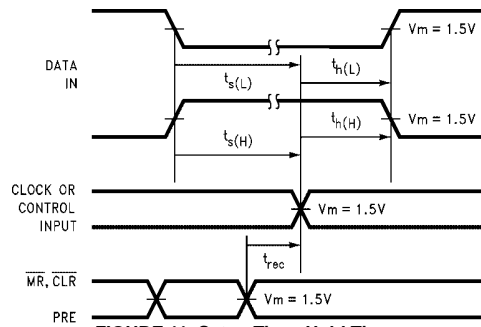
**FIGURE 8. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 9. Propagation Delay,  
Pulse Width Waveforms**

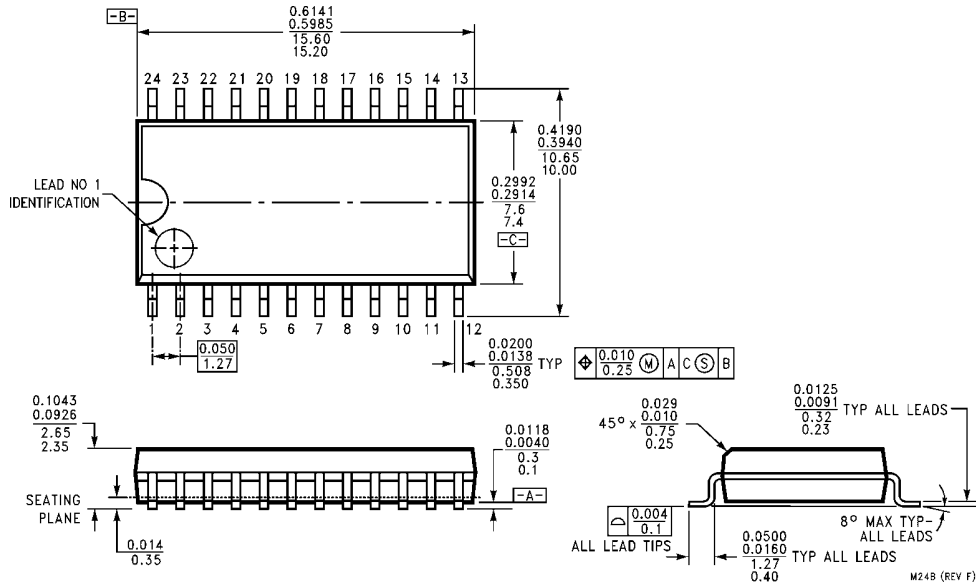


**FIGURE 10. 3-STATE Output HIGH  
and LOW Enable and Disable Times**

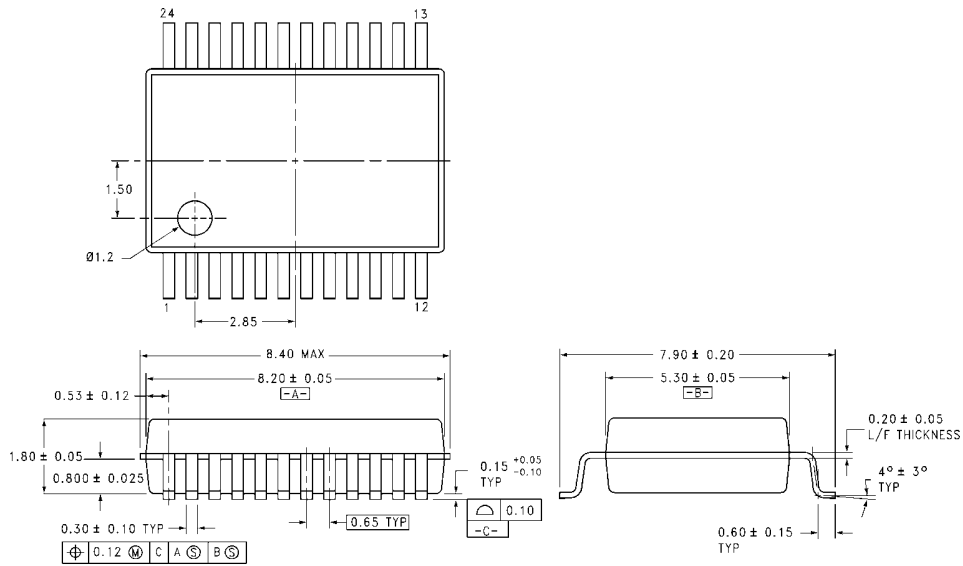


**FIGURE 11. Setup Time, Hold Time  
and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted

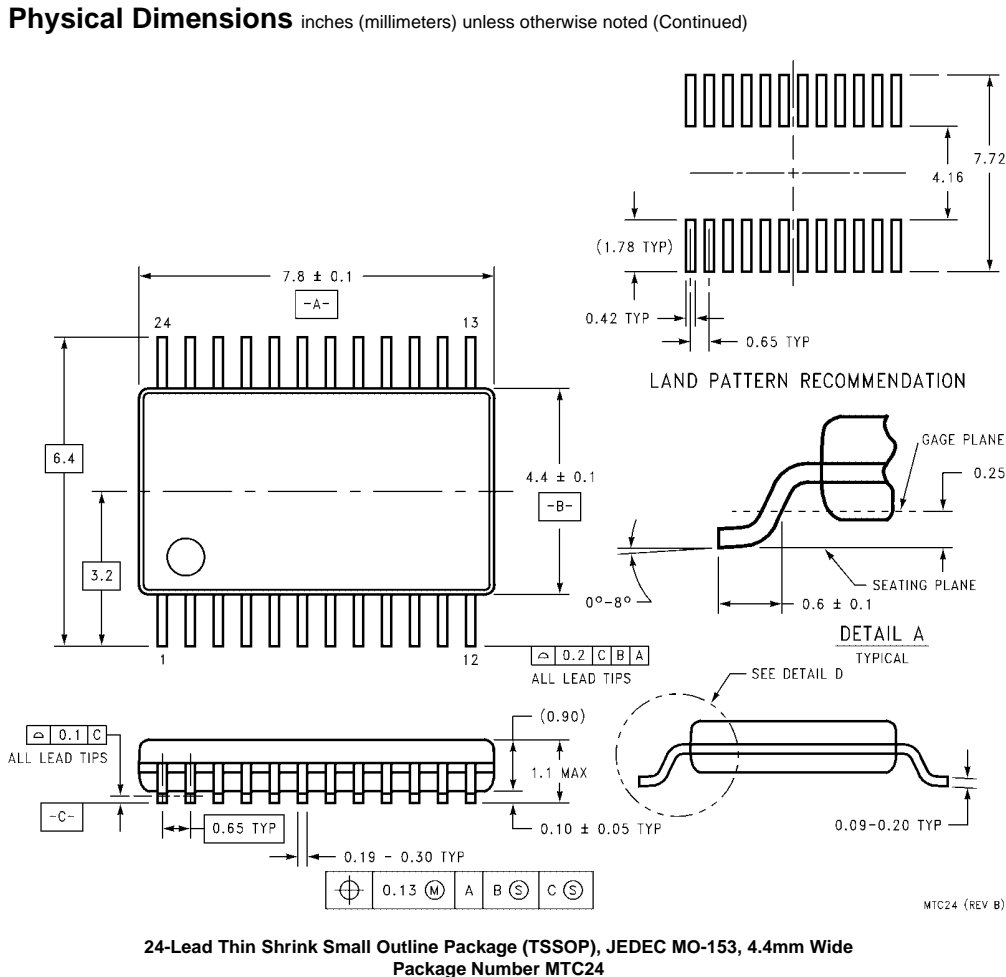


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide Package Number MSA24**





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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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