FAIRCHILD
SEMICONDUCTOR™

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74ACQ241
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The ACQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ utilizes Fairchild FACT Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard AC

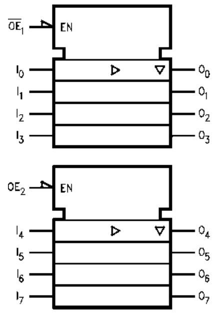
Ordering Code:

Order Number	Package Number	Package Description
74ACQ241SC	M20B	20-Lead Small Outline Integrated Circuit, JEDEC MS-013, 0.300" Wide Body
74ACQ241PC	N20A	20-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

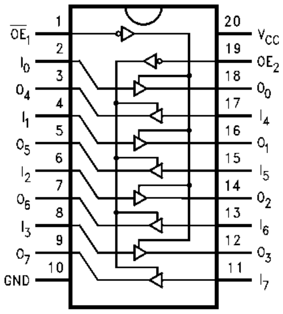
Logic Symbol

IEEE/IEC



Connection Diagram

Pin Assignment for DIP and SOIC



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, OE_2	3-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
OE_2	I_n	(Pins 3, 5, 7, 9)
H	L	L
H	H	H
H	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or	
Sink Current	±300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ΔV/Δt	125 mV/ns
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	$T_A = +25°C$		$T_A = -40°C$ to $+85°C$	Units	Conditions
		(V)	Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	$I_{OUT} = -50\ \mu A$
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic Output Current	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	(Note 3)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	µA	V_I (OE) $= V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	Figures 1, 2 (Note 5)(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	Figures 1, 2 (Note 5)(Note 6)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Note 5)(Note 7)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Note 5)(Note 7)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 5: DIP package.

Note 6: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 7: Max number of Data Inputs (n) switching. n–1 Inputs switching 0V to 5V . Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0	2.0	9.5	ns
		5.0	1.5	4.5	6.0	1.5	6.5	
t_{PZL} t_{PZH}	Output Enable Time	3.3	2.5	8.0	13.0	2.5	13.5	ns
		5.0	1.5	5.5	8.5	1.5	9.0	
t_{PHZ} t_{PLZ}	Output Disable Time	3.3	1.0	8.5	14.5	1.0	15.0	ns
		5.0	1.0	5.5	9.5	1.0	10.0	
t_{OSHL} t_{OSLH}	Output to Output Skew Data to Output (Note 9)	3.3		1.0	1.5		1.5	ns

Note 8: Voltage Range 5.0 is 5.0V ±0.5V. Voltage Range 3.3 is 3.3V ±0.3V.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope

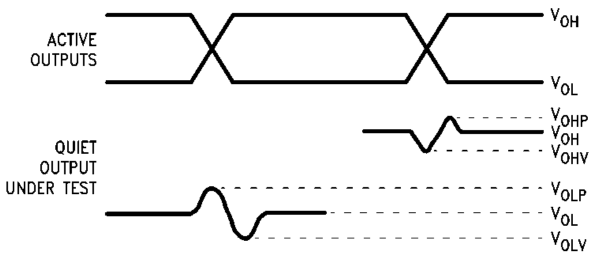


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note 10: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 11: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

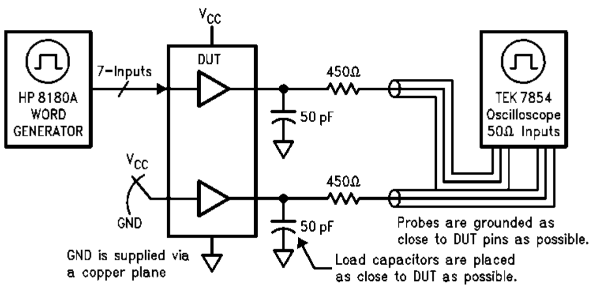
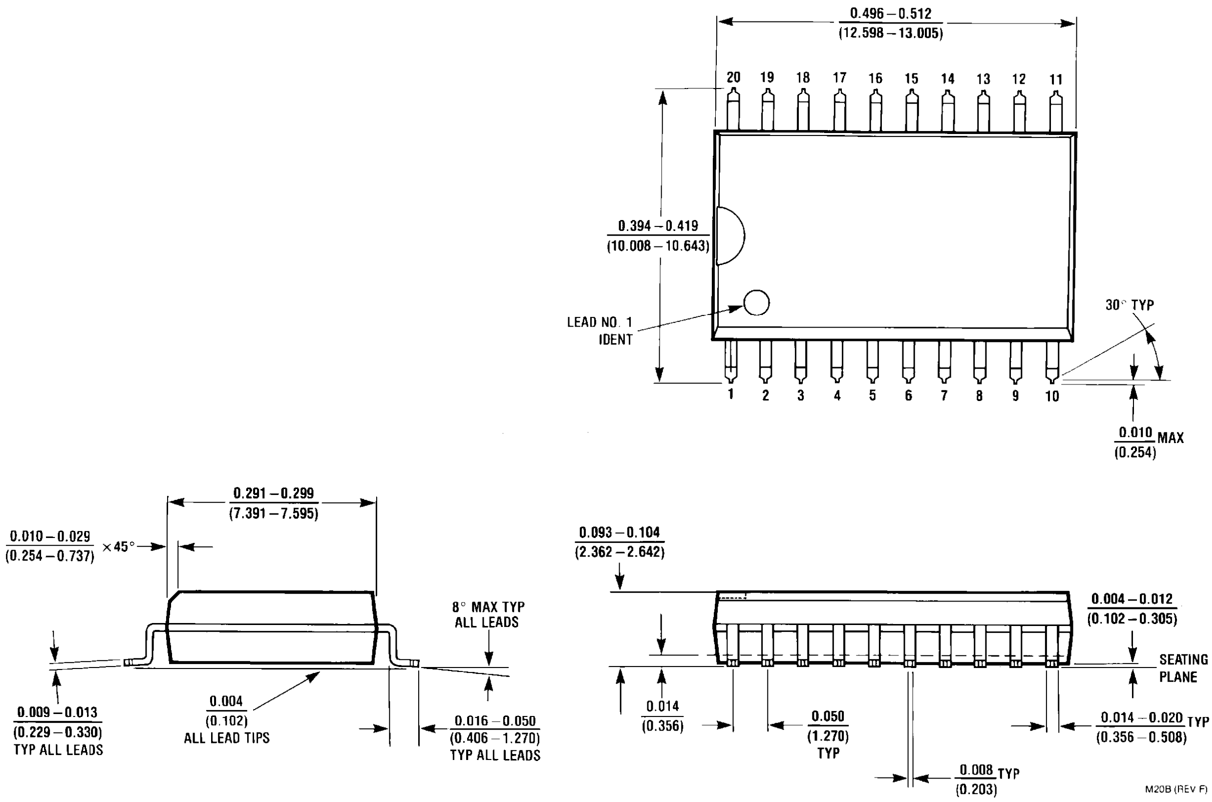


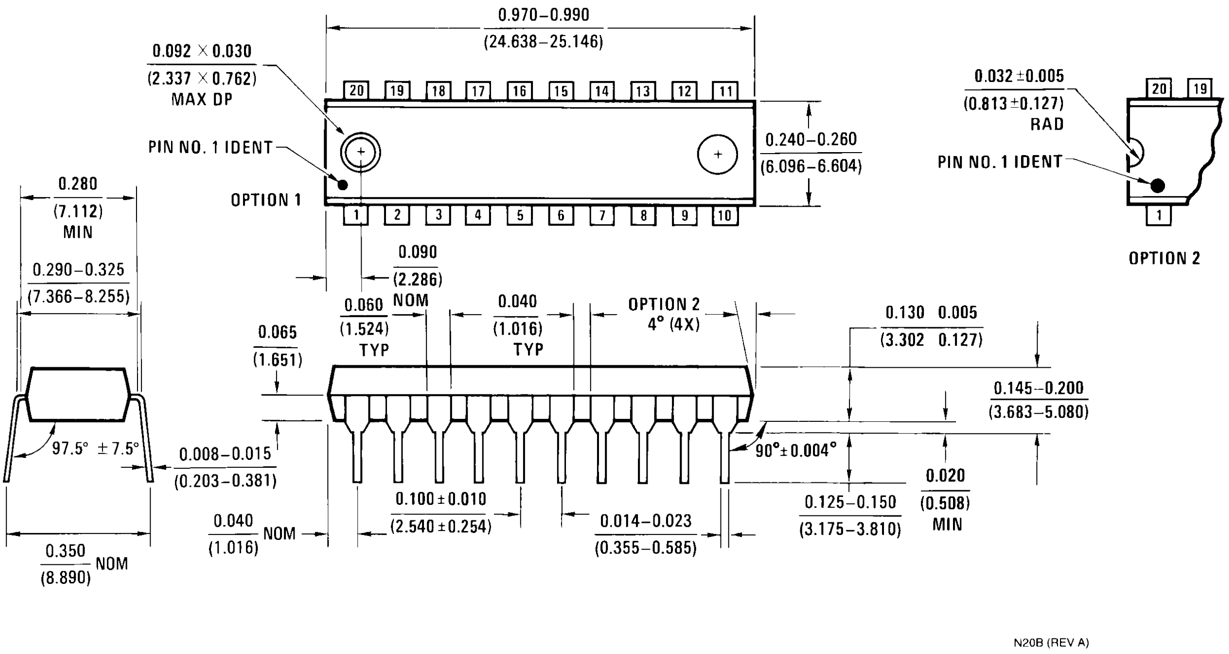
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit, JEDEC MS-013, 0.300” Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide
Package Number N20A

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