FAIRCHILD SEMICONDUCTOR™

November 1988
Revised August 2000

74AC109 • 74ACT109
Dual JK Positive Edge-Triggered Flip-Flop

General Description

The AC/ACT109 consists of two high-speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D-Type flip-flop (refer to AC/ACT74 data sheet) by connecting the J and K inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

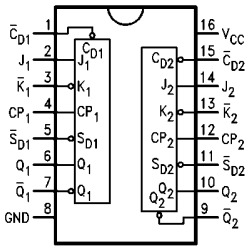
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- ACT109 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74AC109SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC109MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC109PC	N16E	16-Lead Plastic Dual-in-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74AC109MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT109PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

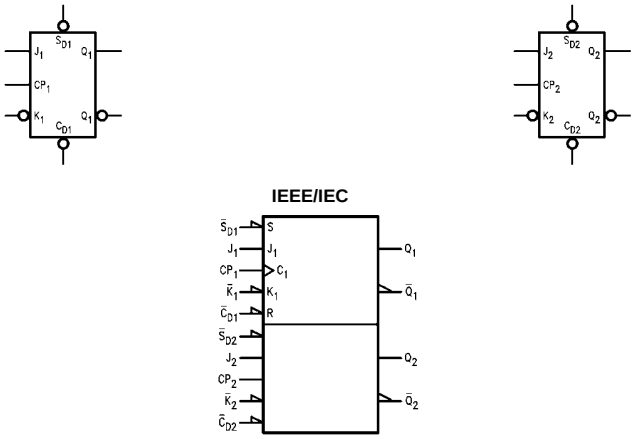


Pin Descriptions

Pin Names	Description
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Logic Symbols



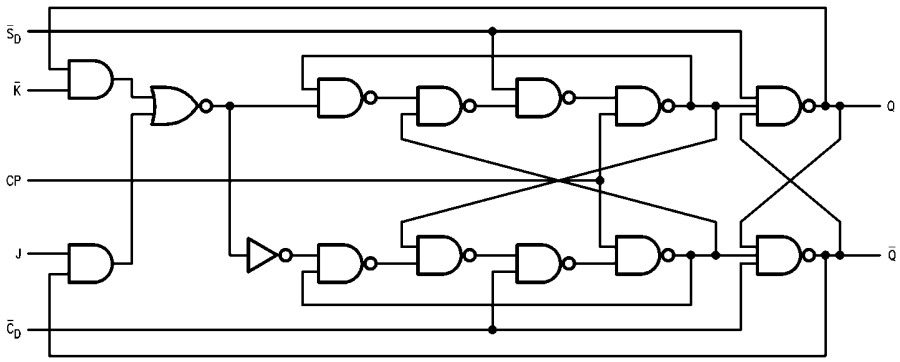
Truth Table

(each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW-to-HIGH Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	T_A = +25°C	T_A = −40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.46		I_{OH} = −12 mA
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.44		I_{OL} = 12 mA
		4.5		0.36	0.44	V	I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	V_I = V_{CC}, GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 5)
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 5)
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	$FV_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 6)	5.5			−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0	µA	$V_{IN} = V_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units
f_{MAX}	Maximum Clock Frequency	3.3	125	150		100		MHz
		5.0	150	175		125		
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	4.0	8.0	13.5	3.5	16.0	ns
		5.0	2.5	6.0	10.0	2.0	10.5	
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	3.0	8.0	14.0	3.0	14.5	ns
		5.0	2.0	6.0	10.0	1.5	10.5	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.0	8.0	12.0	2.5	13.0	ns
		5.0	2.5	6.0	9.0	2.0	10.0	
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.0	10.0	12.0	3.0	13.5	ns
		5.0	2.0	7.5	9.5	2.0	10.5	

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V_{CC} (V) (Note 8)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW	3.3	3.5	6.5	7.5	ns
	J_n or $\overline{K}_n$ to CP_n	5.0	2.0	4.5	5.0	
t_H	Hold Time, HIGH or LOW	3.3	−1.5	0	0	ns
	J_n or $\overline{K}_n$ to CP_n	5.0	−0.5	0.5	0.5	
t_W	Pulse Width	3.3	2.0	7.0	7.5	ns
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	2.0	4.5	5.0	
t_{REC}	Recovery Time	3.3	−2.5	0	0	ns
	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	−1.5	0	0	

Note 8: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V) (Note 9)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	145	210		125		MHz
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.0	11.0	3.5	13.0	ns
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	2.5	11.5	ns
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	5.5	9.5	2.0	10.5	ns
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	6.0	10.0	2.0	11.5	ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

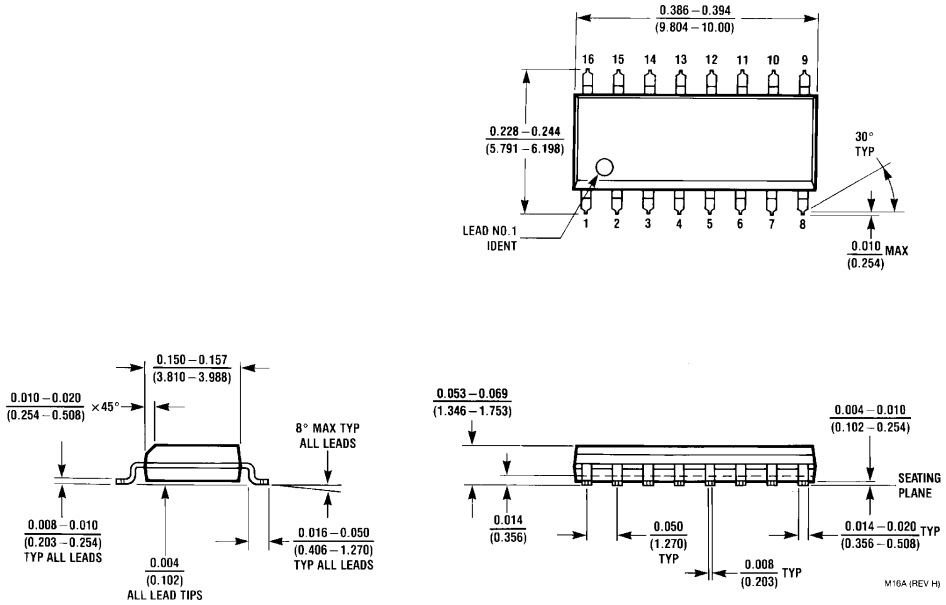
Symbol	Parameter	V_{CC} (V) (Note 10)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	ns
t_H	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	ns
t_W	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	6.0	ns
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	−2.5	0	0	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

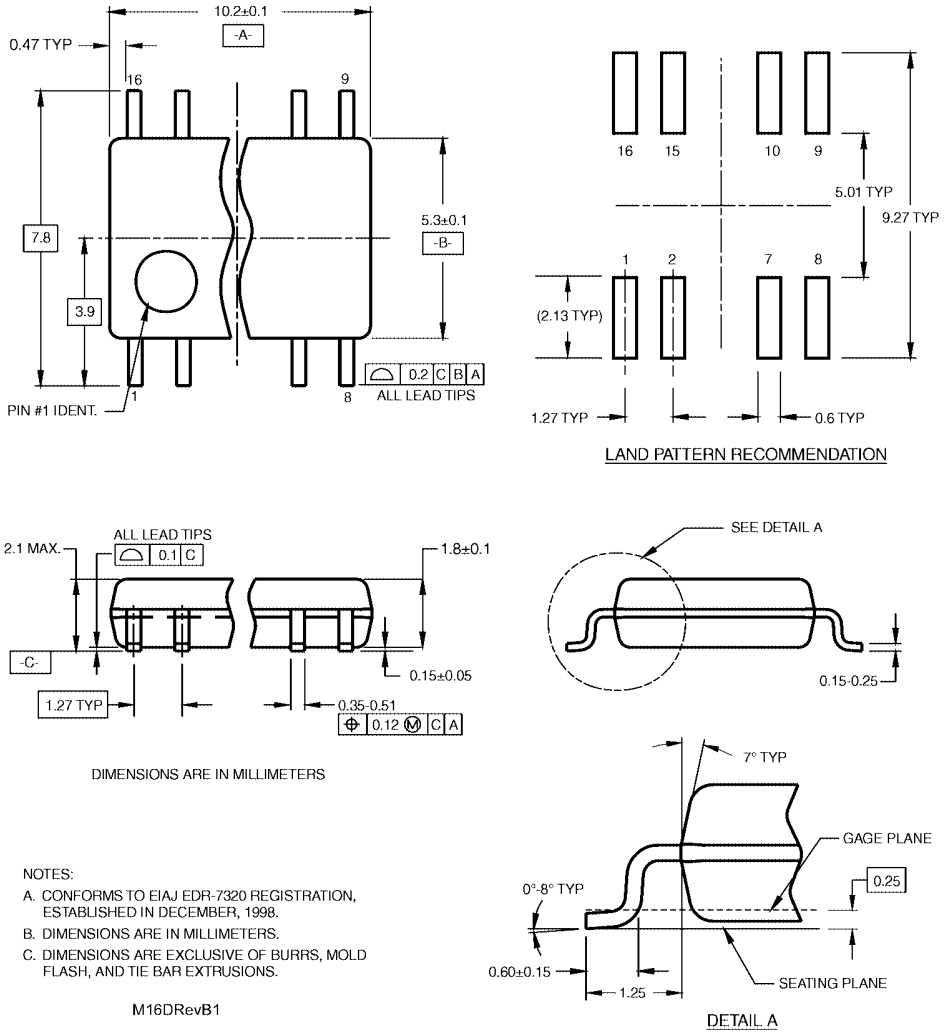
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

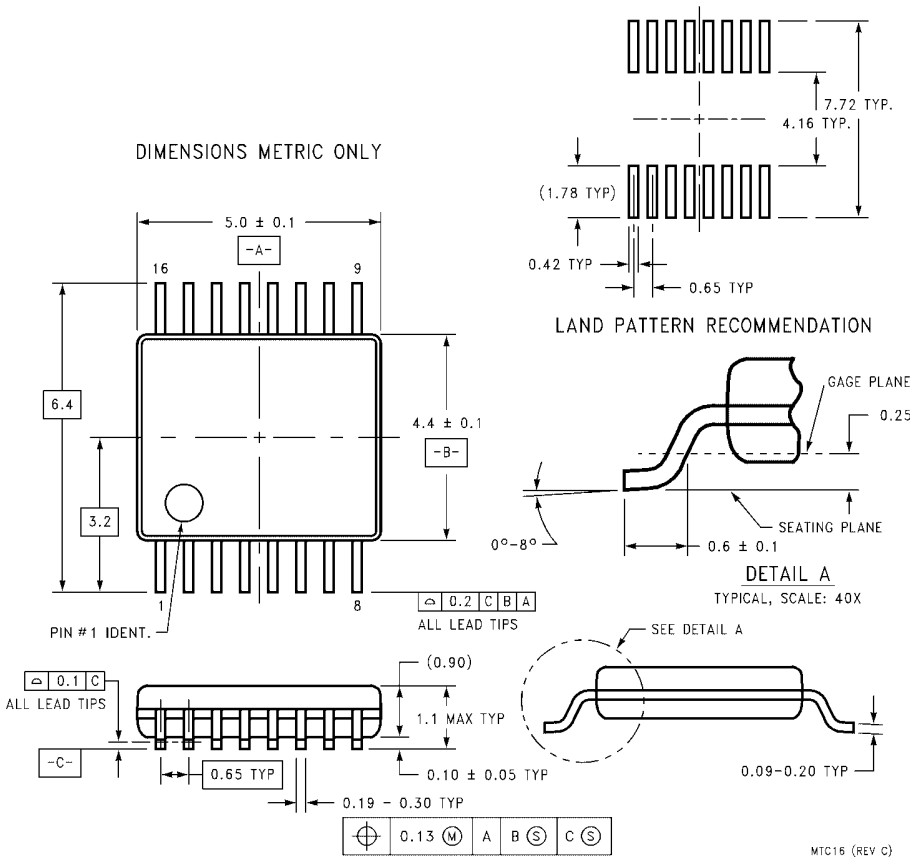
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

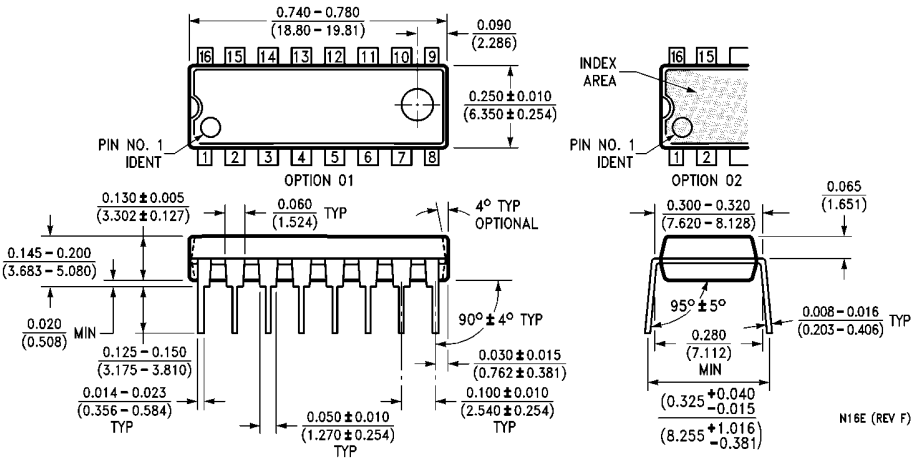
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E