

74ACT563 Octal Latch with 3-STATE Outputs

General Description

The ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

The ACT563 device is functionally identical to the ACT573, but with inverted outputs.

Features

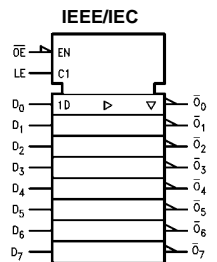
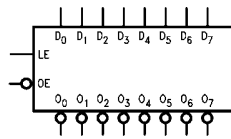
- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- ACT563 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74ACT563SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body

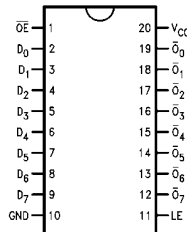
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram

Pin Assignment
for SOIC



Pin Descriptions

Pin Names	Description
D_0 - D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	3-STATE Output Enable Input
\overline{O}_0 - \overline{O}_7	3-STATE Latch Outputs

Functional Description

The ACT563 contains eight D-type latches with 3-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on

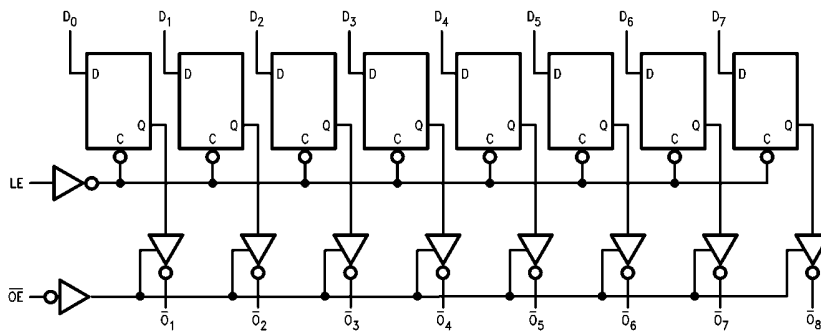
the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Junction Temperature (T_J) (PDIP)	
Supply Voltage (V_{CC})	-0.5V to +7.0V	140°C	
DC Input Diode Current (I_{IK})		Recommended Operating Conditions	
$V_I = -0.5V$	-20 mA	Supply Voltage (V_{CC})	4.5V to 5.5V
$V_I = V_{CC} + 0.5V$	+20 mA	Input Voltage (V_I)	0V to V_{CC}
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Output Voltage (V_O)	0V to V_{CC}
DC Output Diode Current (I_{OK})		Operating Temperature (T_A)	-40°C to +85°C
$V_O = -0.5V$	-20 mA	Minimum Input Edge Rate ($\Delta V/\Delta t$)	
$V_O = V_{CC} + 0.5V$	+20 mA	V_{IN} from 0.8V to 2.0V	
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$	V_{CC} @ 4.5V, 5.5V	125 mV/ns
DC Output Source or Sink Current (I_O)	± 50 mA	Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.	
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		

DC Electrical Characteristics

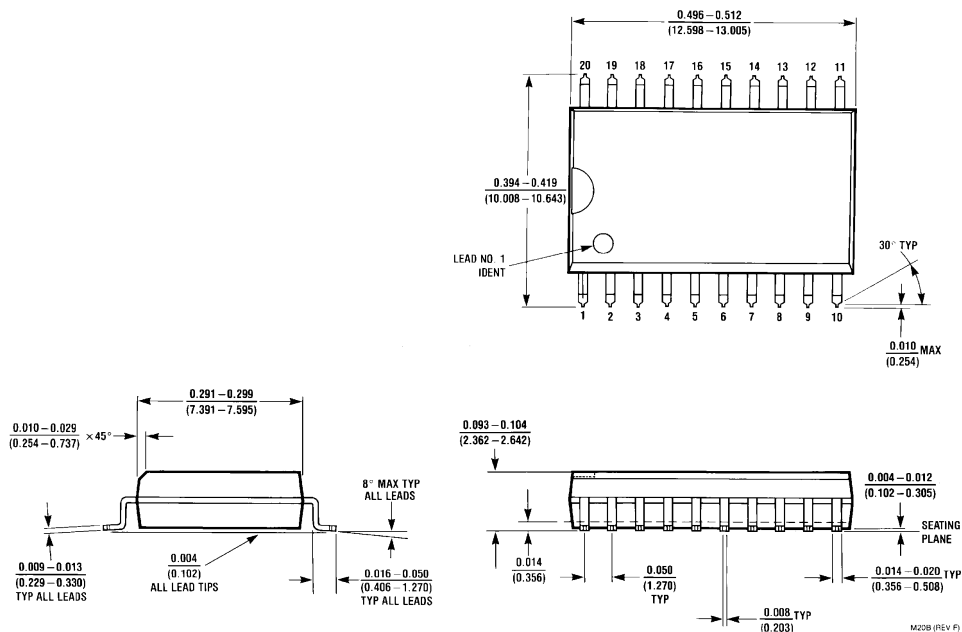
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ (Note 2)	
		5.5		4.86	4.76			
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44			V
5.5		0.36	0.44					
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{ GND}$	
I_{OZ}	Maximum 3-STATE Current	5.5		± 0.25	± 2.5	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{ GND}$	
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
I_{OHD}		5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics								
Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to \overline{O}_n	5.0	3.0	7.0	11.5	2.5	12.5	ns
t _{PHL}	Propagation Delay D _n to \overline{O}_n	5.0	3.0	6.0	10.0	2.5	11.0	ns
t _{PLH}	Propagation Delay LE to \overline{O}_n	5.0	3.0	6.5	10.5	2.5	11.5	ns
t _{PHL}	Propagation Delay LE to \overline{O}_n	5.0	2.5	5.5	9.5	2.0	10.5	ns
t _{PZH}	Output Enable Time	5.0	2.5	5.5	9.0	2.0	10.0	ns
t _{PZL}	Output Enable Time	5.0	2.0	5.5	8.5	2.0	9.5	ns
t _{PHZ}	Output Disable Time	5.0	3.5	6.5	10.5	2.5	11.5	ns
t _{PLZ}	Output Disable Time	5.0	2.0	4.5	8.0	1.0	8.5	ns
Note 4: Voltage Range 5.0 is 5.0V ±0.5V								
AC Operating Requirements								
Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units	
			Typ	Guaranteed Minimum	Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	1.5	4.0	4.5		ns	
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	-2.0	0	0		ns	
t _w	LE Pulse Width, HIGH	5.0	2.0	3.0	3.0		ns	
Note 5: Voltage Range 5.0 is 5.0V ±0.5V								
Capacitance								
Symbol	Parameter	Typ	Units	Conditions				
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN				
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0V				

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body Package Number M20B

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