FAIRCHILD

SEMICONDUCTOR™

74ACTQ16245
16-Bit Transceiver with 3-STATE Outputs

General Description

The ACTQ16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each has separate control inputs which can be shorted together for full 16-bit operation. The T/$\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The ACTQ16245 utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control for superior performance.

Features

- Utilizes Fairchild FACT Quiet Series technology
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin output skew
- Bidirectional non-inverting buffers
- Separate control logic for each byte
- 16-bit version of the ACTQ245
- Outputs source/sink 24 mA
- Additional specs for multiple output switching
- Output loading specs for both 50 pF and 250 pF loads

Ordering Code:

Order Number	Package Number	Package Description
74ACTQ16245SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACTQ16245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol

Connection Diagram
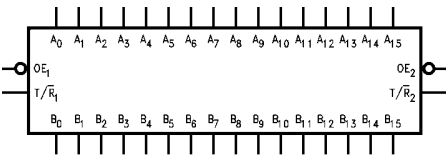
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/Outputs
B_0–B_{15}	Side B Outputs/Inputs
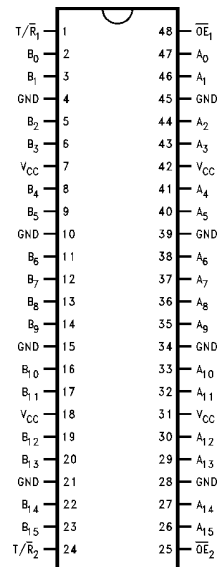
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Functional Description

The ACTQ16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the $T/\overline{R}$ input is HIGH, then Bus A data is transmitted to Bus B. When the $T/\overline{R}$ input is LOW, Bus B data is transmitted to Bus A. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each byte. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source/Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin	± 50 mA
Storage Temperature	−65°C to +150°C
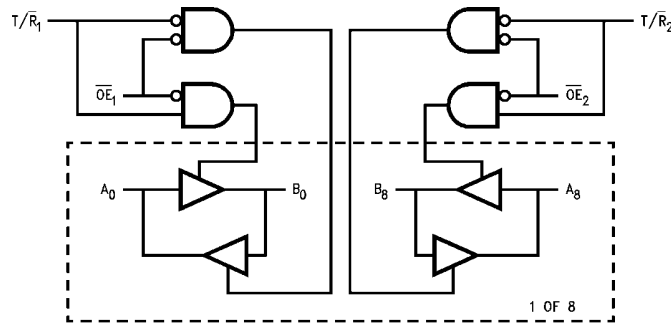
Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = +25°C Guaranteed Limits	T_A = −40°C to+85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum HIGH	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum LOW	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V
	Input Voltage	5.5	1.5	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum HIGH	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 µA
	Output Voltage	5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum LOW	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 µA
	Output Voltage	5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA
		5.5		0.36	0.44		I_{OL} = 24 mA (Note 2)
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} −2.1V
I_{CC}	Max Quiescent Supply Current	5.5		8.0	80.0	µA	V_{IN} = V_{CC} or GND
I_{OLD}	Minimum Dynamic	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5			−75	mA	V_{OHD} = 3.85V Min
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	0.5	0.8		V	Figure 1, Figure 2 (Note 5)(Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.5	−0.85		V	Figure 1, Figure 2 (Note 5)(Note 6)
V_{OHP}	Maximum Overshoot	5.0	V_{OH} + 1.0	V_{OH} + 1.5		V	Figure 1, Figure 2 (Note 4)(Note 6)
V_{OHV}	Minimum V_{CC} Droop	5.0	V_{OH} − 1.0	V_{OH} − 1.8		V	Figure 1, Figure 2 (Note 4)(Note 6)
V_{IHD}	Minimum HIGH Dynamic Input Voltage Level	5.0	1.7	2.0		V	(Note 4)(Note 7)
V_{ILD}	Maximum LOW Dynamic Input Voltage Level	5.0	1.2	0.8		V	(Note 4)(Note 7)

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

Note 4: Worst case package.

Note 5: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched LOW and one output held LOW.

Note 6: Maximum number of outputs that can switch simultaneously is n. (n − 1) outputs are switched HIGH and one output held HIGH.

Note 7: Max number of data inputs (n) switching. (n − 1) input switching 0V to 3V input under test switching 3V to threshold (V_{ILD})

AC Electrical Characteristics

Symbol	Parameter	V_CC (V) (Note 8)	T_A = +25°C C_L = 50 pF Min	T_A = +25°C C_L = 50 pF Typ	T_A = +25°C C_L = 50 pF Max	T_A = −40°C to +85°C C_L = 50 pF Min	T_A = −40°C to +85°C C_L = 50 pF Max	Units
t_{PLH}	Propagation Delay	5.0	3.2	5.7	8.4	3.2	9.0	ns
t_{PHL}	A_n, B_n to B_n, A_n	5.0	2.6	5.1	7.9	2.6	8.4	
t_{PZH}	Output Enable	5.0	3.7	6.4	9.4	2.7	10.0	ns
t_{PZL}	Time	5.0	4.1	7.4	10.5	3.4	11.6	
t_{PHZ}	Output Disable	5.0	2.2	5.4	8.7	2.2	9.3	ns
t_{PLZ}	Time	5.0	2.0	5.2	8.2	2.0	8.8	

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V.

Extended AC Electrical Characteristics

Symbol	Parameter	V_CC (V) (Note 9)	T_A = −40°C to +85°C C_L = 50 pF 16 Outputs Switching (Note 11) Min	T_A = −40°C to +85°C C_L = 50 pF 16 Outputs Switching (Note 11) Typ	T_A = −40°C to +85°C C_L = 50 pF 16 Outputs Switching (Note 11) Max	T_A = −40°C to +85°C C_L = 250 pF (Note 12) Min	T_A = −40°C to +85°C C_L = 250 pF (Note 12) Max	Units
t_{PLH}	Propagation Delay	5.0	4.2		11.9	5.9	14.6	ns
t_{PHL}	Data to Output	5.0	3.5		9.9	5.0	13.4	
t_{PZH}	Output Enable Time	5.0	4.5		11.4	(Note 13)		ns
t_{PZL}		5.0	4.4		12.2			
t_{PHZ}	Output Disable Time	5.0	3.5		9.3	(Note 14)		ns
t_{PZL}		5.0	3.1		8.8			
t_{OSHL} (Note 10)	Pin to Pin Skew HL Data to Output	5.0			1.2			ns
t_{OSLH} (Note 10)	Pin to Pin Skew LH Data to Output	5.0			1.3			ns
t_{OST} (Note 10)	Pin to Pin Skew LH/HL Data to Output	5.0			3.0			ns

Note 9: Voltage Range 5.0 is 5.0V ± 0.5V.

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}).

Note 11: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 12: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 13: 3-STATE delays are load dominated and have been excluded from the datasheet.

Note 14: The Output Disable Time is dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Capacitance

| Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Pin Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.

2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.

3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.

4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
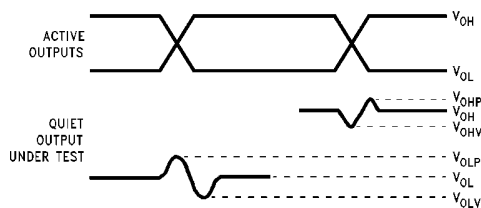
V_{OHV} and V_{OLP} are measured with respect to ground reference.

Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

• Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

• Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.

• Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

• Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

• First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.

• Next decrease the input HIGH voltage level, V_{IH}, until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.

• Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.
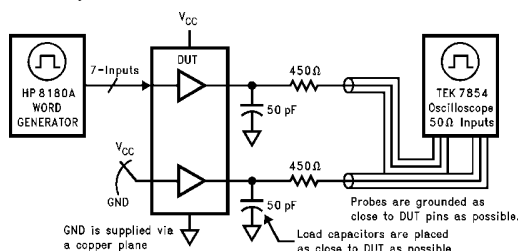
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted

0.620 – 0.630
[15.75 – 16.00]
– A –

48   25

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

1   24

0.025
[0.635] TYP

0.020±0.003
[0.51 ± 0.08]
TYP

0.008 – 0.012
[0.21 – 0.30] TYP

0.0031[0.08]Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –

– C –

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° – 8° TYP

0.004[0.10]
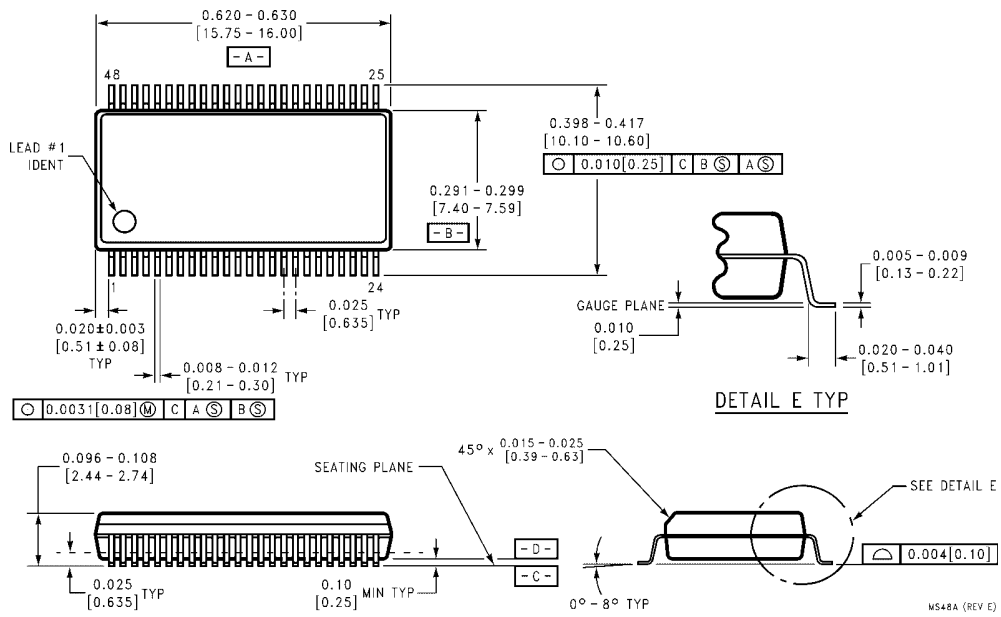
MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.50±0.10
-A-

0.40 TYP

48   43   30   25

8.10

4.05

6.10±0.10
-B-

1   6   19   24

PIN #1 IDENT.

⌓ 0.2 C B A
ALL LEAD TIPS

48   43   30   25

4.60   9.20

2.30

1   6   19   24

0.30

0.50

LAND PATTERN RECOMMENDATION

⌓ 0.1 C
ALL LEAD TIPS

1.2 MAX

-C-

0.50

0.17-0.27

0.90 +0.15 -0.10

0.10±0.05

⊕ 0.13 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

1.25

0 °-8°

0.60±0.10

1.00

SEATING PLANE

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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